

# 2SJ575

Silicon P Channel MOS FET  
High Speed Switching

# HITACHI

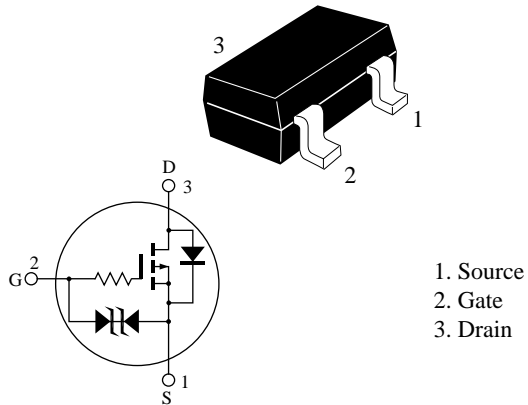
ADE-208-740B (Z)  
3rd.Edition.  
June 1999

## Features

- Low on-resistance  
 $R_{DS} = 2.8$  typ. ( $V_{GS} = -10$  V,  $I_D = -50$  mA)  
 $R_{DS} = 5.7$  typ. ( $V_{GS} = -4$  V,  $I_D = -50$  mA)
- 4 V gate drive device.
- Small package (MPAK)

## Outline

MPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-100	mA
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	-400	mA
Body-drain diode reverse drain current	$I_{DR}$	-100	mA
Channel dissipation	Pch <sup>Note 2</sup>	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW 10 μs, duty cycle 1%

2. Value on the alumina ceramic board (12.5x20x0.7mm)

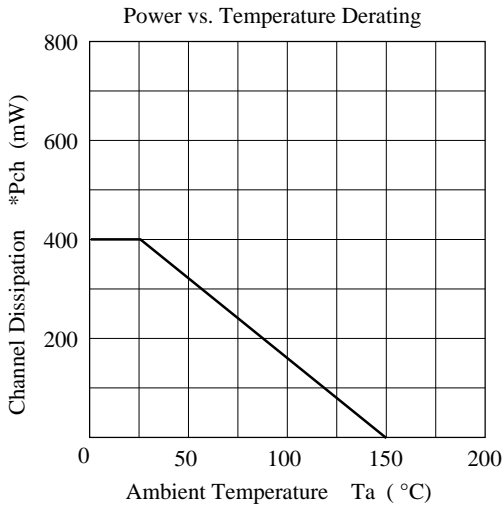
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	μA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.3	—	-2.3	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.3		$I_D = -50 mA, V_{GS} = -10 V$ <sup>Note 3</sup>
	$R_{DS(on)}$	—	5.7	7.9		$I_D = -50 mA, V_{GS} = -4 V$ <sup>Note 3</sup>
Forward transfer admittance	$ y_{fs} $	68	105	—	mS	$I_D = -50 mA, V_{DS} = -10 V$ <sup>Note 3</sup>
Input capacitance	Ciss	—	25	—	pF	$V_{DS} = -10 V$
Output capacitance	Coss	—	20	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	8	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = -50 mA, V_{GS} = -10 V$
Rise time	$t_r$	—	15	—	ns	$R_L = 200$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	$t_f$	—	45	—	ns	

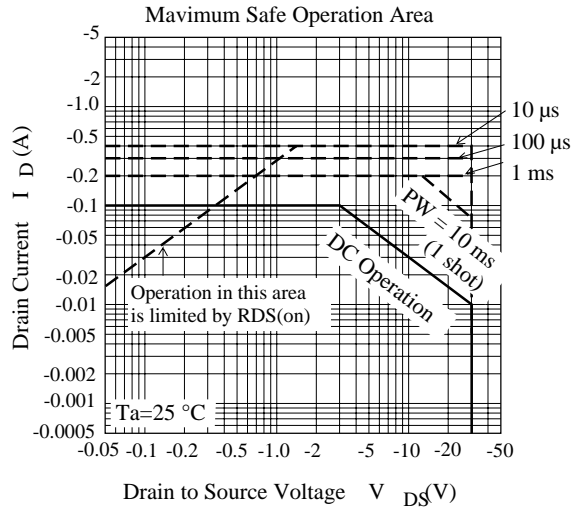
Note: 3. Pulse test

4. Marking is AP

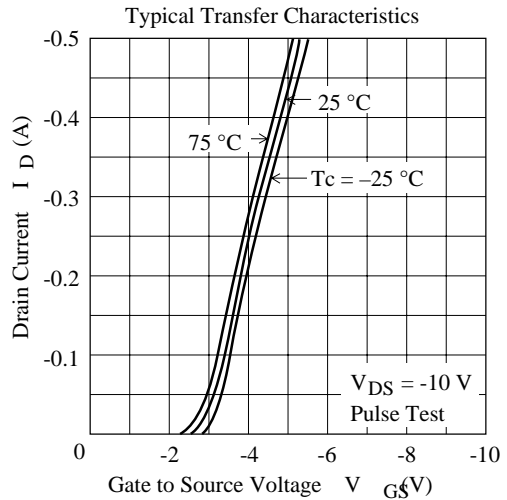
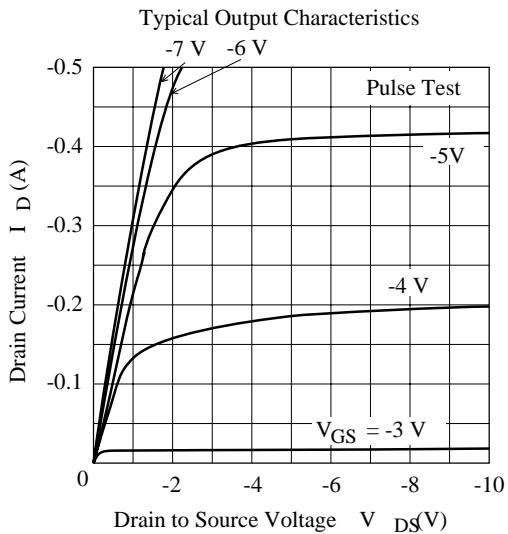
## Main Characteristics



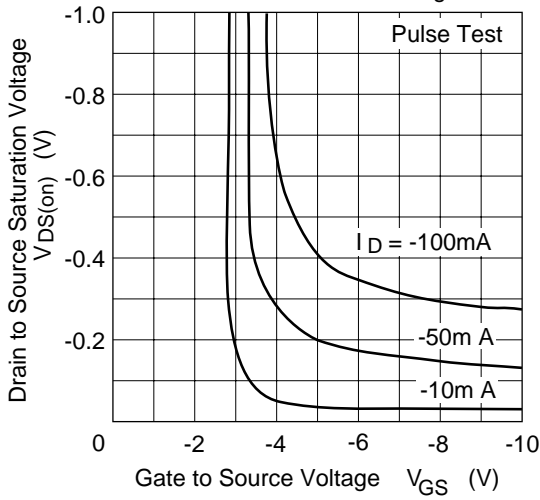
\*Value on the alumina ceramic board (12.5x20x0.7mm)



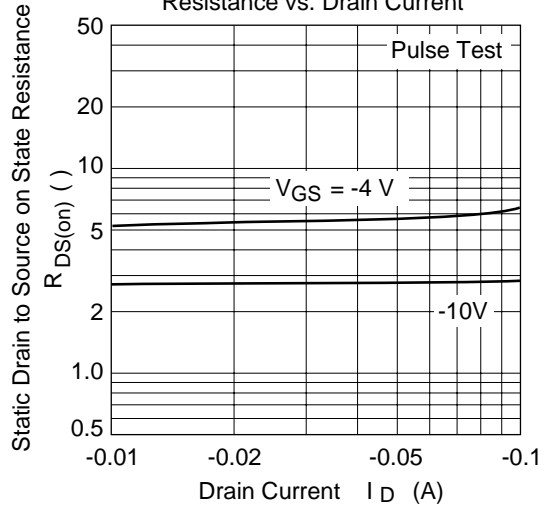
Value on the alumina ceramic board (12.5x20x0.7mm)



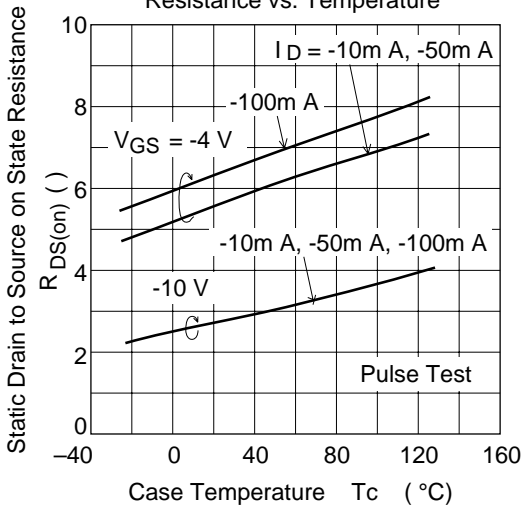
Drain to Source Saturation Voltage vs. Gate to Source Voltage



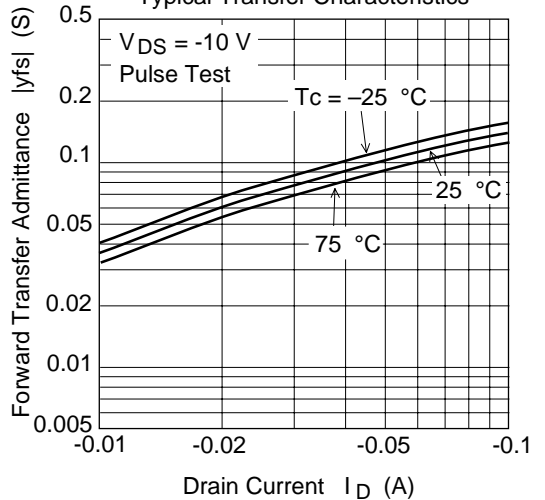
Static Drain to Source on State Resistance vs. Drain Current

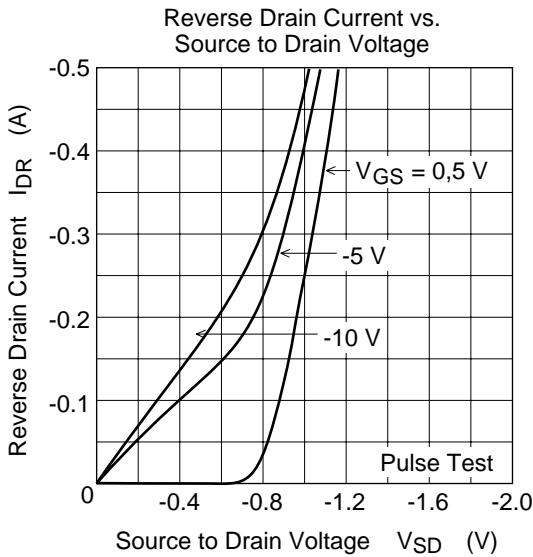
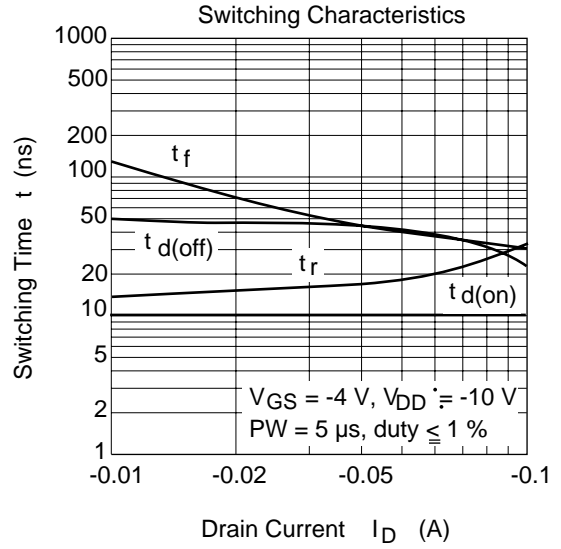
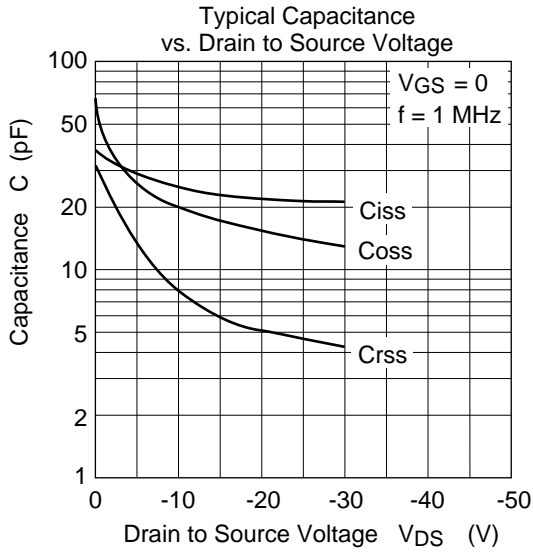


Static Drain to Source on State Resistance vs. Temperature

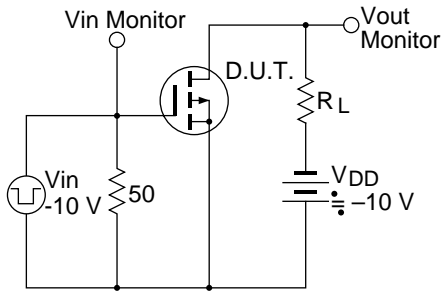


Typical Transfer Characteristics

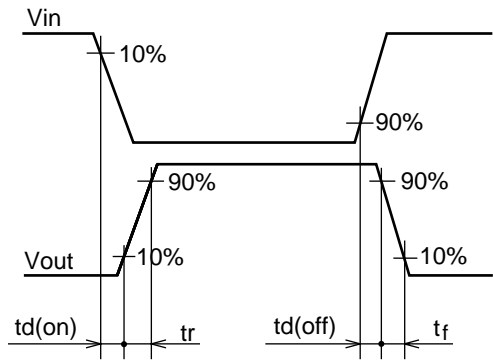




Switching Time Test Circuit

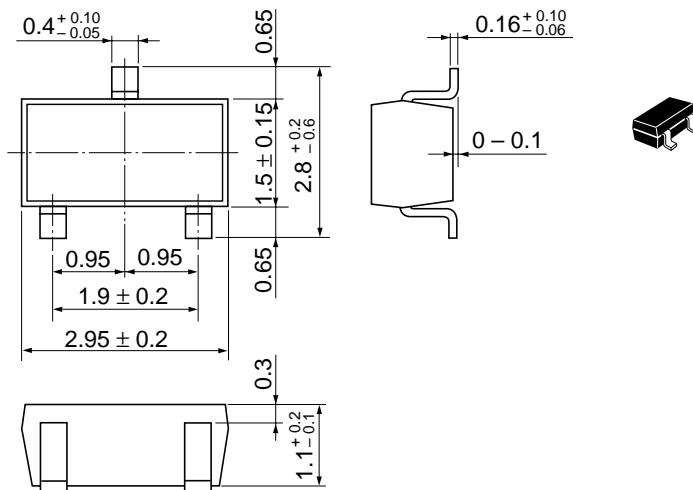


Waveforms



Package Dimensions

As of January, 2001  
Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

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