Smart Part™

* Direction discriminator indentifies & measures forward or backward rotation/direction

* Pulse width measurement

* Frequency measurement

* Cascadable 16-bit up/down counter (THCT12016)

* 24-bit up/down counter (THCT12024)

* TTL compatible

* 8-bit bus parallel 3-state interface

* Simple write & read procedure

* High speed 20Mhz clock operation

* THCT12016 ONLY:

* 1:1 Replacement for the popular LS2000AN/THCT2000NL

* THCT12024 ONLY:

  - 24-bit resolution
  - Small 24-pin 300 mil package
  - Separate Ua0 counter reset

THCT12016NL
28 Pin/600mil

THCT12024NL
24Pin/300mil

Fig 1 Dual-in-line Pinout
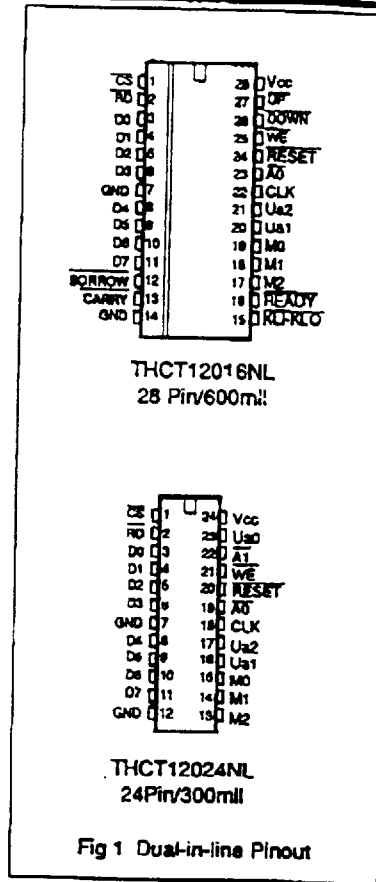
Description

The THCT12016, 2024 incremental encoder interface can independently determine the direction or displacement of a mechanical device or axis based on two input signals from transducers in quadrature. Alternatively, it can measure a pulse width using a known clock rate, or a frequency, by counting input pulses over a known time interval. It includes one 16-bit or 24-bit counter which may also be used separately(*). The THCT12016 may be cascaded to provide accuracy greater than 16-bits. Both devices are designed for use in many microprocessor based systems.

(*) THCT12016 only

Applications

The THCT12016/12024 enables mechanical devices to be interfaced with micro-processors. It may be used in many diverse applications, including robotics, printers/plotters, trackers balls (or mouse), lathes or machine tools. automobiles. conveyor belts and transport mechanisms.

Architecture

The four main elements of the THCT12016 are shown in Fig 2 :-

1. The measurement and mode control logic generates up or down count pulses, internal signals (I1 and I2), from the quadrature signals Ua1 and Ua2. the clock input and from Mode Controls (M0,M1,M2).

2. The control logic provides common microprocessor interface signals.

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Architecture - continued

3. The output multiplexer allows the processor to select data from either the upper (MS-byte) or lower (LS-byte)

4 The 3-state buffers place this data on the bus.

The THCT12024 architecture, shown in Fig 3, is very similar to that of the THCT12016, except for the up/down counter which has 24-bits and can be independently reset by Ua0. The cascading feature has also been removed to permit use of a smaller slimline package (300 mil 24-pin).

LS2000A/THCT2000 Compatibility

The THCT12016 is a pin-for-pin replacement for the LS2000A and THCT2000. However some differences exist which may require modifications to existing LS2000A/THCT2000 applications.

The differences are :

	LS2000A	THCT2000N	THCT12016
/READY output	Open collector with pull-up (5KΩ nom)	Open drain without pull-up	Push-pull output
/KLI-KLO input/output(*)	Open collector with pull-up (5KΩ nom)	Open drain without pull-up	Open drain with pull-up (10kΩ nom)
DATA BUS outputs	I_{ol}= 8mA (3-state) I_{oh}= -0.4MA	I_{ol}= 4mA (3-state) I_{oh}= -4mA	I_{ol}= 8mA (3-state) I_{oh}= -8mA

(*) see configuration section - Page 9

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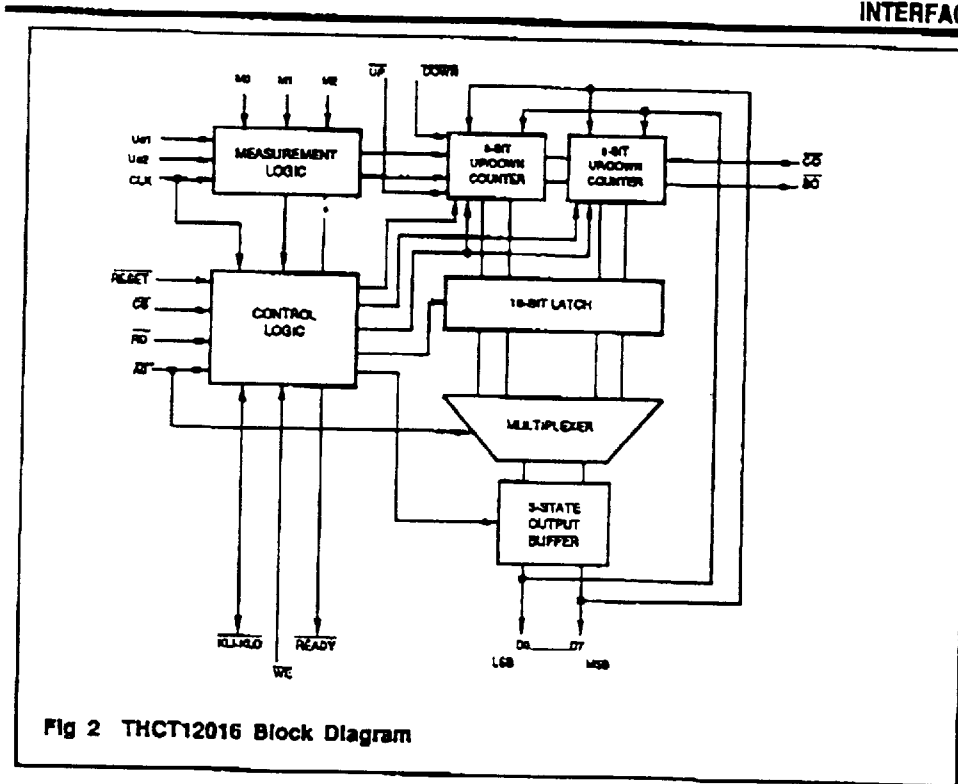
Fig 2   THCT12016 Block Diagram
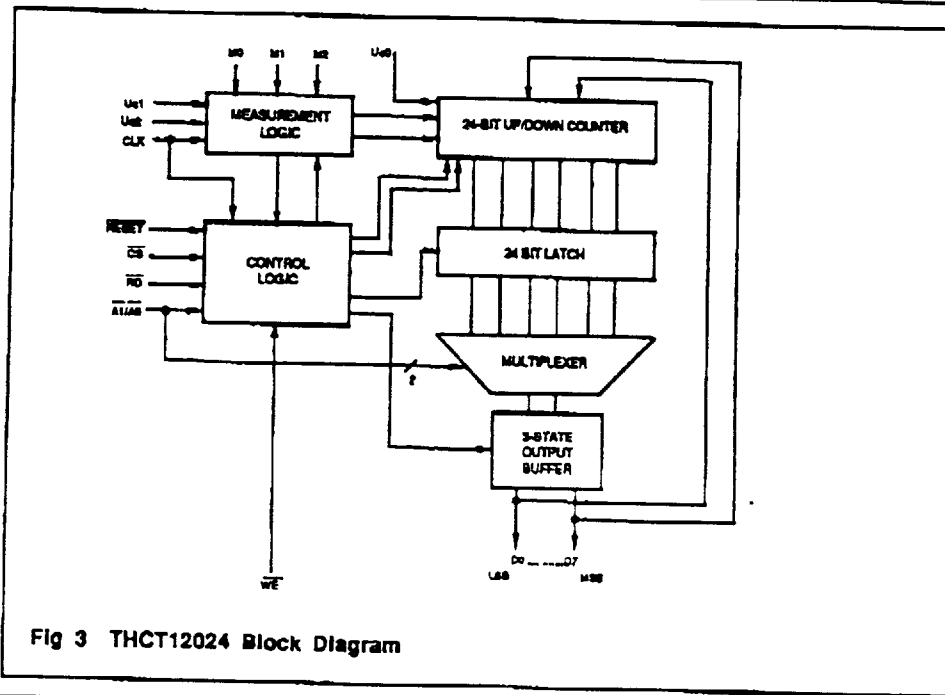
Fig 3   THCT12024 Block Diagram

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Operation

The eight modes of operation of the THCT12016/12024 are summarised in Table 1.

MODE	M2n	M1n	M0n	MODE DESCRIPTION
0	0	0	0	**COUNTER** 16-bit(THCT12016 only) up/down counter (Inhibits direction discriminator)
1	0	0	1	**DIRECTION DISCRIMINATOR** Single count pulse synchronous with Ua1 rising in forward direction and Ua1 falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2 rising in forward direction and Ua2 falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1 rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2 rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
6	1	1	0	**PULSE WIDTH MEASUREMENT** Ua1 is the gate signal Ua2 is high for up counting and low for down counting. Count is synchronous with rising clock.
7	1	1	1	**FREQUENCY MEASUREMENT** Ua1 is frequency signal to be measured Ua2 is the gate signal of known time interval. Count is synchronous with rising edge of Ua1

Table 1 : THCT12016/12024 Operational Modes

MODE 0: 16-BIT UP/DOWN COUNTER MODE

In this mode, the THCT12016 may be used as fast 16-bit up/down counter with cascade capability. This is operated using the /UP and /DOWN inputs.

The states of the counter outputs are transferred to a 16-bit latch. The contents of this 16-bit latch are multiplexed onto an 8-bit parallel data bus (D0.. D7) and enabled using /RD and /CS.

/A0 is the control input for the byte multiplexer. A high level at this input transfers the least significant byte to the data outputs and a low level transfers the most significant byte.

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Operation - continued

The up/down counters are loaded in individual 8-bit bytes by the /WE and /CS signals, with the byte selected by the /A0 input. The counter may be cleared using the /RESET signals (which clears both counter and control logic),or individually, using the Ua0 signal (THCT12024 only).

Cascading to n-bits is possible using inputs /UP and /DOWN, outputs /BORROW, /CARRY and the input-outputs /KLI-KLO (THCT12016 only).

NOTE The THCT12024 cannot be used in Mode 0 since /UP and /DOWN Inputs are not available.

To read or load the 24-bit(THCT12024 only) in all modes, /CS, /RD or /WE, /A0 and /A1 are used to perform the Read or Write operation. The operation should always start with the LSB (/A0=/A1=HIGH), followed by the LSB+1 (/A0=LOW, /A1=HIGH) and then the MSB (/A0=HIGH, /A1=LOW).

/A0	BYTE
H	LSB
L	MSB

(a) THCT12016

/A0	/A1	BYTE
H	H	LSB
L	H	LSB + 1
H	L	MSB

(b) THCT12024

Table 2 - ADDRESS SELECT

MODES 1-5: DIRECTION DISCRIMINATOR MODES

The quadrature signals Ua1 and Ua2, identify forward and backward directions. If Ua1 leads Ua2, the forward direction is indicated and the counter will count up; if Ua1 lags Ua2, the reverse direction is indicated and the counter will count down.
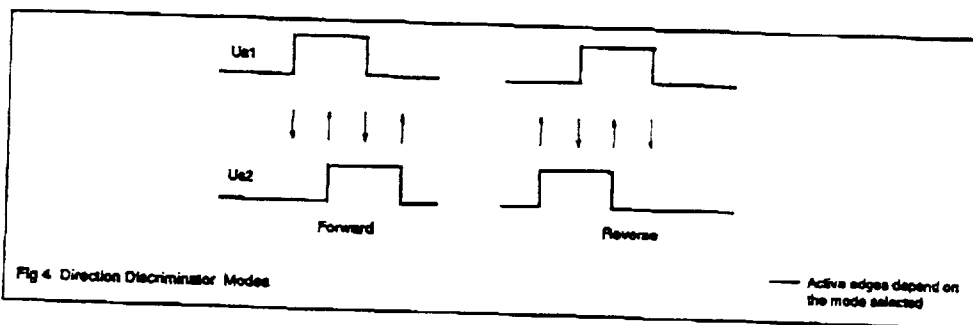

Fig 4 Direction Discriminator Modes

— Active edges depend on the mode selected

Both Ua1 and Ua2 are stored on the clock falling edge in the first of a pair of consecutive D-type flip flops, and are transferred to the next on the clock rising edge. By comparing the states of the four flip flops and checking the mode inputs, the up or down count pulses are generated - see Figs 4 & 5.

Modes 1 to 5 define which edge of the quadrature signals will be counted in accordance with Table 1.

The clock frequency should be at least four times greater than the frequencies of the quadrature signals : this will eliminate problems resulting from timing jitter in the transducer signals and will allow the quadruple counting mode to be used. The frequency of the quadrature signals, Ua1 and Ua2 may be calculated from the relationship :

$$F = \frac{\text{Shaft Speed}}{\text{Resolution of Transducer}}$$

Operation - continued

CLK		M2	M1	M0
Ua1				
Ua2				
SINGLE Ua1		0	0	1
SINGLE Ua2		0	1	0
DOUBLE Ua1		0	1	1
DOUBLE Ua2		1	0	0
QUADRUPLE Ua1 and Ua2		1	0	1

Fig 5 Direction Discriminator Up Clock

CLK		M2	M1	M0
Ua1				
Ua2				
SINGLE Ua1		0	0	1
SINGLE Ua2		0	1	0
DOUBLE Ua1		0	1	1
DOUBLE Ua2		1	0	0
QUADRUPLE Ua1 and Ua2		1	0	1

Fig 6 Direction Discriminator Down Clock
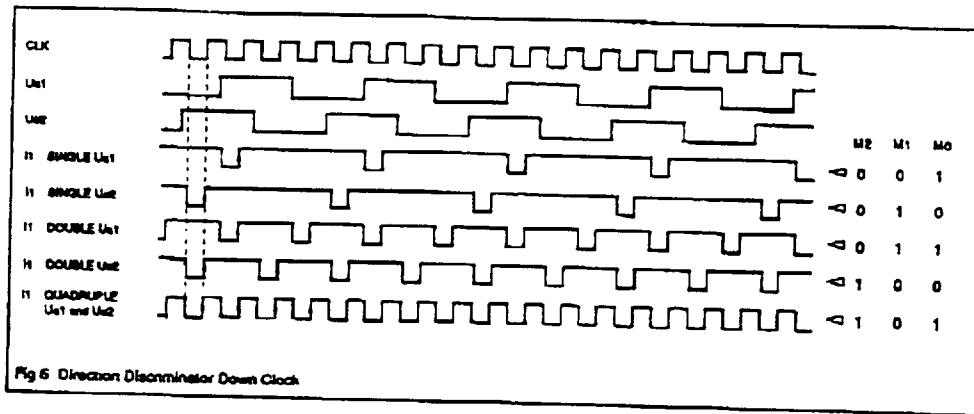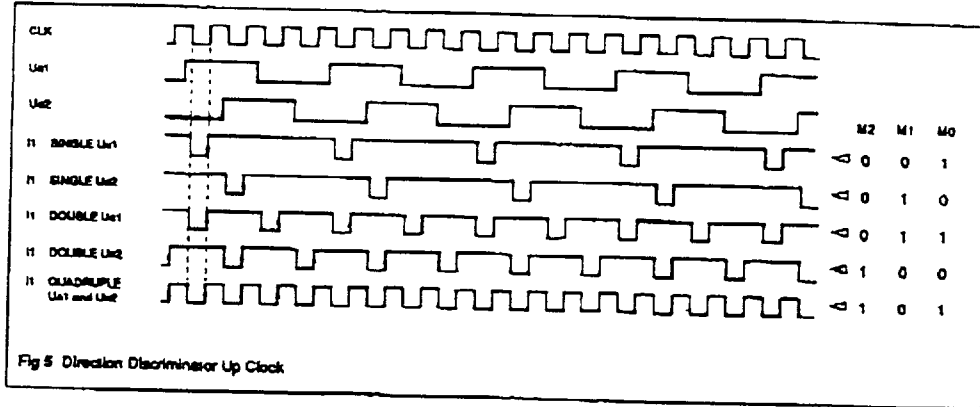
MODE 6: PULSE WIDTH MEASUREMENT MODE

In this mode, Ua1 acts as a gate, and is the pulse width to be measured. Synchronised with the clock edge after a low to high transition in Ua1, counting begins at the at the input clock frequency. Similarly, synchronised with the clock edge after a high to low transition of Ua1, counting is disabled. The value of the counter is loaded in the output register, /KLI-KLO (THCT12016 only) is pulled low and then the counter clears - see Fig 6. If Ua2 is held high, the counter will count up, and if Ua2 is held low, the counter will count down.

Each counter can be preloaded in two or three bytes (THCT12024 only) by activating /CS, /RD and selecting the individual bytes with /A0 and/or /A1 after Ua1 has fallen and before the next preload takes place.
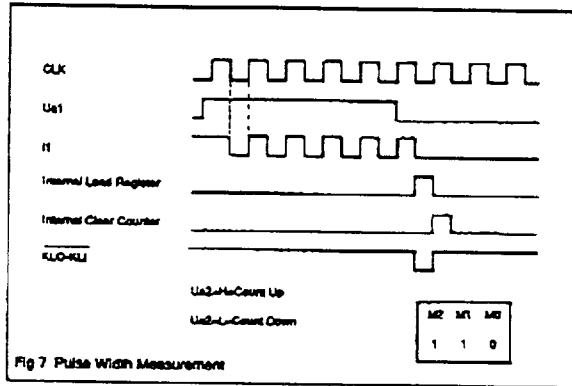
The /KLI-KLO signal (THCT12016 only) may be used as an interrupt to indicate to the processor when the register has been loaded. In the pulse width mode, the output register will not be loaded via /CS and /RD, but by the falling edge of Ua1.

Operation - continued

In pulse width mode, the minimum time that can be measured is :

$$Tmin = 2(To) \qquad (Accuracy\ is\ +/-\ To)$$

Fig 7 Pulse Width Measurement

MODE 7: FREQUENCY MEASUREMENT MODE

In mode 7, Ua1 is the signal of unknown frequency to be measured; Ua2 is a gate signal of known width. A low to high transition of Ua2 enables counting at the frequency of Ua1. When the gate (Ua2) goes low, counting is disabled. The value of the counter is loaded into the output register, /KLI-KLO is pulled low(THCT12016 only), and the counter is then cleared - see Fig 8.

Fig 8 Frequency Measurement
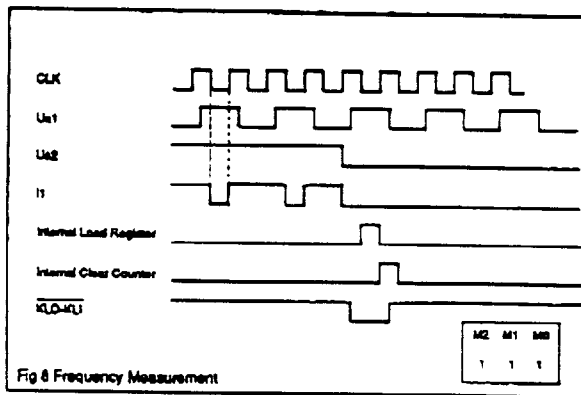
RESET OPERATION

A total reset is initiated by pulling the /RESET pin low. This will clear the counters to zero, reset the D-type flip flops at the inputs of the quadrature signals (Ua1 & Ua2), clear the latches that inhibit the load register pulse and load zero into the register. To avoid a spurious count after a reset (+/-1 error), the Ua1 and Ua2 inputs should be held to the values indicated in Table 3 during and just after the reset pulse.

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Operation · continued

MODE	Ua1	Ua2
0	X	X
1-5	H	H
6-7	L	L

Table 3 : Ua1 and Ua2 levels during reset operation

NOTE If a /RESET=LOW appears during a read or write cycle of the THCT12016, the /READY output will stay LOW as long /RESET is active.

CASCADING DEVICES (THCT12016 only)

The /KLI-KLO pins of all cascaded THCT12016's should be tied together, so that all of the devices load their output registers at the same time. When the 'Master' generates a pulse for the other THCT12016's, /KLI-KLO on the 'Master' works as an output, and /KLI-KLO on the slaves work as inputs. The /CARRY of one device should be tied to the /UP input of the next device in the cascade; similarly, /BORROW should be connected to /DOWN.

* THCT12024 only

READ OPERATION

When in modes 0 to 5, the contents of the counter can be read at any time by pulling /CS and /RD low. The most significant byte may be selected by setting /A0 to low, and the least significant byte may be read by setting /A0 high (THCT12016 only, for THCT12024 - see Table 2 on Page 5). This will cause a 'load output register' to be generated and /KLI-KLO will go low during the next low clock pulse. /READY (THCT12016 only) will also go low as the clock goes low and will stay low until /CS and/or /RD go high. The load output register pulse stores the current value of the counter in a 16-bit or 24-bit latch register : /A0 and /A1 (THCT12024 only) direct the selected byte through a multiplexer to the outputs : also /CS and /RD enable the 3-state outputs - see Fig 12

WRITE OPERATION

A number may be preloaded into the counter by pulling /CS and /WE low while using /A0/A1 (THCT12024 only)) to direct the value on the data bus to the selected byte of the counter. This will cause /READY (THCT12016 only) to go low on the next falling clock edge, and remain low until /CS or /WE goes high - see Fig 13.

The output register will be loaded immediately if /KLI-KLO (THCT12016 only) is pulled low externally : this signal comes normally from a cascaded device.

For Modes 6 & 7 - see the earlier description of these modes.

Configuration

Special consideration should be paid to the automatic configuration features of the THCT12016/12024. The purpose of the features is to allow for the different order of byte reads (high then low or low then high) of different processors when doing a word read across a byte wide bus and also to automatically configure when devices are cascaded.

Byte order configuration -

After a system reset has occurred, the first read operation (/RD & /CS=LOW) will store the value of /A0,/A1 into a latch within the device. From that time until the next system reset, the load output register pulse will only be generated during a read operation if /A0/A1 is at this stored value. This means that the internal load output register pulse is correctly generated for word operations regardless of the byte order of the particular processor. Special care should be taken when reading individual bytes to ensure that these operations are always done in a consistent order.

Configuration - continued

Cascaded Configuration (THCT12016 only)

After a system reset, the first device and channel to receive a read operation (/RD & /CS=low) configures itself into the "master" mode and outputs a pulse on /KLI-KLO. In cascaded operation, the /KLI-KLO pins of the cascaded channels are connected together and the input pulse on /KLI-KLO of the cascaded channels configures these to "slave" mode. On all subsequent read operations, the load output register pulse is only generated by the "master" channel for the appropriate polarity of /A0 and /A1(THCT12024 only), as noted above and this is fed to the "slave" devices via the /KLI-KLO connection. Special care must be taken when cascading devices or channels always to read in the same channel order as well as the byte order already mentioned - see also System Application.

Pin Description - (THCT12016/12024)

PIN NAME	PIN NUMBER		I/O	DESCRIPTION
	28Pin '12016	24Pin '12024		
/CS	1	1	Input	Chip Select. A low enables this device.
/RD	2	2	Input	Read. When this and /CS are active(low),the data from the output register will be present on the data bus.
D0 D7	3-6 8-11	3-6 8-11	Input (3-state)	Data bus buffer: 8-Bit bidirectional Output buffer with 3-state outputs connected to the microprocesor system.
/BORROW	12	-	Output (PP) THCT12016 only	Push-pull output of the counter under-flow signal
/CARRY	13	- (PP) THCT12016 only	Output	Counter overflow signal
/KLI-KLO	15	-	Input/ Output (OD with Pull-up) THCT12016 only	Cascade load input/cascade load output. Open drain output with internal 400uA pull-up. Can be an input or output according to configuration.

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Pin Description - (THCT12016/12024) - continued

PIN NAME	PIN NUMBER		I/O	DESCRIPTION
	28Pin '12016	24Pin '12024		
/READY	16	-	Output (PP) THCT12016 only	When active low, the signal indicates to the MPU that read or write may be completed. /READY falling edge is synchronous with CLK. The push pull output requires no external pull up resistor.
M0 M1 M2	19 18 17	15 14 13	Input	Mode select inputs(See Table 1)
Ua1 Ua2	20 21	16 17	Input	Measuring input signals
Ua0	-	23	Input THCT12024 only	Reset input for the 24-bit counter
CLK	22	18	Input	Clock - used for internal synchronisation and control timing.
/A0	23	19	Input	Byte select. - see Table 2.
/A1	-	22	Input THCT12024 only	Byte select. - see Table 2.
/RESET	24	20	Input	Device reset. When active (low),the control logic is reset to a known state and the counter is cleared.
/WE	25	21	Input	Write enable.When this and /CS are active (low), the data that is on the bus is loaded into the counter.
/DOWN	26	-	Input THCT12016 only	Cascade input for counting down.
/UP	27	-	Input THCT12016 only	Cascade input for counting up.
VCC	28	24	Input	Power supply voltage 5V +/- 10%.
GND	7,14	7,12	Ground, 0V	

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Absolute maximum ratings over operating free air temperature

Parameter	MIN	MAX	UNIT
Supply voltage, Vcc	-0.5	7.0	V
All input voltages, Vi (*)	-0.5	Vcc+0.5	V
Continuous current in any signal pin	-20	+20	mA
Continuous current through any Vcc or Ground pin	-50	+50	mA
Storage Temperature Range, Ts	-65	150	°C

(*) but not to exceed 7.0 volts or the input current limit

NOTE:

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation at these and any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum operating conditions for extended periods may affect device reliability.

Recommended operating conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX (**)	UNITS	
Vcc	Supply Voltage	4.5	5	5.5	V	
Vih	High Level Input Voltage	2.0		Vcc	V	
Vil	Low Level Input Voltage	0.0		0.8	V	
Ta	Operating Temperature Range	0		70	°C	

Electrical characteristics over recommended operating free air temperature range (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITIONS		MIN	TYP (**)	MAX	UNITS
V_{oh}	High Level Output Voltage -all except D0 - D7 and /KLI-KLO	Vcc = Min Vil = 0V Vih = Vcc	Ioh= -80uA	Vcc-0.1			V
			Ioh= -0.8mA	Vcc-0.2			V
			Ioh= -8mA	3.76			V
V_{ol}	Low Level Output Voltage -all except D0 - D7 and /KLI-KLO	Vcc = Min Vil = 0V Vih = Vcc	Iol= +80uA			0.1	V
			Iol= +8mA			0.4	V

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THCT12016,12024
INCREMENTAL ENCODER
INTERFACE

Electrical characteristics over recommended operating free air temperature range (unless otherwise noted) - continued

SYMBOL	DESCRIPTION	TEST CONDITIONS		MIN	TYP (**)	MAX	UNITS
V_{oh}	High Level Output Voltage D0 - D7 and /KLI-KLO only	Vcc = Min Vil = 0V Vih = Vcc	Ioh= -120uA	Vcc-0.1			V
			Ioh= -1.2mA	Vcc-0.2			V
			Ioh= -12mA	3.76			V
V_{ol}	Low Level Output Voltage D0 - D7 and /KLI-KLO only	Vcc = Min Vil = 0V Vih = Vcc	Iol= +240uA			0.1	V
			Iol= +24mA			0.4	V
I_{oz}/I_i	High Impedance State Output Current D0-D7	Vcc = Max Voz = Vcc (max) Vil = 0V Vih = Vcc	25°C over all temps	-0.6 -6		+0.6 +6	µA µA
I_{off}	Open Drain Leakage Current	Vcc = Max Vo = 0v-Vcc Vil = 0V-Vcc	25°C over all temps	-0.5 -5		+0.5 +5	µA µA
I_i	InputLeakage Current, except Ua0, /UP, DOWN,/A1 D0-D7	Vcc = Max Vi = 0V-Vcc	25°C over all temps	-0.1 -1		+0.1 +1	µA µA
I_{cc}	Supply Current D0-D7	Vcc = Max Input Mode Outputs Open	Standby Avg @ 20MHz			550 10	µA mA
I_o	Input Pull-up Current	Vcc=Min					
	/KLI-KLO		Vin = 0V	-200	-400	-1000	µA
	Ua0 (THCT12024) /UP, /DOWN		Vin = 0V	-47.5	-95	-238	µA
	/A1 (THCT12024)		Vin = 0V	-2.5	-5	-12.5	µA

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Timing requirements over recommended operating conditions

SYMBOL	PARAMETER	MIN	TYP (*)	MAX	UNITS
Tc1	Clk Cycle time,duty cycle 50%	50			ns
Tc1 ⊕	Clk Cycle time,duty cycle 50% ⊕ Cascaded Mode	100			ns
Tc2	Pulse width low CLK Tr, Tf<5ns	25			ns
Tc2 ⊕	Pulse width low CLK Tr, Tf<5ns ⊕ Cascaded Mode	50			ns
Twrs	Pulse width, /RESET input low	50			ns
Fmud	Maximum frequency, /UP or /DOWN, Input duty cycle 50% (THCT12016 only)	20	25		MHz
Fmud ⊕	Maximum frequency, /UP or /DOWN, Input duty cycle 50% (THCT12016 only) ⊕ Cascaded Mode	10	12.5		MHz
Twud	Pulse width, /UP or /DOWN input low (THCT12016 only)	25			ns
Twk	Pulse width, /KLI-KLO input low (THCT12016 only)	20			ns
Twrd1	Pulse width, /RD input low (Mode= 6 & 7)				ns
Twrd2	Pulse width, /RD input low (Mode= 0 TO 5)		Tc1		ns
Tdrd	Time between two or three* Read cycles (LSB or LSB+1*and MSB)	0			ns
Twwr	Pulse width /WE input low	25			ns
Tdwr	Time between two or three* Write cycles (LSB or LSB+1* and MSB)	0			ns
Tsd	Set Up time, Data prior to ↑ /WE	15			ns
Twua0	Pulse width, Ua0 input high*	25			ns
Tsus	Set Up time, /CS and /RD low before CLK falling edge	15			ns
Tsa	Set Up time, /A0/1* prior to /WE and /CS low	10			ns
Tsud	Set Up time, /UP or /DOWN rising edge before CLK falling edge (THCT12016 only)	20			ns

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Timing requirements over recommended operating conditions - continued

SYMBOL	PARAMETER	MIN	TYP (**)	MAX	UNITS
Tsab	Set Up time, UA1 or UA2 prior to CLK falling edge	15			ns
Tsda	Set Up time, data prior to ↑ /WE	Tsd			ns
Tsbb	Set Up time, UA2 stable before CLK falling edge	15			ns
Tsac	Set Up time, UA1 or UA2 rising edge before CLK falling edge	15			ns
Tsar	Set Up time, A0/1*stable before /CS and /RD low after reset	10			ns
Tsbc	Set Up time, UA1 or UA2 falling edge	15			ns
Tsr	Set Up time, /RESET high prior to CLK falling edge	0			ns
Tsuc	Set Up time, /UP or /DOWN rising edge prior to/KLI-KLO (input) falling edge (THCT12016 only)	20			ns
Thdw	Hold time DATA after ↑ /WE	10			ns
Twgp	Pulse width, Ua1N input high - (Mode= 6)		MIN 2 X Tc1		
Twgp	Pulse width, Ua2 input high - (Mode= 7)		MIN 2 X Tc1		ns
Tdgp	Pulse Width, Ua1 Input low (Mode = 6)		MIN 2 X Tc1		ns
Tdgf	Pulse Width, UA2 input low (Mode = 7)		MIN 1 X Tc1		ns
Tha	Address hold time after /WE or /CS high	12			ns
Thab	Ua1 or Ua2 Hold time after CLK falling edge	12			ns
Thda	D0-D7Hold time after/A0 or /A1* change	10			ns
Thac	Ua1 High hold time after CLK falling edge	12			ns
Thbc	Ua2 Hold time after CLK falling edge	12			ns

* THCT12024 ONLY

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Switching characteristics Vcc=Min, all temperatures, Freq=1MHz,Rl=1KOHMS, Cl=35pF (50pF bidirectional pins)

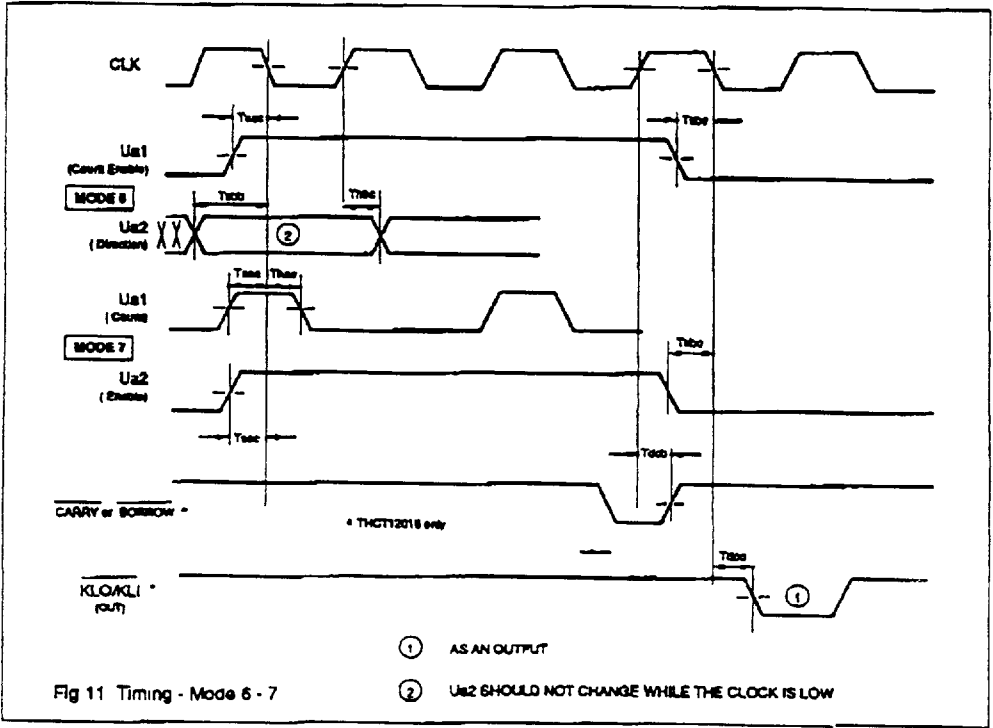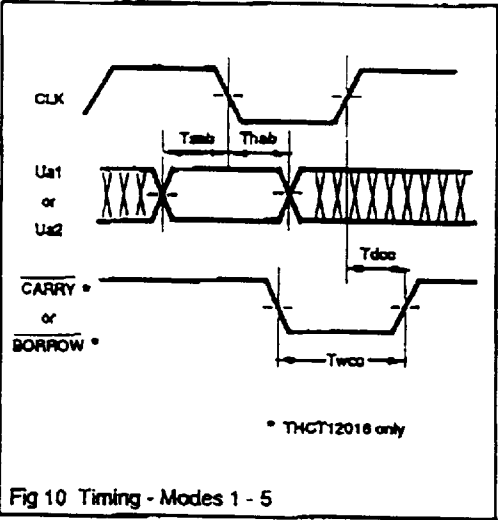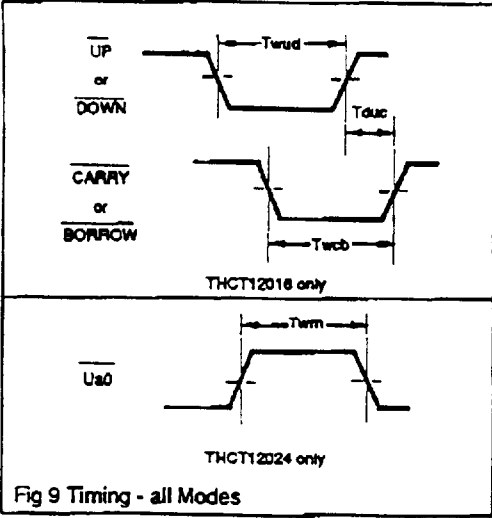| SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (**)	MAX	UNITS
Tdd1	Access time /RD and CLK to data output valid (Mode= 0 to 5)	From CLK ↓ Mode 1 Data >FD_{16} - >01_{16}			65	ns
Tdd2	Access time /RD to data output Mode=0-5, 2nd byte or 3rd byte* Mode=6-7 both bytes, or all three bytes* (* THCT12024 only)	From A0 ↓ Mode 1 Data >AA_{16}- >55_{16} valid From RD ↓ Mode 6 Data >FF_{16}- >00_{16} >00_{16}- >FF_{16}			45	ns
Thr	Propagation delay /RD, /WE or /CS Inactive to /READY (THCT12016 only)	from CS ↑			20	ns
Tdr	Propagation delay CLK to /READY low (THCT12016 only)				30	ns
Tduc	Propagation delay /UP or /DOWN rising edge to to /CARRY or /BORROW rising edge (THCT12016 only)	From /UPN ↑ to /CARRY ↑			35	ns
Tdcc	Propagation delay from CLK to /CARRY or /BORROW rising edge (THCT12016 ONLY)	From CLK ↑ to /CARRY or From CLK ↑ to /BORROW			25	ns
Tdc0	Propagation delay CLK falling edge to /KLI-KLO falling edge (THCT12016 only)				55	ns
Tdcb	Propagation Delay CLK rising edge to /CARRY or /BORROW rising edge (THCT12016 ONLY)	From CLK ↑ to /CARRY ↑ /BORROW ↑			25	ns

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Switching characteristics Vcc=Min, all temperatures, Freq≈1MHz, RI≈1KOHMS,
Cl=35pF (50pF bidirectional pins) - continued

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (***)	MAX	UNITS
Twc0	/KLI-KLO low output pulse width (THCT12016 only)			Tc2		ns
Ted	Enable time /RD and /CS low to D0 - D7	From /RD ↓ Data >ZZ - >AA	5		65	ns
Twcb	/CARRY or /BORROW low output pulse width (THCT12016 only)			Twud		ns
Twcc	/CARRY or /BORROW low Output pulse width (THCT12016 only)			Tc2		ns
Thdr	Release time, data after /RD./CS	From CS ↑ data >01 - >ZZ	0		45	ns

(***) TYP VALUES @ 25°C, VCC = 5V

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Fig 9 Timing - all Modes

Fig 10 Timing - Modes 1 - 5

Fig 11 Timing - Mode 6 - 7

① AS AN OUTPUT

② Ua2 SHOULD NOT CHANGE WHILE THE CLOCK IS LOW

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Fig 12 READ CYCLE

CLK

SRESET

CS

RD

A0

A1 **

D0–D7

READY *

KLO/KLI (OUT) *

UP or DOWN *

KLO/KLI (IN) *

UP or DOWN *

* THCT12016 ONLY
** THCT12024 ONLY

NOTES

① EITHER OR BOTH MAY GO HIGH
② STATE GENERATING OUTPUT LATCH LOAD PULSE
③ STATE NOT GENERATING OUTPUT LATCH LOAD PULSE
④ AS AN OUTPUT
⑤ AS AN INPUT
⑥ WHICHEVER IS LATER
⑦ WHICHEVER IS EARLIER
⑧ FIRST BYTE (HIGH OR LOW)
⑨ SECOND BYTE (OPPOSITE TO FIRST BYTE)

CASCADED DEVICE

Fig 13   WRITE CYCLE

* THCT12016 ONLY
** THCT12024 ONLY

NOTES

① EITHER OR BOTH MAY GO HIGH
② WHICHEVER IS LATER
③ WHICHEVER IS EARLIER
④ FIRST BYTE (HIGH OR LOW)
⑤ SECOND BYTE (OPPOSITE TO FIRST BYTE)

System Application

The implementation of a three axis control system with the THCT12016,12024 is shown in Fig 14. The microcontroller accesses each channel, memory mapped I/O or I/O addresses with normal read or write cycles. CLK frequencies up to 20Mhz can be sourced directly from the microcontroller. For an external freeze, all /KLI-KLO's can be connected together and driven by the external "freeze-logic". This logic must be designed such that all THCT12016/12024's are programmed into the slave mode before the first read or write cycle appears and must be synchronised with CLK (see Design Checklist).

If the /READY output (THCT12016 only), is used, it must be externally wire-OR'ed (not shown in Fig 14) and fed to the microcontroller READY input. An external zero pulse from the resolver can drive the THCT12024 /Ua0 input.

Fig 14 Block Diagram for a Three-axis Control System
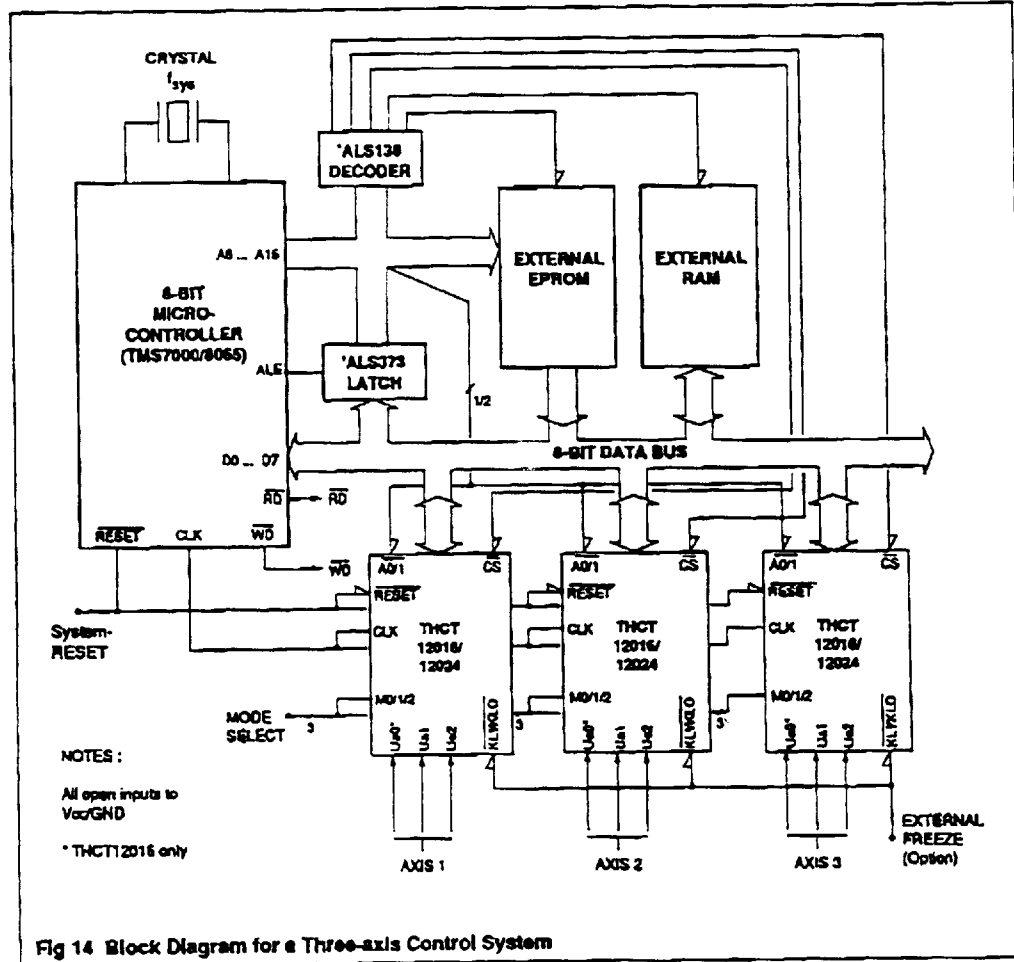
Cascading the THCT12016

Fig 15 shows the cascading of two THCT12016's for 32-bit resolution. The master(LS-word) needs to be programmed to Mode 1 - 5 and the slave(MS-word) to Mode 0(Count only). The /KLI-KLO inputs of both devices are connected together. An external pull-up is not required since it is on-chip. The optional /KLI-KLO signal could be used as an external freeze input. In this case, both both devices operate in the slave mode (see Page 9- cascaded configuration) by generating a /FREEZE low pulse, synchronous with CLK and before the first read or write cycle appears after /RESET.

In normal applications, the THCT12016 receiving the first read/write cycle after initialisation via a /RESET, is programmed into the Master mode. /CARRY and /BORROW of the master THCT12016 are connected to the /UP and /DOWN inputs of the slave. If /READY is used to slow down the microprocessor read/write cycle, both /READY outputs must be OR'ed to generate a common READY signal.
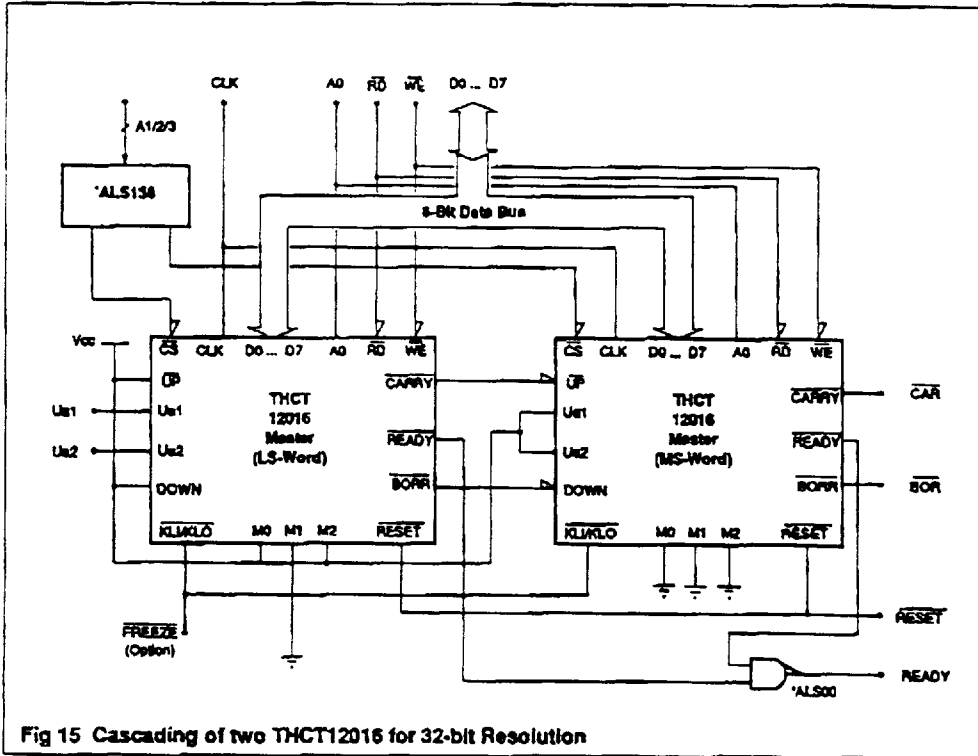

Fig 15 Cascading of two THCT12016 for 32-bit Resolution

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THCT12016,12024
INCREMENTAL ENCODER
INTERFACE

Design Audit Checklist

Before releasing a THCT12016,12024 design to test or production, the following Design Checklist should be worked through to avoid errors and to arrive at a reliable design.

What must be checked ?	What is important ?
timing parameters	
/UPn/DOWNn Fmax ?	- Fmax must not be exceeded. The minimum pulse width is> 25ns (Twud)
What is Fclk ?	Fclk max is 20Mhz and must not be exceeded (50% duty cycle). -In the cascading mode, Fclk needs to be chosen such that the ripple through of /KLI-KLO (THCT12016) is achieved. Fclk should should not exceed 10Mhz.
Is the read/write cycle synchronised with CLK ?	The setup time for /CS,/WE and /RD must be > 15 ns (Tsus) to the negative edge of CLK. The setup time of /A0-/A1 with reference to /RD or /WE must be> 10ns (Tsa,Tsar).
External /KLI-KLO pulse ? If yes, what is the position of /KLI-KLO pulse in relation to CLK and what is the pulse width ?	- The external /KLI-KLO pulse width must be > 20ns (Twk) and not collide with the positive (count) edge of CLK. It is recommended that /KLI-KLO be synchronised with the negative edge of CLK such that Twk = Fclk/4.
Is the read/write cycle long enough ?	- The access time to the first byte is defined by Tdd1 and is < 60ns for the read cycle. The write data must be stable 15ns (Tsda) before the positive going edge of /CS or /WE and be held for 10ns (Thdw).
Are the setup and hold times for Ua1/Ua2 met ?	- The setup time must be > 15ns (Tsab)and the hold time > 12ns (Thab). If these times cannot be met, meta-stable conditions can cause false counting. · If Fclk is > 10Mhz, an external synchchronisation flip flop e.g 'ALS74 or 'AC74 is required.

What must be checked ?	What is important ?

timing parameters - continued

Pulse width and the position of Ua0 ?	If the external zero pulse is used, the pulse width must be > 25ns (TwUa0). To avoid collision with the positive (counting) edge of the clock, which would cause false counting, Ua0 should be synchronised with the negative clock edge.
Is /RESET used ?	- /RESET is required after power-up to set the THCT12016/12024 into a known state. It resets the control logic, the mode bit (master/slave) and the up/down counters.
What is the level of Ua1 and Ua2 during /RESET = low ?	- During RESET = low, Ua1 and Ua2 should be at a high level in Modes 1-5 and at a low in Modes 6-7. If this is not met in Modes 1-5, a count error of +/-1 can occur.
What are the rise and fall times of the input signals ?	- For all signals, Tf/Tr should be < 300ns. For all clock and control inputs Tr/Tf should be < 20ns. This helps to reduce power consumption.

external connections

Unused Inputs ?	- All unused inputs must be tied to either Vcc or GND : - * /UP,/DOWN to Vcc * Ua1,Ua2 to Vcc or GND * M1,M2,M3 to the Vcc/GND according to the mode selected.
Cascaded mode ? (THCT12016 only) * M1,M2,M3 ?	- The MS-word device must always be configured in Mode 0 (M1=M2=M3=Low)
* /CARRY,/BORROW,/UP, /DOWN ?	/CARRYn to /UPn,/BORROWn to /DOWNn from the LS word to the MS-word device.

What must be checked ?	What is important ?
DC parameters	
Is Vcc decoupled with a capacitor ?	- Each THCT12016/1024 device should be decoupled with a 100nF capacitor as close as possible to the Vcc/GND pins.
Capacitive load on the data outputs ?	- Long lines on the data outputs will result in current spikes and line reflections. Capacitive loads should not exceed 50pF.
Over and undershooting due to line reflections ?	- If over and under shooting is greater than -1V or Vcc+1V, a series resistor should be connected in the data lines or any output stage driving THCT12016,12024 inputs e.g. CLK, /WE or /RD. A series resistor should also be included if the capacitive load exceeds 50pF. Special care must be taken if long backplane bus lines are being driven - these are not recommended.

PARAMETER MEASUREMENT INFORMATION

Input/Output Voltage Waveforms

LOAD CIRCUIT

TEST POINT

From output under test

V_{cc}
S1
R_L
C_L
S2

SET UP & HOLD TIMES

Timing Input ... 1.5V ... 3V ... 0V

t_{su} t_h

Data In ... 1.5V ... 1.5V ... 3V ... 0V

PULSE WIDTH

High-level Pulse ... 1.5V ... 1.5V ... 3V ... 0V

t_w

Low-level Pulse ... 1.5V ... 1.5V ... 3V ... 0V

PROPAGATION DELAY TIMES

INPUT ... 50% ... 50% ... V_{OH} ... 0V

t_{PLH} t_{PHL}

IN-PHASE OUTPUT ... 2.2V ... 0.8V ... V_{OH} ... V_{OL}

OUT-OF-PHASE OUTPUT ... 0.8V ... 2.2V ... V_{OH} ... V_{OL}

t_{PHL} t_{PLH}

ENABLE & DISABLE TIMES, 3-STATE OUTPUTS

OUTPUT ENABLE ... 50% ... V_{cc} ... 0V

t_{PZH}

OUTPUT OFF-TO-HIGH ... 2.2V ... V_{OH} ... GND

t_{PZL}

OUTPUT OFF-TO-LOW ... 0.8V ... V_{cc} ... V_{OL}

OUTPUT DISABLE ... 50% ... V_{cc} ... 0V

t_{PHZ}

OUTPUT HIGH-TO-OFF ... 90% ... V_{OH} ... GND

t_{PLZ}

OUTPUT LOW-TO-OFF ... 10% ... V_{cc} ... V_{OL}

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