LX1801

SMBus to Analog & Digital System Interface

PRODUCTION DATA SHEET

DESCRIPTION

The LX1801 is a SMBus controlled dimming interface for CCFL inverters. It complies with the Dell Inc. M07 specification for Notebook backlight inverters.

The LX1801 processes 3 brightness control inputs, one each from the SMBus, an ambient light sensor, and a separate system side PWM signal and generates an analog output signal that drives the dimming circuitry of a CCFL inverter controller. Five different brightness control modes are supported which include Intel DPST display power saving technology.

In addition to its SMBus interface, the LX1801 contains an eight bit ADC, seven 8 bit registers, three 8 bit DAC's, a multiplier, and other special circuits that process its analog voltage output.

The LX1801 controls inverter on/off and monitors and reports lamp status and inverter faults in real time.

The LX1801 is available in the 16 lead 3 x 3mm MLPQ package.

KEY FEATURES

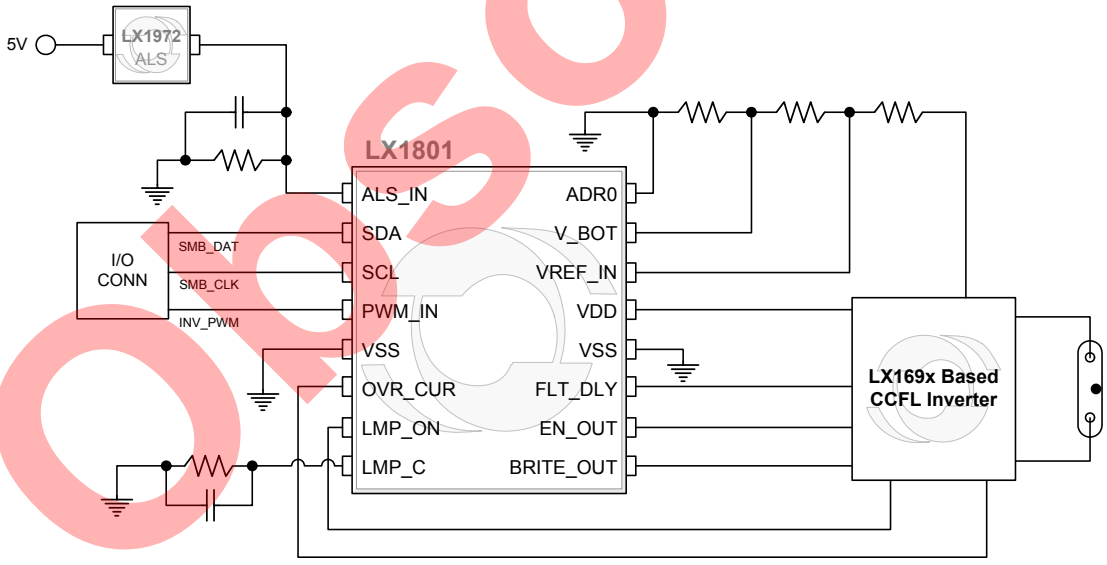
- Fully Compliant to Standard SMBus Specifications
- I2C Bus Compatible
- 8 bit Resolution
- ±10 LSB Accuracy
- One 8 bit ADC
- Three 8 bit DAC's
- SMBus Address Strap for 2 Selectable Addresses
- External Reference Inputs Set Analog Brightness Voltage Lower Limit and Range

APPLICATIONS

- Processor and Ambient Light Senor (ALS) Controlled LCD Panel Dimming with Intel DPST
- General Purpose SMBus I/O Control Applications

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

PRODUCT HIGHLIGHT



Notebook LCD inverter with 5 SMBus dimming modes including bus driven, ambient light sensor driven, PWM driven, and either SMBus or ALS with Intel® DPST enhancement.

PACKAGE ORDER INFO

T_J (°C)	LQ Plastic 3x3 mm MLPQ 16 pin RoHS Compliant / Pb-free
-40 to 85	**LX1801ILQ**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1801ILQ-TR)

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ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage .....-0.3V to 7.0V
Input and Output Pins .....-0.3V to 7.0V
Operating Temperature Range. .....-40 to 85°C
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range.....-65°C to 150°C
Peak Package Solder Reflow Temp (40 seconds max. exposure)..... 260°C(+0,-5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

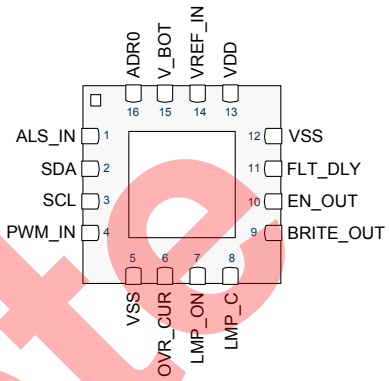
THERMAL DATA

LQ **Plastic 3x3 mm MLPQ 16-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	33.3°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Description
VDD	Power Supply Input: 4.5V to 5.5V
VSS	Ground (2 Pins)
SCL	Digital Input. SMBus Clock – 10 to 100 KHz capable
SDA	Digital I/O. SMBus Data – SMBus Data line
ADR0	SMBus Address strap input – The address for the LX1801 is determined by the state of this pin (see table 1).
ALS_IN	Analog input. Ambient light sensor input. Zero to VREF_IN range.
PWM_IN	A digital input from the system controller whose duty cycle determines lamp brightness when in PWM mode, and multiplies lamp brightness by a fractional value equal to its duty cycle when in DPST mode.
VREF_IN	Analog Input reference voltage for ADC and DAC. Operating range is 1.5 to 3 Vdc. Nominal input is 2.040V. Input impedance is greater than 10MΩ.
V_BOT	An analog voltage input whose value determines the minimum output voltage of BRITE_OUT after the effect of the PWM input when in DPST mode and at all times in other modes.
BRITE_OUT	Analog output voltage that is equal to desired BRITE_OUT voltage after modulation by the PWM input and offset by the voltage at the V_BOT input. An R/C filter at this pin to low pass filters the signal and determines response time when in PWM and DPST modes. In PWM and DPST modes, the output voltage is modulated on and off at the duty cycle and frequency of PWM_IN. The R/C filter is comprised of an internal 100K resistor and an external capacitor to ground.
LMP_C	Lamp Capacitor. A capacitor, typically 10nF and a resistor, typically 1MΩ, are connected in parallel from this pin to ground. They filter a peak voltage detector with the LMP_ON input.
OVR_CUR	Analog / Digital input to comparator and latch. Used for over current status input in M07 application. 1.2V threshold. If OVR_CUR > $1.2V_{DC}$, a "1" is latched and written to bit 0 (FAULT) and bit 2(OV_CURR) of the fault status register (Register 0x02). The latched bits can only be cleared by a write byte command to register 0x01 to make the LAMP_CTL bit true. If bit 0 or bit 2 of register 0x02 is set, this will reset the LAMP_CTL bit in register 0x01, causing the enable output to the CCFL controller (EN_OUT) to go low and turn off the inverter. Zero to VDD input voltage range.
LMP_ON	Digital input. Approximately 1V threshold. When LMP_ON is "1" it charges the capacitor at pin LMP_C to VDD, indicating the lamp is turned on. This pin is normally connected to the A_OUT pin of the LX1692 / 93 controller, and will cause internal circuitry to report the lamp is on if there are pulses on A_OUT. If these pulses stop long enough for the voltage at LMP_C to decrease below 1.2 V, the lamp is reported off at bit 03 of the FLT/STAT register (0x02). . If LAMP_CTL transitions to high, requesting the inverter to turn on, and LMP_C does not go above 1.2V before the FLT_DLY pin reaches 2.5V, an open lamp error signal is produced and is stored, along with other error conditions, to bit zero of the FLT STATUS register 0x02. An Open lamp fault will cause EN_OUT to go low. See FLT_DLY description. Zero to VDD input voltage range
FLT_DLY	Analog / Digital input to the open lamp comparator and latch. This input provides for a time out before LMP_ON is sensed for an open lamp fault. The comparator has a 2.5V threshold. The comparator output is latched when 2.5V is exceeded. The latch is reset at power on and when EN_OUT transitions to high. This pin is normally connected to the C_TO pin of the LX1692 or 1693 CCFL controller.
EN_OUT	Digital Output. Enable output to CCFL controller. TTL voltage and current levels. EN_OUT is made high or low by a write byte command to register 0x01. It is also reset by bit zero of register 0x02 going high.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -40°C ≤ T_A ≤ 85°C except where otherwise noted and the following test conditions: V_{DD} = 5V + 10 / -5%.

Parameter	Symbol	Test Conditions	LX1801 Min	LX1801 Typ	LX1801 Max	Units
POWER SUPPLY						
Operating Supply Voltage	VDD		4.5		5.5	V
Average Supply Current	IDD	DAC = FFH; idle ADC	1.0	2.5	4.0	mA
BRIGHTNESS CONTROL DAC DC PERFORMANCE						
Resolution				8		Bits
Integral Nonlinearity	INL	CODE = 0 to 255, -10nA < IOUT < 10nA	-9		9	LSB
Differential Nonlinearity	DNL	CODE = 0 to 255, -10nA < IOUT < 10nA	-2		5	LSB
Full Scale Output Voltage	FSV	CODE = 255, -10nA < IOUT < 10nA	97% * VREF	VREF	103% * VREF	V
Offset Error		CODE = 0, -10nA < IOUT < 10nA	-3		4	LSB
Gain Error		-10nA < IOUT < 10nA	-4	2	3	% of Ideal
LOW LIMIT CLAMP DAC DC PERFORMANCE						
Resolution				8		Bits
Relative Accuracy (Note 1)		Low Limit DAC CODE = 15 to 205, High Limit DAC CODE ≥ 50 LSB above Low Limit DAC CODE	-10		7	LSB
Offset Error		Low Limit DAC CODE = 0, High Limit DAC CODE ≥ 50 LSB above Low Limit DAC CODE	-1		12	LSB
HIGH LIMIT CLAMP DAC DC PERFORMANCE						
Resolution				8		Bits
Relative Accuracy (Note 2)		High Limit DAC CODE = 50 to 232, Low Limit DAC CODE = 50 LSB below High Limit DAC CODE	-7		7	LSB
ALS MODE ACCURACY						
Output Error at BRITE_OUT		Low Limit DAC CODE = 15 to 205, High Limit DAC Code ≥ 50 LSB above Low Limit DAC CODE, ALS_IN = 20% * VREF to 80% * VREF. VBOT = 0V		3		% of ALS_IN
ADC						
Resolution				8		Bits
Resolvable Input Range			0		VREF	V
Full Scale Output Voltage	FSV		97% * VREF	VREF	103% * VREF	V
Input Leakage Current (ALS_IN)	I_leak	ALS_IN = 0V to VDD	-1		+1	µA
Integral Nonlinearity	INL	Only Major Carry Codes Tested		±3		LSB
Differential Nonlinearity	DNL	Only Major Carry Codes Tested		±1.5		LSB
Offset Error		ALS_IN = 0V	-2	0	2	LSB
Gain Error		ALS_IN = VREF; Read Register. 4	-3	2	3	% of FSR
REF_IN						
Reference Voltage	V_{REF}		1.80	2.040	3.00	V
Input Leakage Current	I_{REF}		-50	0	50	nA
ADR						
High Level Input Voltage	V_{AHL}		80			%VDD
Low Level Input Voltage	V_{ALL}				20	%VDD
Input Leakage Current	I_{ADR}		-50	0	50	nA
SCL, SDA, PWM						
High Level Input Voltage	V_{SHL}		2.1			V
Low Level Input Voltage	V_{SLL}				0.8	V
Input Leakage Current	I_{SMB}		-5	0	1	µA
SDA Low Level Output Voltage	V_{OL}	IOUT = 3mA			0.4	V
SMBUS						
SMB clock frequency	F_{CLK}		10		100	KHz

Note 1: The Relative Accuracy of the Low Limit DAC is specified to be the deviation from the ideal programmed value: Ideal = VREF * (CODE/255). The Relative Accuracy is specified for the range CODE = 15 to 205

Note 2: The Relative Accuracy of the High Limit DAC is specified to be the deviation from the ideal programmed value: Ideal = VREF * (CODE/255). The Relative Accuracy is specified for the range CODE = 50 to 232

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APPLICATION NOTE

The LX1801 is a seven register device that uses SMBus commands to communicate with the host system. All registers are defined as full byte wide with reserved (undefined) bits containing a default value of "0". Four of the seven registers are read / write, and three are read only with respect to the SMBus.

SMB PROTOCOL

Only standard SMBus protocol, version 2.0 or higher, may be used for this device. The only required commands are the SMBus Read Byte and the SMBus Write Byte protocols. There are to be no non standard protocols implemented. Further, register contents shall not be altered by invalid commands.

General Rules for Writing and Reading LX1801 Registers with the SMBus.

Writes to registers can be performed by either the SMBus Write Byte protocol and / or by internal IC logic, depending on the register type (see table 1).

Reads can be performed on all seven registers by issuing the Read_Byte protocol.

Read Only registers can be written only by internal logic. Their contents can not be affected by SMBus write commands.

Specific Requirements for SMBus Protocols:

- The IC shall implement the SMBus Read Byte protocol.
- The IC shall implement the SMBus Write Byte protocol.
- The IC shall not require the use of any other SMBus protocol to meet the requirements contained in the Dell M07 specification.
- The IC shall operate correctly when the SMBus master clock operates at a frequency of 55KHz and over the complete frequency range of 10KHz to 100KHz.
- The IC shall not employ clock stretching.
- The IC shall not include SMBus pull up resistors. These are provided by the host system.

Read Byte Protocol:

S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	Ā	P
1	7	1	1	8	1	1	7	1	1	8	1	1

Write Byte Protocol:

S	Slave Address	Wr	A	Command Code	A	Data Byte	Ā	P
1	7	1	1	8	1	8	1	1

Grey shading represents cycles during which the LX1801 "owns" or "drives" the Data line. All other cycles are driven by the host.

Definitions

S: Start condition
Wr: Write
Rd: Read
A: Acknowledge
P: Stop Condition

Protocol must be per standard SMB specification version 2.0 or higher.

APPLICATION NOTE

SMBus De-featuring

Packet Error Correction (PEC) and the Alarm function are not supported.

DEVICE ADDRESS:

In this document the device address is always expressed as a full 8 bit address. The high nibble of the address is always 5H. In the low nibble bit 0 is always the R/W bit, and bits 3-1 are A2, A1, and A0. This device implements one address strap at A0. When this strap is grounded the resulting device address is 58(H); when pulled to 5V, the resulting device address is 5A(H). The state of the A0 strap is sensed at Power on reset. The pin will not change state when the system is in operation.

REGISTER DEFINITIONS:

DESCRIPTION	ADDR	TYPE	BIT DEFINITIONS							
			7	6	5	4	3	2	1	0
BRIGHTNESS CONTROL	0x00	R/W	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
DEVICE CONTROL	0x01	R/W	RESRVD	RESRVD	ALS DLY1 (OPTION)	ALS DLY0 (OPTION)	ALS_CTL	PWM_MD	PWM_SEL	LMP_CTL
FAULT / STATUS	0x02	R/O	RESRVD	RESRVD	RESRVD	RESRVD	LMP_ST 1= LAMP IS ON	OV_CUR 1= OVER CURENT	THR_SD 1= OVER TEMP	FAULT 1= ANY FAULT
IDENTIFICATION	0x03	R/O	MFG4	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
ALS STATUS	0x04	R/O	ALS7	ALS6	ALS5	ALS4	ALS3	ALS2	ALS1	ALS0
ALS LOW LIMIT	0x05	R/W	ALSLL7	ALSLL6	ALSLL5	ALSLL4	ALSLL3	ALSLL2	ALSLL1	ALSLL0
ALS HIGH LIMIT	0x06	R/W	ALSHL7	ALSHL6	ALSHL5	ALSHL4	ALSHL3	ALSHL2	ALSHL1	ALSHL0

Specific requirements for Register 0:

1. A Write Byte cycle shall set the brightness level if the IC is in SMBus mode as selected by bits 3-1 of the Device control register.
2. A Write Byte cycle shall have no effect on the BRITE_OUT pin when the IC is not in the SMBus mode.
3. A Read Byte cycle shall return the current brightness level regardless of the value of PWM_SEL.
4. When in SMBus or SMBus + DPST mode, register 0x00 must reflect *exactly the last value written to it via the SMBus, not a digitized version of the analog brightness control output voltage.* If DPST is active a read to register 0x00 shall not include its affect.
5. When the PWM or ALS or ALS+DPST mode is set, register 0x00 reads will return the digitized DC brightness control voltage exclusive of any offset produced from the V_BOT input. Range of the read voltage is from zero to VREF_IN.
6. A value of 0xFF shall set the BRITE_OUT level to maximum brightness.
7. A value of 0x00 shall set the BRITE_OUT level to minimum brightness.
8. The default value shall be 0xFF.

Specific requirements for Register 4:

1. Register 0x04 reads always produce the digitized raw ALS_IN voltage, independent of what mode has been set. This data will not include the effect of DPST if DPST is active, or the effect of the high and low limit registers.

LX1801 COMMANDS

W/R	Register	Description
W	0x00	Write an 8 bit data byte to the Brightness Control register.
R	0x00	Read the 8 bit data byte stored in the Brightness Control register.
W	0x01	Write an 8 bit control byte to the Device Control Register. See the M07 specification for command details.
R	0x01	Read the 8 bit control byte from the Device Control Register. See the M07 specification for command details.
W	0x02	Write the 8 bit Fault / Status Register. This register shall ignore write operations. It is read only.
R	0x02	Read the 8 bit Fault / Status Register. See the M07 specification for command details.
W	0x03	Write the 8 bit Identification Register. This register shall ignore write operations. It is read only.
R	0x03	Read the 8 bit Identification Register. See the M07 specification for command details.
W	0x04	Write the 8 bit ALS Status Register. This register shall ignore write operations. It is read only.
R	0x04	Read the 8 bit ALS Status Register. See the M07 specification for command details.
W	0x05	Write the 8 bit ALS Low Limit Register. See the M07 specification for command details.
R	0x05	Read the 8 bit ALS Low Limit Register. See the M07 specification for command details.
W	0x06	Write the 8 bit ALS High Limit Register. See the M07 specification for command details.
R	0x06	Read the 8 bit ALS High Limit Register. See the M07 specification for command details.

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FUNCTIONAL BLOCK DIAGRAM

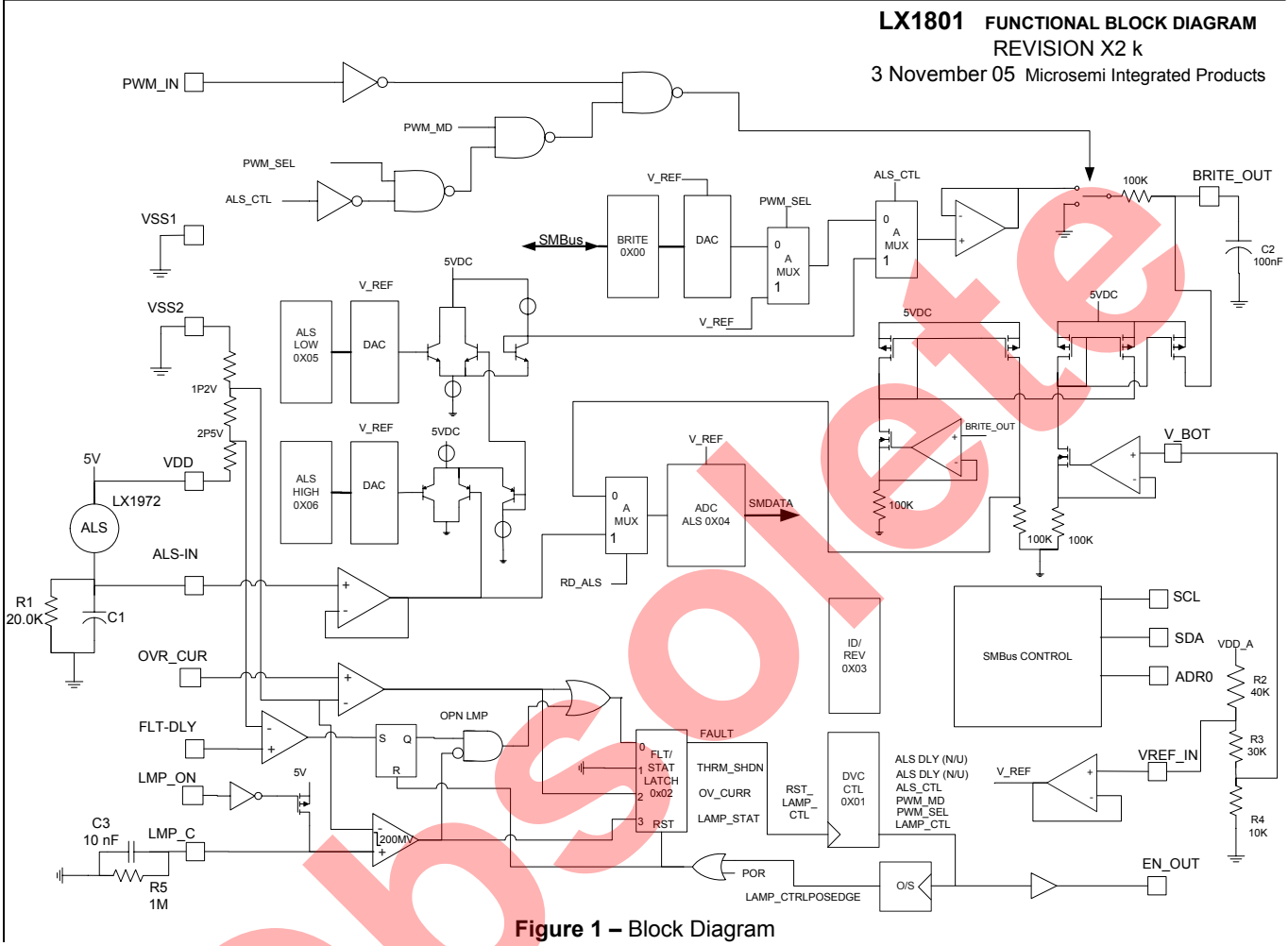

Figure 1 – Block Diagram

APPLICATION CIRCUITS

LX1692 WIDE INPUT VOLTAGE RANGE NOTEBOOK INVERTER
with ALS & INTEL DPST FOR DELL M07 Inverters
LX1801 Application Schematic With LX1962 REV 4NOV05.VSD

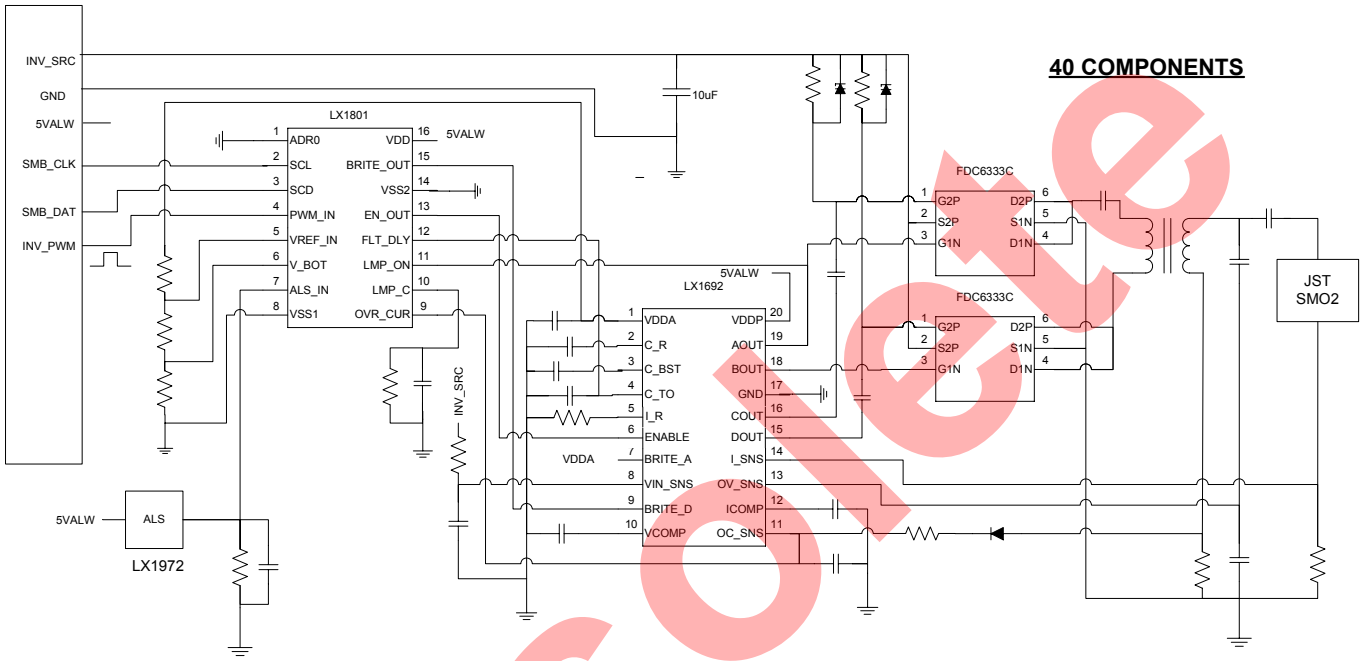

Figure 2 – Typical Application

THEORY OF OPERATION

BASIC FUNCTIONALITY

The LX1801 contains three 8 bit DAC's, an 8 bit ADC and a SMBus interface with 7 addressable registers to control 5 dimming modes for a notebook backlight inverter. The ADC contains a track and hold input that stores the analog voltage level while the conversion is being processed. Several special circuits are also present in the LX1801. Analog comparators and a 2 bit R/S register detect and latch inverter fault conditions. Another analog comparator monitors real time on / off status of the CCFL lamp and writes it, along with inverter fault status to a host readable register.

An analog multiplier provides the ability for implementing Intel™ DPST (Display Power Savings Technology), and voltage limiting clamps on the ALS input provide SMBus programmable range limiting of the ambient light sensor output signal.

SMBUS INTERFACE

The LX1801 communicates over the SMBus in the slow speed Low Power Level and operates in a "slave" mode receiving commands and sending and receiving data from the host or bus "master". The LX1801 can be configured for one of two addresses by connecting the ADR0 input to 5V or ground. Addresses 0x58 and 0x5A can be selected with the strapping code below:

Table 1. Address strapping codes

Option #	ADR 0	Hex Address
1	0V	:058
2	5V	:05A

APPLICATION NOTE

LAYOUT GUIDELINES

The LX1801 is sensitive to noise at the analog input pins so these nodes should be a low impedance path to ground for high frequency noise. As a precaution, the BRITE_OUT and ALS _IN pins should be routed away from digital switching traces and have ceramic capacitors located close to the package pins. The VDD Pin should be decoupled to ground with a 0.1uF ceramic capacitor located as close as possible to the IC.

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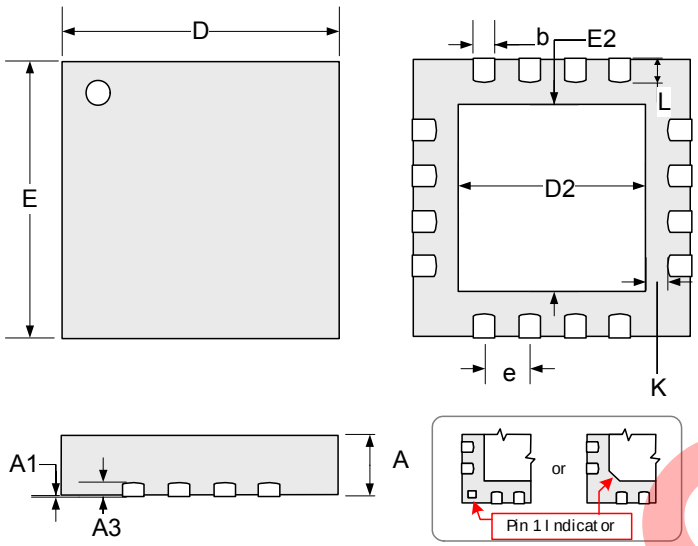
PACKAGE DIMENSIONS

LQ 16-Pin MLPQ 3x3



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.00 BSC		0.118 BSC	
E	3.00 BSC		0.118 BSC	
e	0.50 BSC		0.020 BSC	
D2	1.30	1.55	0.051	0.061
E2	1.30	1.55	0.051	0.061
K	0.2	-	0.008	-
L	0.35	0.50	0.012	0.020
L1	-	0.15	-	0.006

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.
2. Due to multiple qualified assembly sub-contractors either package (with different pin one indicators) may be shipped. Package type will be consistent within the smallest individual container.

NOTES