



## DESCRIPTION

The A7111 is a constant frequency, 1.5MHz, slope compensated current mode PWM stepdown converter working under an input voltage range of 2.5V to 5.5V. This feature makes the A7111 suitable for single cell Liion battery-powered applications.

The internal synchronous rectifier is desired to increase efficiency without an external Schottky diode. 100% duty cycle capability extends battery life in portable devices, while the quiescent current is 200µA at no load, and drops to < 1µA in shutdown. Pulse Skipping Mode operation increases efficiency at light loads, further extending battery life.

The A7111 is offered in a low profile (1mm) 5-pin, thin SOT-23 package, and is available in an adjustable version and fixed output versions of 1.0V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

The A7111 is available in SOT-25 and DFN6(2x2) Package.

## ORDER INFORMATION

| Package Type  | Part Number   |              |
|---|---|--------------|
| SOT-25  | E5  | A7111E5R-XX  |
|   |   | A7111E5VR-XX |
| DFN6<br>(2x2)   | J6  | A7111J6R-XX  |
|   |   | A7111J6VR-XX |
| Note  | XX: Output Voltage<br>33=3.3V,ADJ=Adjustable<br>R: Tape & Reel<br>V: Halogen free Package |              |
| AiT provides all RoHS products<br>Suffix "V" means Halogen free Package |   |              |

## FEATURES

- High Efficiency: Up to 96%
- 1.5MHz Constant Switching Frequency
- Current Mode Operation for Excellent Line and Load Transient Response
- No Schottky Diode Required
- 2.5V to 5.5V Input Voltage Range
- 1.0V,1.2V,1.5V,1.8V,2.5V and 3.3V Fixed/Adjustable Output Voltage
- 100% Duty Cycle in Dropout Mode
- Low Quiescent Current: 200µA
- Over temperature Protection
- Short Circuit Protection
- Shutdown Quiescent Current < 1µA
- Available in SOT-25 and DFN6(2x2) package

## APPLICATION

- Cellular and Smart Phones
- Wireless Handsets and DSL Modems
- Microprocessors and DSP Core Supplies
- PDAs
- Digital Still and Video Cameras
- MP3/MP4/MP5 Players
- Portable Instruments
- GPS Receivers

## TYPICAL APPLICATION CIRCUIT

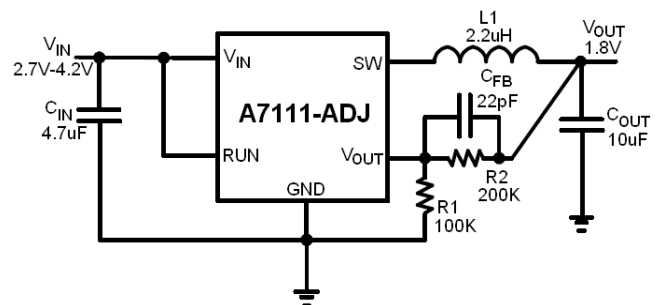
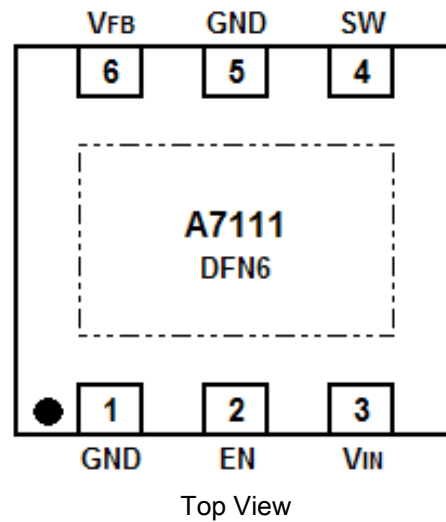
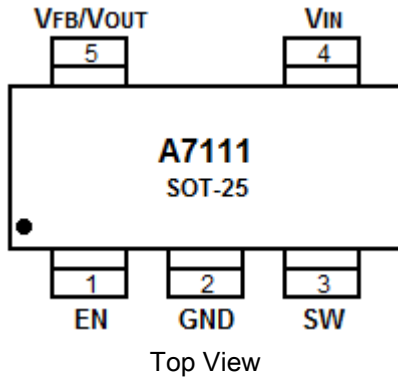


Figure 1. A7111-ADJ Typical Application Circuit



**PIN DESCRIPTION**



| Pin #  |      | Symbol                            | Function   |
|--------|------|-----------------------------------|--|
| SOT-23 | DFN6 |                                   |  |
| 1      | 2    | EN                                | Regulator Enable Control Input. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. In shutdown, all functions are disabled drawing <1KA supply current. Do not leave EN floating.  |
| 2      | 1, 5 | GND                               | Ground   |
| 3      | 4    | SW                                | Power Switch Output. It is the Switch node connection to external Inductor. This pin connects to the drains of the internal P-CH and N-CH MOSFET switches.   |
| 4      | 3    | V <sub>IN</sub>                   | Supply Input Pin. Must be closely decoupled to GND, Pin 2, with a 2.2μF or greater ceramic capacitor.  |
| 5      | 6    | V <sub>FB</sub> /V <sub>OUT</sub> | V <sub>FB</sub> (ADJ): Feedback Input Pin. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.<br>V <sub>OUT</sub> (Fixed): Output Voltage Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage. |



## ABSOLUTE MAXIMUM RATINGS

|                                      |                                  |
|--------------------------------------|----------------------------------|
| Input Supply Voltage                 | -0.3V to +6V                     |
| EN, V <sub>FB</sub> Voltages         | -0.3V to +V <sub>IN</sub>        |
| SW Voltages                          | -0.3V to (V <sub>IN</sub> +0.3V) |
| P-Channel Switch Source Current (DC) | 1.1A                             |
| N-Channel Switch Sink Current (DC)   | 1.1A                             |
| Peak SW Sink and Source Current      | 1.5A                             |
| Operating Temperature Range          | -40°C to +85°C                   |
| Junction Temperature <sup>NOTE</sup> | +125°C                           |
| Storage Temperature Range            | -65°C to +150°C                  |
| Lead Temperature (Soldering, 10s)    | +300°C                           |

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE: T<sub>J</sub> is calculated from the ambient temperature T<sub>A</sub> and power dissipation P<sub>D</sub> according to the following formula:

$$T_J = T_A + (P_D) \times (220^\circ\text{C/W})$$

## THERMAL RESISTANCE

| Package | θ <sub>JA</sub> | θ <sub>Jc</sub> |
|---------|-----------------|-----------------|
| SOT-25  | 250°C/W         | 130°C/W         |
| DFN6    | 165°C/W         | 20°C/W          |

NOTE: Thermal Resistance is specified with approximately 1 square of 1 oz copper



## ELECTRICAL CHARACTERISTICS

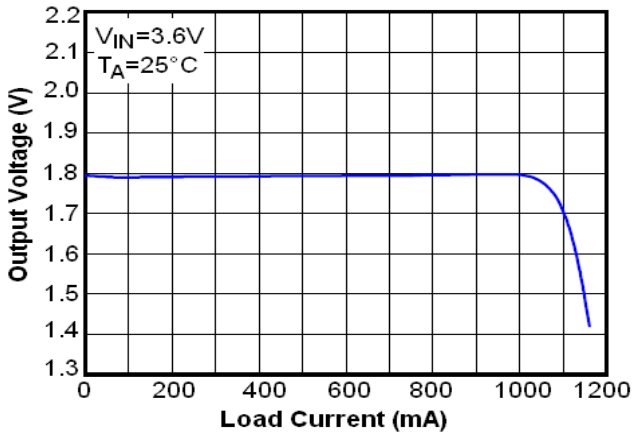
$V_{IN} = V_{EN} = 3.6V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

| Parameter                         | Conditions   | MIN    | TYP        | MAX      | unit     |
|-----------------------------------|--|--------|------------|----------|----------|
| Input Voltage Range               |  | 2.5    | -          | 5.5      | V        |
| Input DC Supply Current           |  |        |            |          |          |
| Active Mode                       | $V_{FB} = 0.5V$ or $V_{OUT} = 90\%$  | -      | 200        | 300      | $\mu A$  |
| Shutdown Mode                     | $V_{FB} = 0V$ , $V_{IN} = 4.2V$  | -      | 0.1        | 1.0      | $\mu A$  |
| Regulated Feedback Voltage        | $T_A = +25^\circ C$  | 0.5880 | 0.6000     | 0.6120   | V        |
|                                   | $T_A = 0^\circ C \leq T_A \leq 85^\circ C$                                 | 0.5865 | 0.6000     | 0.6135   | V        |
|                                   | $T_A = -40^\circ C \leq T_A \leq 85^\circ C$                               | 0.5850 | 0.6000     | 0.6150   | V        |
| $V_{FB}$ Input Bias Current       | $V_{FB} = 0.65V$   | -      | -          | $\pm 30$ | nA       |
| Reference Voltage Line Regulation | $V_{IN} = 2.5V$ to $5.5V$  | -      | 0.04       | 0.4      | %/V      |
| Regulated Output Voltage          | 12V   $-40^\circ C \leq T_A \leq 85^\circ C$                               | 1.164  | 1.200      | 1.236    | V        |
|                                   | 18V   $-40^\circ C \leq T_A \leq 85^\circ C$                               | 1.746  | 1.800      | 1.854    | V        |
| Output Overvoltage Lockout        | $\Delta V_{OVL} = V_{OVL} - V_{FB}$ , Adjustable Version                   | 20     | 50         | 80       | mV       |
|                                   | $\Delta V_{OVL} = V_{OVL} - V_{OUT}$ , Fixed Version                       | 2.5    | 7.8        | 13       | %        |
| Output Voltage Line Regulation    | $V_{IN} = 2.5V$ to $5.5V$  | -      | 0.04       | 0.40     | %        |
| Output Voltage Load Regulation    |  | -      | 0.5        | -        | %        |
| Peak Inductor Current             | $V_{IN} = 3V$ , $V_{FB} = 0.5V$ or $V_{OUT} = 90\%$<br>Duty Cycle $< 35\%$ | -      | 1.3        | -        | A        |
| Oscillator Frequency              | $V_{FB} = 0.6V$ or $V_{OUT} = 100\%$                                       | 1.2    | 1.5        | 1.8      | MHz      |
| $R_{DS(ON)}$ of P-CH MOSFET       | $I_{SW} = 300mA$   | -      | 0.40       | 0.50     | $\Omega$ |
| $R_{DS(ON)}$ of N-CH MOSFET       | $I_{SW} = -300mA$  | -      | 0.35       | 0.45     | $\Omega$ |
| SW Leakage                        | $V_{EN} = 0V$ , $V_{SW} = 0V$ or $5V$ , $V_{IN} = 5V$                      | -      | $\pm 0.01$ | $\pm 1$  | $\mu A$  |
| EN Threshold                      | $-40^\circ C \leq T_A \leq 85^\circ C$                                     | 0.3    | 1.1        | 1.30     | V        |
| EN Leakage Current                |  | -      | $\pm 0.01$ | $\pm 1$  | $\mu A$  |

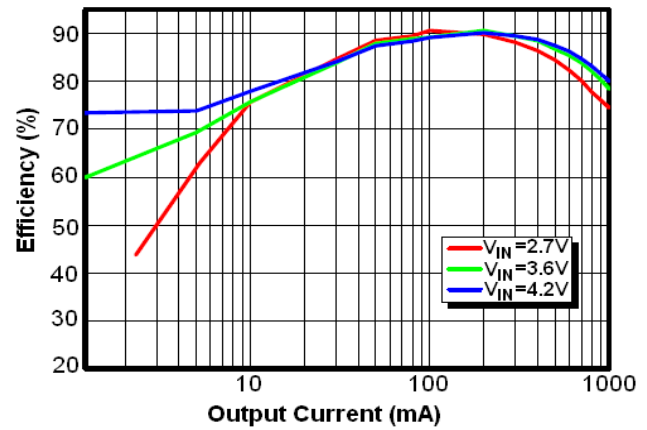


## TYPICAL PERFORMANCE CHARACTERISTICS

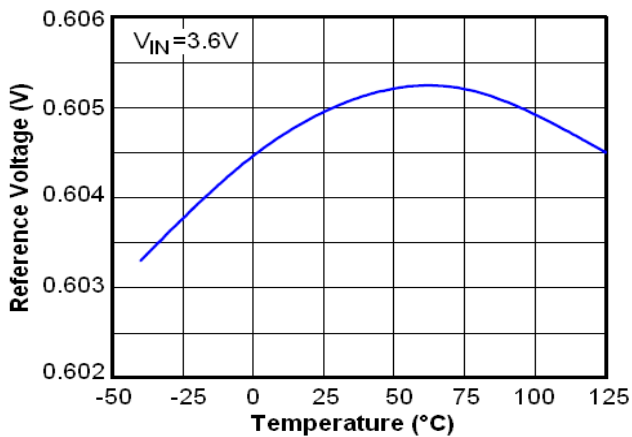
1. Output Voltage vs Load Current



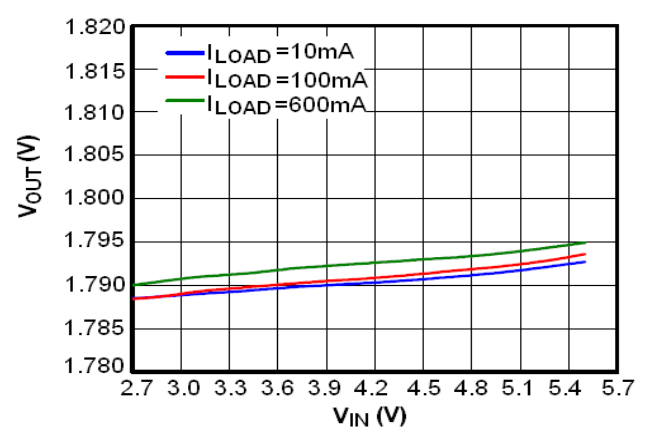
2. Efficiency vs Output Current



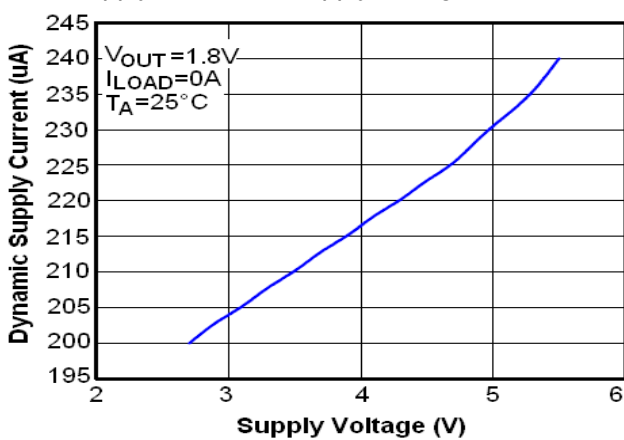
3. Reference Voltage vs Temperature



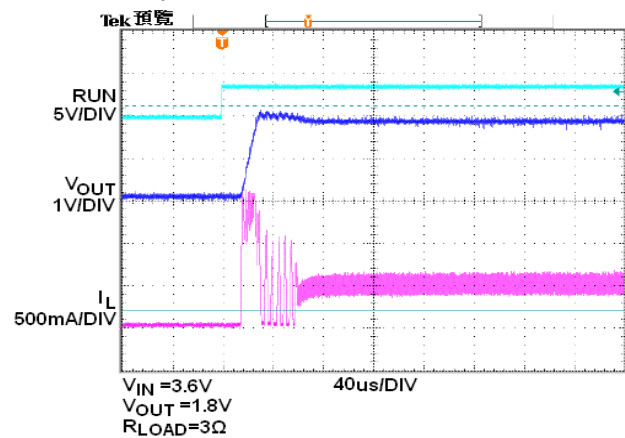
4. Output Voltage vs Input Voltage



5. Supply Current vs Supply Voltage

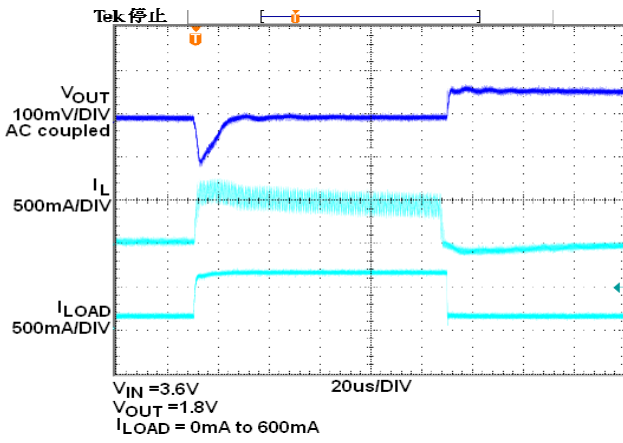


6. Start-up from Shutdown

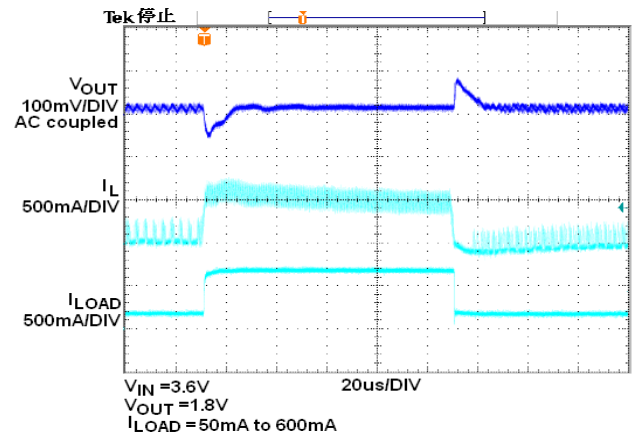




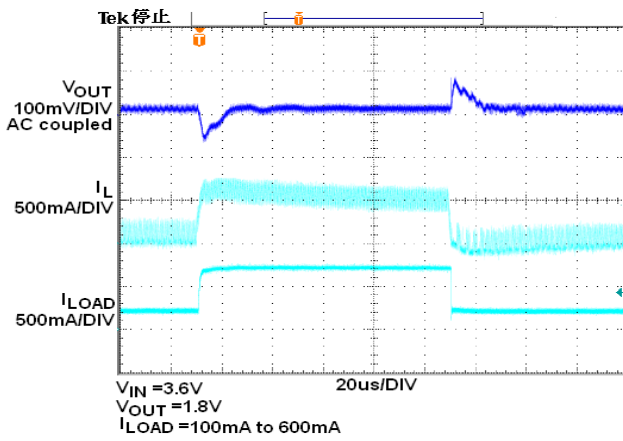
7. Load Step



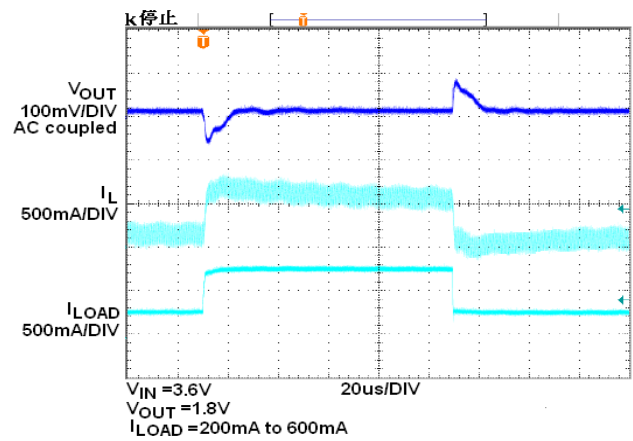
8. Load Step



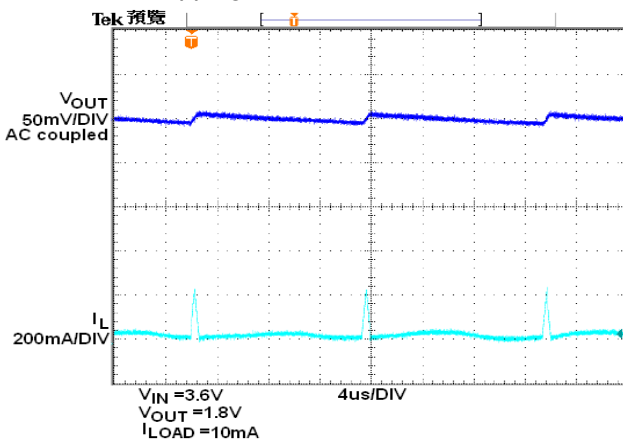
9. Load Step



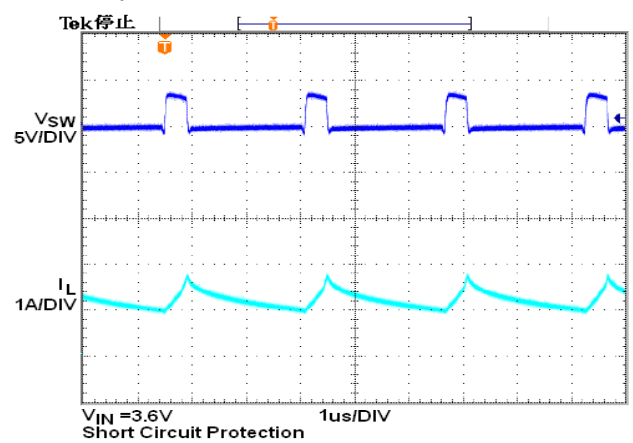
10. Load Step



11. Pulse Skipping Mode

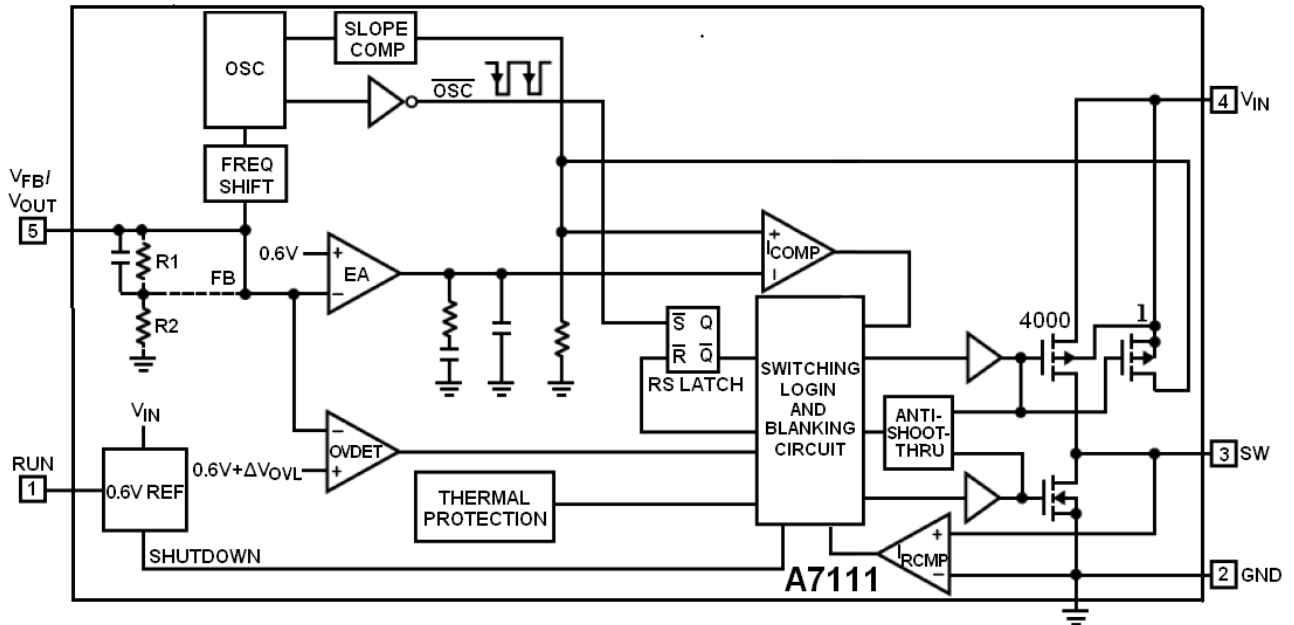


12. Output Short





**BLOCK DIAGRAM**





## DETAILED INFORMATION

### Operation

The A7111 uses a constant frequency, current mode step-down architecture. Both the main switch (P-channel MOSFET) and the synchronous rectifier (N-channel MOSFET) are integrated internally. This Step-Down DC-DC Converter can supply 600mA output current over a wide input voltage range from 2.5V to 5.5V. The over voltage comparator OVDET guards against transient overshoots >7.8% by turning the main switch off and keeping it off until the fault is removed.

### Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle by- cycle current limit for excellent load and line responses. During normal operation, the internal main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and turned off when the peak inductor current reaches the controlled value. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I<sub>RCMP</sub>, or the beginning of the next clock cycle.

### Pulse Skipping Mode Operation

At very light loads, the A7111 will automatically enter Pulse Skipping Mode to increase efficiency, further extending battery life. In this mode, the control loop skips PWM pulses while maintaining output in regulation, and the switching frequency depends on the load condition. This is a kind of PFM mode operation.

### Dropout Operation

When the input voltage decreases toward the value of the output voltage, the A7111 will keep the main switch on for more than one switching cycle and increases the duty cycle <sup>NOTE5</sup> until it reaches 100%. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the R<sub>DS(ON)</sub> of the P-Channel MOSFET increases, and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated not to exceed the maximum junction temperature of the IC.

NOTE5: The duty cycle D of a step-down converter is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

where T<sub>ON</sub> is the main switch on time, and f<sub>OSC</sub> is the oscillator frequency (1.5MHz).





### Short Circuit Protection

The A7111 has short circuit protection. When output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

### Maximum Load Current

The A7111 will operate with input supply voltage as low as 2.5V, however the maximum load current decreases at lower input voltage due to large IR drop on the main switch and synchronous rectifier.

### Application Information

Figure 2 below shows the basic application circuit with A7111 fixed output versions.

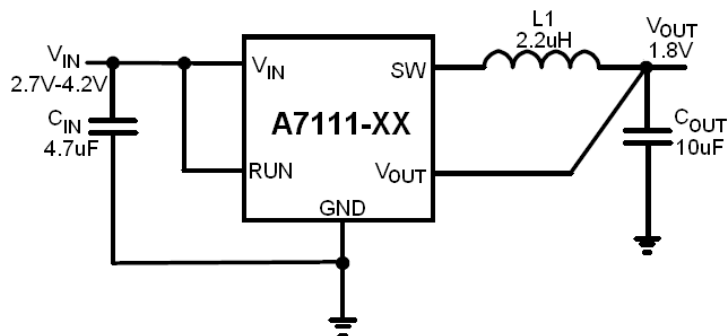


Figure 2. Basic Application Circuit with fixed output versions

### Setting the Output Voltage

Figure 1 of page #1 shows the basic application circuit with A7111 adjustable output version. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R2}{R1}\right)$$

Table 1-Resistor Selection vs Output Voltage Setting

| V <sub>OUT</sub> | R1  | R2  |
|------------------|-----|-----|
| 1.0V             | 180 | 120 |
| 1.2V             | 180 | 180 |
| 1.5V             | 180 | 270 |
| 1.8V             | 180 | 360 |
| 2.5V             | 158 | 499 |
| 3.3V             | 180 | 810 |



### Inductor Selection

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. In continuous mode, the ripple current is determined by:

$$\Delta I_L = \frac{1}{f \times L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A reasonable starting point for setting ripple current is  $\Delta I_L = 240\text{mA}$  (40% of 600mA). For output voltages above 2.0V, when efficiency at light load condition is important, the minimum recommended inductor is 2.2 $\mu\text{H}$ . For optimum voltage-positioning load transients, choose an inductor with DC series resistance below 150m $\Omega$ . For higher efficiency at heavy loads (above 200mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100m $\Omega$ . The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA+120mA).

### Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. In continuous mode, the source current of the main switch is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{0.5}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current.

### Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current. The output ripple  $\Delta V_{OUT}$  is determined by:



$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left( ESR + \frac{1}{8 \times f_{OSC} \times C_2} \right)$$

### Efficiency Considerations

### Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the A7111. These items are also illustrated graphically in Figures 5 and 6. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the  $V_{IN}$  trace should be kept short, direct and wide.
2. Does the  $V_{FB}$  pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of  $C_{OUT}$  and ground.
3. Does the (+) plate of  $C_{IN}$  connect to  $V_{IN}$  as closely as possible? This capacitor provides the AC current to the internal power MOSFETS.
4. Keep the switching node, SW, away from the sensitive  $V_{FB}$  node.
5. Keep the (-) plates of  $C_{IN}$  and  $C_{OUT}$  as close as possible.

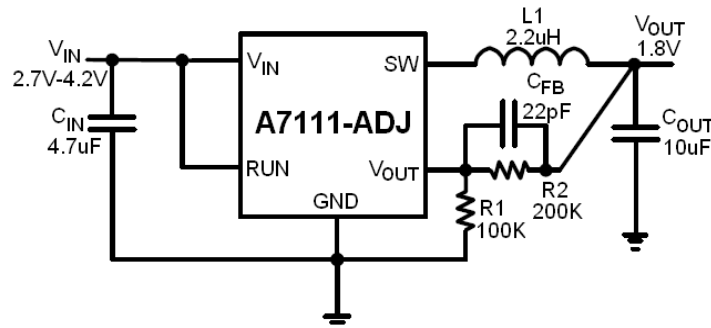


Figure 3. A7111-ADJ Layout Circuit

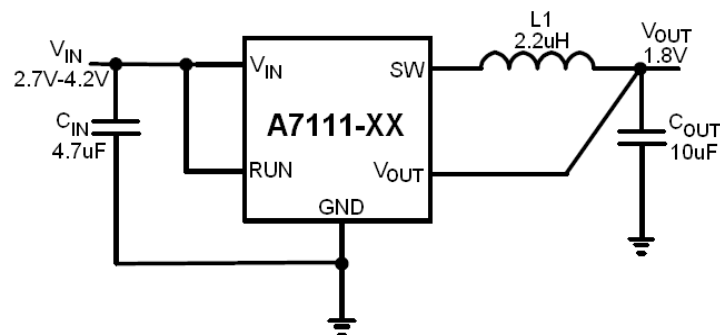


Figure 4. A7111-1.8 Layout Circuit

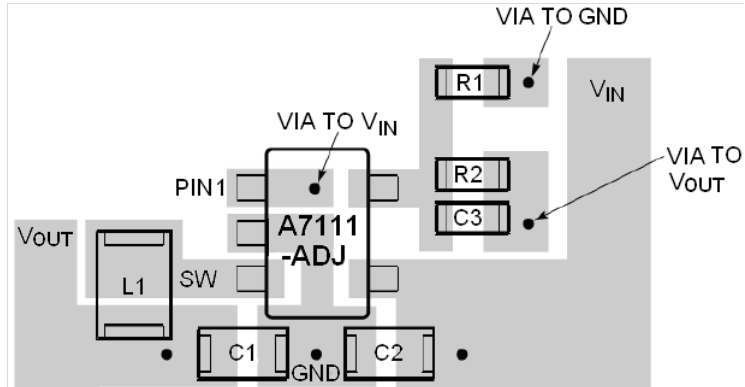


Figure 5. A7111-ADJ Suggested Layout

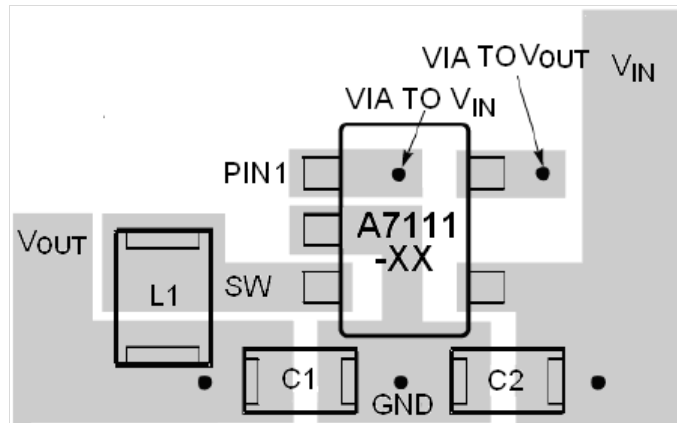
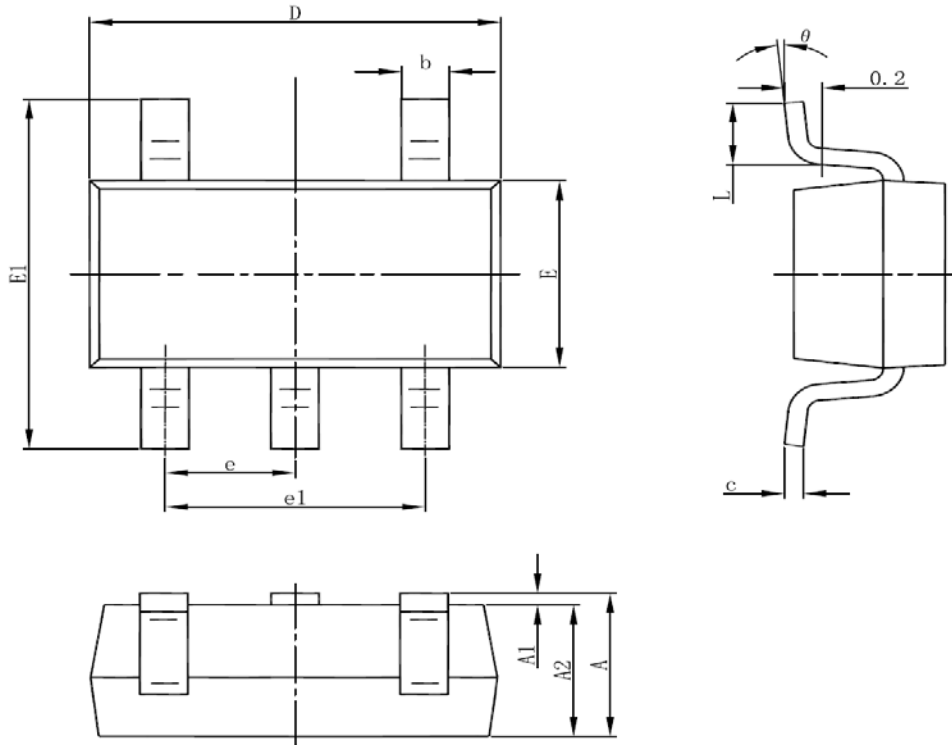


Figure 6. A7111-XX (Fixed) Suggested Layout



**PACKAGE INFORMATION**

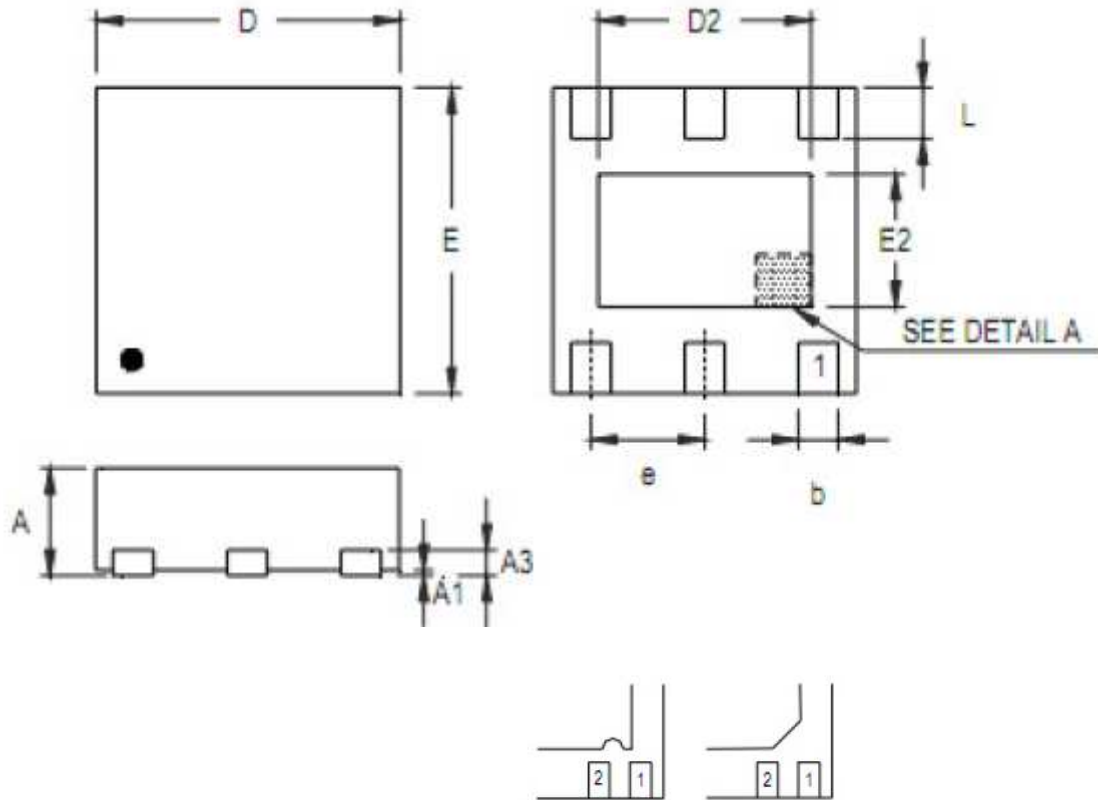
Dimension in SOT-25 (Unit: mm)



| Symbol   | Min        | Max   |
|----------|------------|-------|
| A        | 1.050      | 1.250 |
| A1       | 0.000      | 0.100 |
| A2       | 1.050      | 1.150 |
| b        | 0.300      | 0.500 |
| c        | 0.100      | 0.200 |
| D        | 2.820      | 3.020 |
| E        | 1.500      | 1.700 |
| E1       | 2.650      | 2.950 |
| e        | 0.950(BSC) |       |
| e1       | 1.800      | 2.000 |
| L        | 0.300      | 0.600 |
| $\theta$ | 0°         | 8°    |



Dimension in DFN6(2x2) Package (Unit: mm)



**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Min       | Max   |
|--------|-----------|-------|
| A      | 0.700     | 0.800 |
| A1     | 0.000     | 0.050 |
| A3     | 0.175     | 0.250 |
| b      | 0.200     | 0.350 |
| D      | 1.950     | 2.050 |
| D2     | 1.000     | 1.450 |
| E      | 1.950     | 2.050 |
| E2     | 0.500     | 0.850 |
| e      | 0.650TYP. |       |
| L      | 0.300     | 0.400 |



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