ADS125H0x Wide-Input Range, 2-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Voltage Reference

1 Features

- Precision, Wide-Input Range, 24-Bit ΔΣ ADC
- Differential Input Voltage Range: ±7 mV to ±20 V
- Absolute Input Voltage Range: ±15.5 V
- High Impedance PGA: 1 GΩ
- PGA Gain: 0.125 to 128
- High Accuracy:
  - Offset Drift: 5 nV/°C
  - Gain Drift: 1 ppm/°C
  - Linearity: 2 ppm
- Data Rate: 2.5 to 40000 SPS
- 2.5-V Reference
- Simultaneous 50-Hz and 60-Hz Rejection Mode
- Single-Cycle Settling Mode
- Signal and Reference Voltage Monitors
- Cyclic Redundancy Check (CRC)
- Two Reference Inputs (H02)
- Sensor Excitation Current Sources (H02)
- Four General-Purpose Inputs/Outputs (H02)
- 5-mm × 5-mm VQFN Package

2 Applications

- Wide Common-Mode Voltage Measurements
- ±10-V Analog Input PLC Modules
- Test and Measurement Equipment
- Lab Instrumentation

3 Description

The ADS125H01 and ADS125H02 (ADS125H0x) are 2-channel, 24-bit, 40-kSPS, delta-sigma (ΔΣ) ADCs with an integrated ±18-V programmable gain amplifier (PGA). The devices also include a voltage reference and features to enhance data reliability such as CRC and signal monitors. The ADCs provide a complete, high-resolution measurement solution over a wide range of common-mode voltage, with differential input voltage ranges from ±7 mV to ±20 V.

The ADCs are comprised of an ±18-V PGA providing gain of 0.125 to 128, a 24-bit ΔΣ modulator, programmable digital filter, and an internal reference.

The PGA inputs are high-impedance (1 GΩ) and accommodate high common-mode voltages with no external attenuation required. The devices support 1 differential or 2 single-ended inputs.

The flexible digital filter is programmable for single-cycle settled conversions while providing simultaneous 50-Hz and 60-Hz line cycle rejection.

Signal and reference monitors, a temperature sensor, and CRC data verification enhance data reliability.

The ADS125H01 and ADS125H02 are pin compatible. The devices are available in a 5-mm × 5-mm VQFN package and are specified over the –40°C to +125°C temperature range.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS125H0x	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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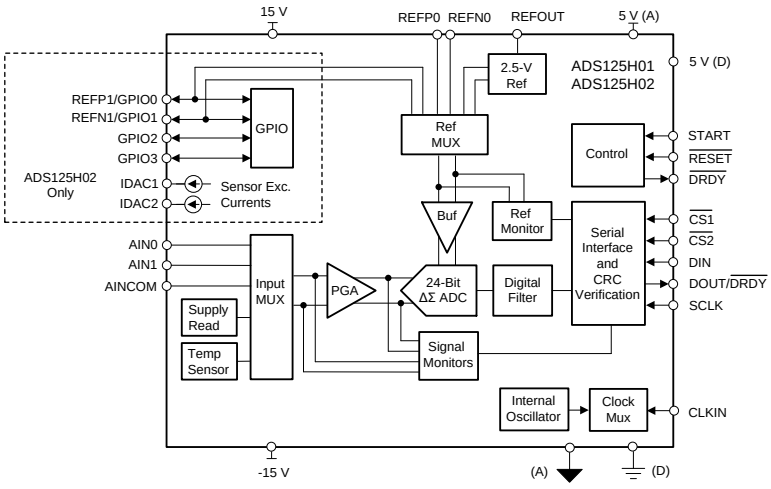
Functional Block Diagram



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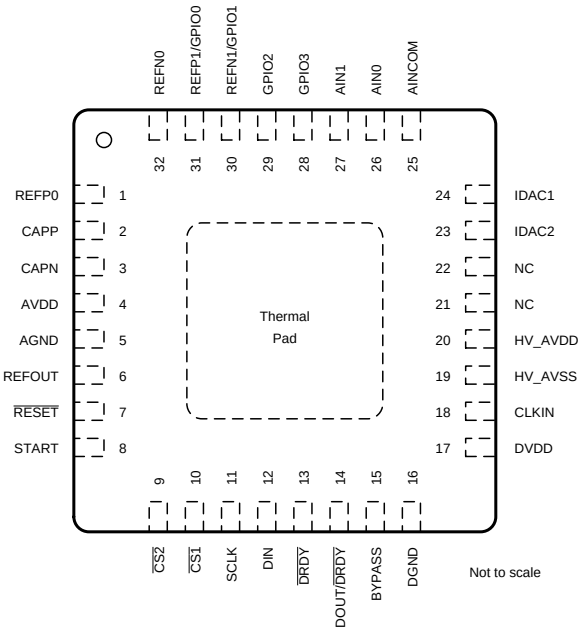
4 Revision History

DATE	REVISION	NOTES
October 2018	*	*

5 Pin Configuration and Functions

RHB Package: ADS125H02
32-Pin VQFN
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NO.	ADS125H01	ADS125H02		
1	REFP0	REFP0	Analog input	Reference input 0 positive
2	CAPP	CAPP	Analog output	PGA output P; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
3	CAPN	CAPN	Analog output	PGA output N; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
4	AVDD	AVDD	Analog	Low-voltage analog power supply (5 V)
5	AGND	AGND	Analog	Analog ground. Connect to ADC ground plane
6	REFOUT	REFOUT	Analog output	2.5-V reference output; connect a 10-µF capacitor to AGND
7	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Digital input	Reset; active low
8	START	START	Digital input	Conversion start, active high
9	$\overline{\text{CS2}}$	$\overline{\text{CS2}}$	Digital input	Serial interface chip select 2; active low
10	$\overline{\text{CS1}}$	$\overline{\text{CS1}}$	Digital input	Serial interface chip select 1; active low
11	SCLK	SCLK	Digital input	Serial interface shift clock
12	DIN	DIN	Digital input	Serial interface data input
13	$\overline{\text{DRDY}}$	$\overline{\text{DRDY}}$	Digital output	Data ready indicator; active low
14	DOUT/$\overline{\text{DRDY}}$	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial interface data output and data ready indicator (active low)
15	BYPASS	BYPASS	Analog output	2-V subregulator output; connect a 1-µF capacitor to DGND
16	DGND	DGND	Digital	Digital ground. Connect to ADC ground plane
17	DVDD	DVDD	Digital	Digital power supply (3 V to 5 V)
18	CLKIN	CLKIN	Digital input	1: Internal oscillator: connect to DGND 2: External clock: apply clock input
19	HV_AVSS	HV_AVSS	Analog	High-voltage negative analog power supply
20	HV_AVDD	HV_AVDD	Analog	High-voltage positive analog power supply
21,22	NC	NC	—	No connection. Electrically float or tie to AGND.
23	NC	IDAC2	Analog output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: Current source 2 output
24	NC	IDAC1	Analog output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: Current source 1 output
25	AINCOM	AINCOM	Analog input	Analog input common (single-ended common)
26	AIN0	AIN0	Analog input	Analog input 0
27	AIN1	AIN1	Analog input	Analog input 1
28	NC	GPIO3	Digital input/output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: General-purpose input/output 3
29	NC	GPIO2	Digital input/output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: General-purpose input/output 2
30	NC	REFN1/GPIO1	Analog/Digital input/output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: Reference input 1 negative and general-purpose input/output 1
31	NC	REFP1/GPIO0	Analog/Digital input/output	ADS125H01: No Connection. Electrically float or tie to AGND ADS125H02: Reference input 1 positive and general-purpose input/output 0
32	REFN0	REFN0	Analog input	Reference input 0 negative
Thermal pad				Exposed thermal pad; connect to DGND. See recommended PCB land pattern at end of document.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Power-supply voltage	HV_AVDD to HV_AVSS	–0.3	38	V
	HV_AVSS to AGND	–20	0.3	
	AVDD to AGND	-0.3	6	
	DVDD to DGND	–0.3	6	
	AGND to DGND	–0.1	0.1	
Analog input voltage	AIN0, AIN1, AINCOM	HV_AVSS – 0.3	HV_AVDD + 0.3	V
	GPIO[3:0], REFP[1:0], REFN[1:0], IDAC[2:1]	AGND – 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, START, $\overline{RESET}$, CLKIN, $\overline{DRDY}$, DOUT/$\overline{DRDY}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous (input voltage specification exceeded)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-voltage analog power supplies	HV_AVDD to HV_AVSS	10		36	V
		HV_AVSS to AGND	–18		0	
		HV_AVDD to AGND	AVDD		36	
	Low-voltage analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	2.7		5.25	V
SIGNAL INPUTS						
$V_{(AINX)}$	Absolute input voltage		See PGA Input Range			V
V_{IN}	Differential input voltage range (1)	$V_{IN} = V_{AINP} - V_{AINN}$	-20	$\pm V_{REF}$ / gain	20	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Reference voltage input	$V_{REF} = V_{(REFPx)} – V_{(REFNx)}$	0.9		AVDD	V
$V_{(REFNx)}$	Negative reference voltage		AGND – 0.05		$V_{(REFPx)}$ – 0.9	V
$V_{(REFPx)}$	Positive reference voltage		$V_{(REFNx)}$ + 0.9		AVDD + 0.05	V
GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)						
	Input voltage		AGND		AVDD	V
DIGITAL INPUTS (Other than GPIOs)						
	Input voltage		DGND		DVDD	V
EXTERNAL CLOCK						
$f_{(CLK)}$	Frequency	2.5 to 25600 SPS	1	7.3728	8	MHz
		40000 SPS	1	10.24	10.75	
	Duty cycle		40%		60%	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

(1) The full available differential input voltage range is limited under certain operating conditions. See PGA Input Range for details.

6.4 Thermal Information

THERMAL METRIC (1)		ADS125H0x RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS and gain = 1 V/V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
	Absolute input current	$V_{(AINx)}$ = 0 V			0.5		nA
	Absolute input current drift				10		pA/°C
	Differential input current	V_{IN} = 2.5 V	Standard mode		±0.1		nA
			Chop Mode(1)		5		
	Differential input current drift	V_{IN} = 2.5 V, T_A < 105°C			±10		pA/°C
	Differential input impedance				1		GΩ
	Crosstalk				1		µV/V
PGA							
	Gain				0.125, 0.1875, 0.25, 0.5, 1, 2, 4, 8, 16, 32 ,64,128		V/V
	Anti-alias filter				230		kHz
PERFORMANCE							
	Resolution	No missing codes		24			Bits
DR	Data rate			2.5		40000	SPS
	Noise performance				See Table 1 and Table 2		
INL	Integral nonlinearity	Gain = 0.125 to 32			2	10	ppm
		Gain = 64, 128			6		
V_{OS}	Offset voltage	Chop mode off, T_A = 25°C		-30 + 300 / Gain	±10 + 100 / Gain	30 + 300 / Gain	µV
		Chop mode on, T_A = 25°C		-0.5 + 0.5 / Gain	±0.5 / Gain	0.5 + 0.5 / Gain	
		After calibration			On the level of noise		
	Offset voltage drift	Chop mode off			±200 / Gain	TBD	nV/°C
		Chop mode on			±5 / Gain	TBD	
GE	Gain error	T_A = 25°C, all gains			±0.1%	0.7%	
		After calibration			On the level of noise		
	Gain drift	All gains			1	4	ppm/°C
NMRR	Normal-mode rejection ratio(2)				See Table 7		
CMRR	Common-mode rejection ratio(3)	Data rate = 20 SPS			130		dB
		Data rate = 400 SPS		85	100		
PSRR	Power-supply rejection ratio(4)	HV_AVDD, HV_AVSS			2	15	µV/V
		AVDD			5	50	
		DVDD			3	20	
VOLTAGE REFERENCE INPUTS							
	Absolute input current				±250		nA
	Input current vs voltage				15		nA/V
	Input current drift				0.2		nA/°C
	Input impedance	Differential			30		MΩ

(1) Input current in chop mode operation scales with the data rate. See graph TBD.
(2) Normal-mode rejection ratio performance is dependent on the digital filter configuration.
(3) Common-mode rejection ratio is specified at 60 Hz.
(4) Power-supply rejection ratio is specified at dc.

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Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS and gain = 1 V/V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCE(5)						
	Voltage			2.5		V
	Initial error	T_A = 25°C	TBD	±0.2%	TBD	
	Temperature drift	T_A = 0°C to 85°C		5	TBD	ppm/°C
		T_A = –40°C to 125°C		8	TBD	
	Long term drift	T_A = 85°C, 1st 1000 hr		TBD		ppm
	Thermal hysteresis(6)	First 0°C to 105°C cycle		±70		ppm
		Second 0°C to 105°C cycle		±25		
	Output current		–10		10	mA
	Load regulation			20		µV/mA
	Start-up time	Settling to ±0.001% final value		100		ms
TEMPERATURE SENSOR						
	Voltage	T_A = 25°C		122.4		mV
	Temperature coefficient			420		µV/°C
EXCITATION CURRENT SOURCES (IDACS)						
	Currents		50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000			µA
	Compliance range	All currents	AGND		AVDD – 1.1	V
	Absolute error	All currents	–5%	±0.7%	5%	
	Match error	Same current magnitudes	–1.5%	±0.1%	1.5%	
		Different current magnitudes		±1%		
	Temperature drift	Absolute		100		ppm/°C
		Matched values		5	TBD	
PGA MONITORS (7)						
	Input low threshold			HV_AVSS + 2		V
	Input high threshold			HV_AVDD – 2		V
	Output low threshold			HV_AVSS + 2		V
	Output high threshold			HV_AVDD – 2		V
REFERENCE MONITOR						
	Low voltage threshold			0.4	0.6	V
INTERNAL OSCILLATOR						
f_{CLK}	Frequency	2.5 to 25600 SPS operation		7.3728		MHz
		40000 SPS operation		10.24		
	Accuracy			±0.5%	±2%	
GENERAL-PURPOSE INPUT/OUTPUTS (GPIO)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD		AVDD	V
V_{IL}	Low-level input voltage		AGND		0.3 × AVDD	V
	Input hysteresis			0.5		V

(5) Soldered to PCB using recommended PCB layout pattern and using reflow profile per JEDEC standard J-STD-020D.1
(6) Voltage reference hysteresis measured by operating the device at 25°C cycling the device to 0°C and 105°C and returning the device to 25°C.
(7) See PGA Monitor for details.

ADVANCE INFORMATION

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS and gain = 1 V/V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT (OTHER THAN GPIO)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
		I_{OH} = 8 mA		0.75 × DVDD		
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × DVDD	V
		I_{OL} = –8 mA		0.2 × DVDD		
V_{IH}	High-level input voltage		0.7 ×DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 × DVDD	V
	Input hysteresis			0.1		V
	Input leakage				±1	µA
POWER SUPPLY						
I_{HV_AVDD} I_{HV_AVSS}	HV_AVDD, HV_AVSS supply current			1.1	1.8	mA
I_{AVDD}	AVDD supply current			2.8	4.6	mA
	Additional AVDD supply current (by function)	Voltage reference		0.2		mA
		40000 SPS operation		1		
		Current sources		As programmed		µA
I_{DVDD}	DVDD supply current			0.5	0.7	mA
		40000-SPS operation		0.7	0.9	
P_D	Power dissipation			50	80	mW

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6.6 Timing Requirements

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V.

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS1}$ or $\overline{CS2}$ falling edge	50		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	25		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
$t_{c(SC)}$	SCLK period	97		ns
$t_{w(SCH)}$, $t_{w(SCL)}$	Pulse duration, SCLK high or low	40		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge before $\overline{CS1}$ or $\overline{CS2}$ rising edge	50		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS1}$ or $\overline{CS2}$ high to reset interface	25		ns
RESET				
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	4		$1 / f_{CLK}$
CONVERSION CONTROL				
$t_{w(STH)}$	Pulse duration, START high	4		$1 / f_{CLK}$
$t_{w(STL)}$	Pulse duration: START low	4		$1 / f_{CLK}$
$t_{su(STDR)}$	Set-up time, START low or STOP command before $\overline{DRDY}$ low to *stop* next conversion (continuous mode)		100	$1 / f_{CLK}$
$t_{h(DRSP)}$	Hold time, START low or STOP command after $\overline{DRDY}$ low to continue next conversion (continuous mode)	150		$1 / f_{CLK}$

ADVANCE INFORMATION

6.7 Switching Characteristics

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V. DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND, (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
SERIAL INTERFACE					
$t_{w(DRH)}$	Pulse duration: $\overline{DRDY}$ high	16			$1/f_{CLK}$
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ falling edge to DOUT/$\overline{DRDY}$ driven	0		50	ns
$t_{p(SCDO1)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{DRDY}$			40	ns
$t_{h(SCDO1)}$	Hold time, SCLK rising edge to invalid DOUT/$\overline{DRDY}$	0			ns
$t_{h(SCDO2)}$	Hold time, last SCLK falling edge to invalid DOUT/$\overline{DRDY}$ data output function	15			ns
$t_{p(SCDO2)}$	Propagation delay time, last SCLK falling edge to DOUT/$\overline{DRDY}$ data ready function			110	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ rising edge to DOUT/$\overline{DRDY}$ high impedance			50	ns
RESET					
$t_{p(RSCN)}$	Propagation delay time, $\overline{RESET}$ rising edge or RESET command to conversion start	512			$1/f_{CLK}$
$t_{p(PRCM)}$	Propagation delay time, power on threshold voltage to ADC communication		2^{16}		$1/f_{CLK}$
$t_{p(CMCN)}$	Propagation delay time, ADC communication to conversion start	512			$1/f_{CLK}$
AC EXCITATION					
$t_{d(ACX)}$	Delay time, phase-to-phase blank period		8		$1/f_{CLK}$
$t_{c(ACX)}$	ACX period	2			t_{STDR}
CONVERSION CONTROL					
$t_{p(STDR)}$	Propagation delay time, START pin high or START command to $\overline{DRDY}$ high			2	$1/f_{CLK}$

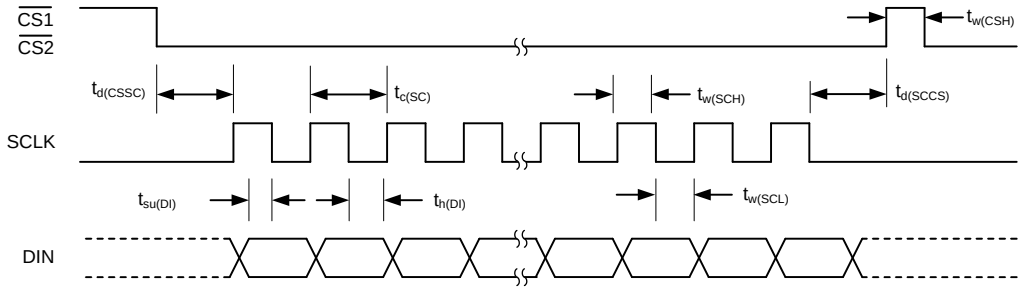
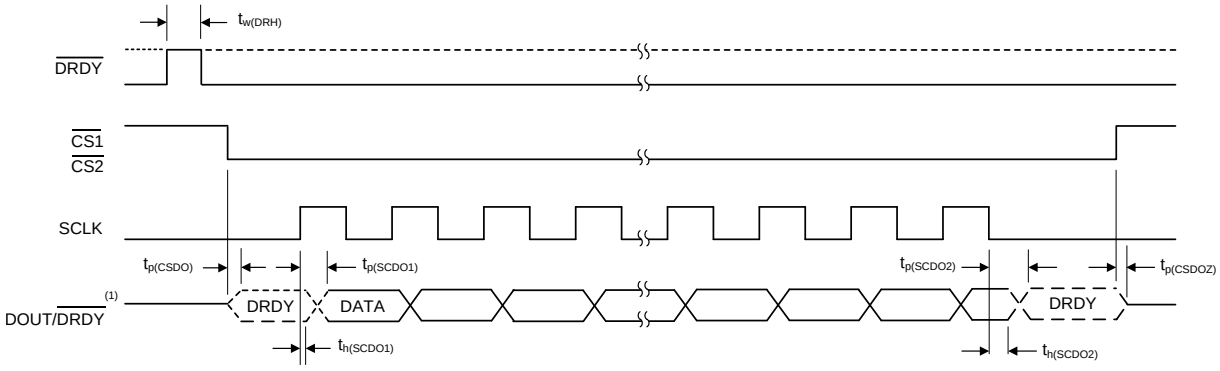


Figure 1. Serial Interface Timing Requirements



(1) DRDY = data ready function at end of command.

(2) DATA = data output function during command.

Figure 2. Serial Interface Switching Characteristics

ADVANCE INFORMATION

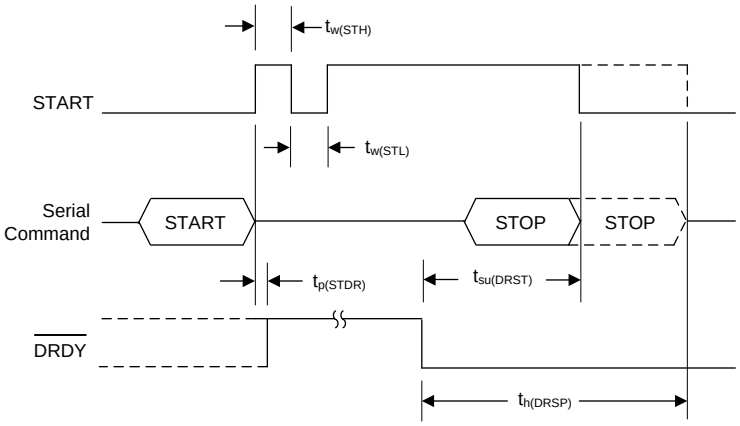


Figure 3. Conversion Control Timing Requirements

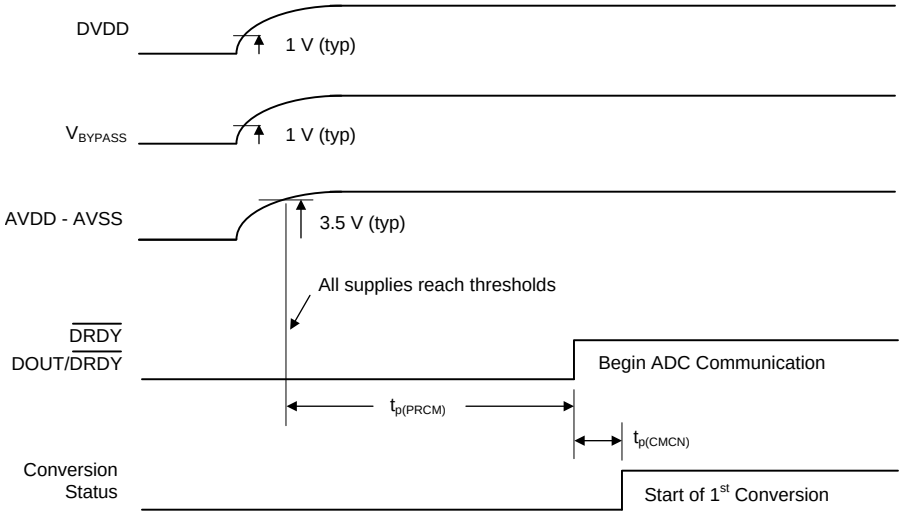


Figure 4. Power-Up Characteristics

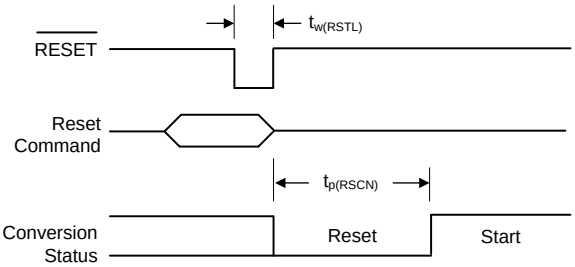


Figure 5. $\overline{\text{RESET}}$ Pin and Reset Command Timing Requirements

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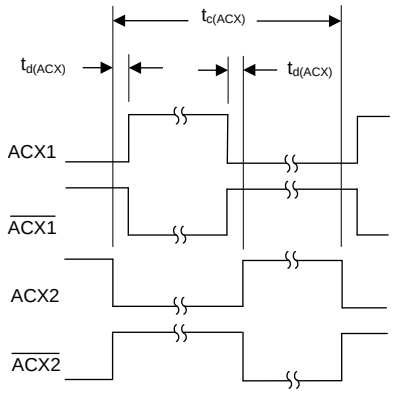

Figure 6. AC-Excitation Timing Characteristics

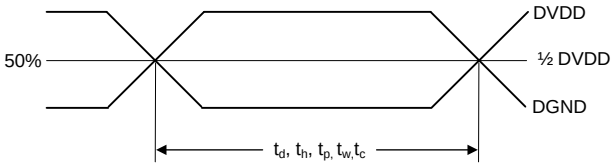

Figure 7. Timing Reference

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7 Parameter Measurement Information

7.1 Noise Performance

The ADS125H0x noise performance depends on configuration: data rate, PGA gain, digital filter configuration, and chop mode. All these parameters influence noise performance. The two largest factors affecting noise performance are data rate and gain factor. Since the noise profile is predominantly white (flat vs frequency), deceasing the data rate proportionally decreases total noise. Since the noise of the PGA is lower than that of the ADC, increasing the gain reduces noise when treated as an input-referred quantity. Noise performance also depends on the digital filter and chop mode. As the order of the digital filter increases, the noise bandwidth correspondingly decreases, which results in lower noise. As a result of two-point data averaging in chop mode, noise performance improves by $\sqrt{2}$ compared to the normal operating mode.

Table 1 shows noise performance for gains 0.125 to 2. Table 2 show noise performance for gains 4 to 128. The noise performance data are in units of μV_{RMS} (RMS = Root Mean Square) under the conditions listed. Values in parenthesis are peak-to-peak values.

Effective resolution (bits) and noise-free resolution (resolution with no code flicker) performance data are calculated using Equation 1:

$$\text{Effective Resolution or Noise-Free Bits resolution (bits)} = \ln (FSR / e_n) / \ln (2) \quad (1)$$

where

- FSR = full scale range = $2 \cdot V_{REF}$ / gain (See PGA Input Range for conditions that limit FSR)
- e_n = Input-referred voltage noise
  (use RMS value to calculate effective resolution, use p-p value to calculate noise-free resolution)

The data shown in the noise performance tables represent typical ADC performance at T_A = 25°C with chop mode disabled. The noise-performance data are the standard deviation and peak-to-peak computations of the ADC data. The noise data are acquired with inputs shorted, based on consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first. Because of the statistical nature of noise, repeated noise measurements may yield higher or lower noise performance results. Long periods of data acquisition may result in increased peak-to-peak noise results.

Table 1. Noise in μV_{RMS} (μV_{P-P}) at T_A = 25°C, 2.5-V Reference, Gain = 0.125 to 2

DATA RATE (SPS)	FILTER MODE	GAIN (V/V)					
		0.125	0.1875	0.25	0.5	1	2
2.5	FIR	1.3 (4.8)	0.89 (3.6)	0.69 (2.1)	0.49 (1.9)	0.37 (1.5)	0.17 (0.67)
2.5	Sinc1	1.1 (4.2)	0.6 (2.4)	0.57 (2.4)	0.39 (1.5)	0.29 (1)	0.15 (0.63)
2.5	Sinc2	1 (3.6)	0.68 (2)	0.44 (1.8)	0.32 (1)	0.26 (0.97)	0.12 (0.52)
2.5	Sinc3	1.1 (3)	0.67 (2)	0.49 (1.5)	0.32 (1)	0.24 (0.89)	0.11 (0.41)
2.5	Sinc4	0.98 (3.6)	0.64 (2)	0.48 (1.2)	0.3 (1)	0.26 (0.97)	0.11 (0.41)
5	FIR	1.7 (6.6)	1.2 (4.8)	0.93 (4.2)	0.57 (2.5)	0.45 (2)	0.24 (1.2)
5	Sinc1	1.5 (6.6)	0.98 (3.6)	0.77 (3.6)	0.53 (2.2)	0.4 (1.9)	0.2 (0.93)
5	Sinc2	1.3 (4.8)	0.91 (4)	0.68 (2.4)	0.44 (1.8)	0.35 (1.6)	0.18 (0.82)
5	Sinc3	1.2 (4.8)	0.83 (3.2)	0.62 (2.4)	0.39 (1.6)	0.3 (1.3)	0.16 (0.75)
5	Sinc4	1.2 (3.6)	0.75 (3.2)	0.54 (2.1)	0.38 (1.5)	0.27 (1.2)	0.14 (0.56)
10	FIR	2.4 (11)	1.6 (7.9)	1.2 (5.7)	0.82 (4.3)	0.69 (3.3)	0.34 (1.7)
10	Sinc1	1.9 (9.5)	1.4 (6.8)	1.1 (5.4)	0.7 (3.4)	0.55 (2.7)	0.3 (1.5)
10	Sinc2	1.7 (8.9)	1.2 (5.6)	0.9 (4.5)	0.56 (2.7)	0.47 (2.3)	0.24 (1.2)
10	Sinc3	1.5 (6.6)	1.1 (5.2)	0.89 (4.2)	0.54 (2.7)	0.46 (2.5)	0.24 (1.1)
10	Sinc4	1.5 (6.6)	0.99 (4.4)	0.79 (3.6)	0.49 (2.4)	0.39 (1.9)	0.2 (1)
16.6	Sinc1	2.6 (11)	1.7 (8.7)	1.4 (6.6)	0.87 (4.5)	0.72 (3.5)	0.37 (2)
16.6	Sinc2	2.1 (10)	1.5 (7.5)	1.1 (5.7)	0.78 (3.7)	0.62 (3.2)	0.32 (1.6)
16.6	Sinc3	1.9 (9.5)	1.4 (7.2)	1.1 (5.1)	0.72 (3.6)	0.54 (2.5)	0.27 (1.3)
16.6	Sinc4	1.8 (7.7)	1.3 (6.4)	0.97 (4.8)	0.65 (3.1)	0.48 (2.5)	0.24 (1.2)
20	FIR	3 (15)	2.1 (11)	1.8 (8.6)	1.1 (5.2)	0.89 (4.8)	0.46 (2.6)

Noise Performance (continued)

Table 1. Noise in μV_{RMS} (μV_{P-P}) at T_A = 25°C, 2.5-V Reference, Gain = 0.125 to 2 (continued)

DATA RATE (SPS)	FILTER MODE	GAIN (V/V)					
		0.125	0.1875	0.25	0.5	1	2
20	Sinc1	2.7 (13)	1.9 (9.5)	1.5 (7.5)	0.97 (5.5)	0.76 (4.2)	0.43 (2.3)
20	Sinc2	2.2 (11)	1.5 (7.2)	1.3 (6)	0.83 (4.2)	0.69 (3.7)	0.35 (1.8)
20	Sinc3	2.1 (10)	1.6 (8.3)	1.2 (5.4)	0.77 (4)	0.64 (3.1)	0.31 (1.6)
20	Sinc4	2 (9.5)	1.3 (6.8)	1.1 (4.8)	0.65 (3.1)	0.56 (2.7)	0.28 (1.4)
50	Sinc1	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (7.7)	1.2 (7.5)	0.64 (3.7)
50	Sinc2	3.2 (18)	2.3 (12)	1.9 (11)	1.3 (7)	1.1 (5.8)	0.54 (3.1)
50	Sinc3	3.3 (18)	2.2 (13)	1.8 (9.2)	1.2 (6.7)	0.93 (5.3)	0.49 (3)
50	Sinc4	3.1 (17)	2 (11)	1.6 (8.3)	1 (5.8)	0.87 (4.7)	0.43 (2.4)
60	Sinc1	4.5 (27)	3.1 (17)	2.4 (13)	1.6 (9.2)	1.4 (8.3)	0.69 (3.8)
60	Sinc2	3.8 (23)	2.6 (14)	2.1 (11)	1.4 (7.3)	1.2 (5.9)	0.57 (3.1)
60	Sinc3	3.4 (19)	2.3 (13)	1.8 (9.2)	1.3 (6.9)	1 (5.4)	0.54 (3.1)
60	Sinc4	3.3 (18)	2.1 (12)	1.9 (9.8)	1.2 (6.6)	0.95 (5.2)	0.52 (2.8)
100	Sinc1	5.6 (34)	4.1 (23)	3.3 (20)	2.1 (12)	1.8 (9.7)	0.91 (5.7)
100	Sinc2	4.9 (30)	3.4 (21)	2.7 (16)	1.8 (11)	1.5 (8.7)	0.75 (4.4)
100	Sinc3	4.4 (26)	3.1 (18)	2.5 (14)	1.7 (10)	1.3 (8.2)	0.69 (4.2)
100	Sinc4	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (8.5)	1.3 (7.7)	0.63 (4)
400	Sinc1	12 (74)	8.1 (55)	6.4 (43)	4.3 (27)	3.6 (25)	1.8 (11)
400	Sinc2	9.3 (60)	6.7 (44)	5.3 (32)	3.5 (23)	2.9 (19)	1.5 (10)
400	Sinc3	8.6 (54)	6.2 (39)	4.9 (32)	3.2 (20)	2.7 (17)	1.4 (9.1)
400	Sinc4	8 (52)	5.6 (37)	4.5 (30)	3 (20)	2.5 (16)	1.3 (8.3)
1200	Sinc1	20 (140)	14 (98)	11 (75)	7.3 (48)	6 (40)	3.1 (20)
1200	Sinc2	17 (110)	12 (78)	9.2 (62)	6.1 (41)	5 (33)	2.6 (18)
1200	Sinc3	15 (100)	11 (72)	8.4 (56)	5.6 (37)	4.6 (31)	2.4 (16)
1200	Sinc4	14 (95)	9.9 (68)	7.8 (51)	5.2 (37)	4.3 (29)	2.2 (15)
2400	Sinc1	27 (200)	19 (140)	15 (110)	10 (72)	8.3 (60)	4.2 (30)
2400	Sinc2	23 (180)	16 (120)	13 (97)	8.7 (62)	7 (53)	3.6 (26)
2400	Sinc3	21 (160)	15 (110)	12 (94)	7.9 (59)	6.5 (50)	3.3 (23)
2400	Sinc4	20 (140)	14 (100)	11 (78)	7.3 (53)	6 (43)	3.1 (22)
4800	Sinc1	37 (270)	26 (200)	21 (160)	14 (110)	11 (83)	5.6 (42)
4800	Sinc2	33 (250)	23 (170)	18 (140)	12 (88)	9.8 (73)	5 (40)
4800	Sinc3	31 (230)	21 (150)	17 (130)	11 (83)	9 (65)	4.7 (36)
4800	Sinc4	29 (220)	20 (150)	16 (120)	11 (81)	8.5 (63)	4.4 (33)
7200	Sinc1	44 (330)	31 (230)	24 (180)	16 (120)	13 (98)	6.5 (48)
7200	Sinc2	39 (300)	28 (210)	22 (170)	14 (100)	12 (90)	5.9 (46)
7200	Sinc3	37 (280)	26 (200)	21 (160)	13 (100)	11 (82)	5.5 (41)
7200	Sinc4	35 (260)	25 (180)	20 (150)	13 (95)	10 (81)	5.3 (41)
14400	Sinc5	53 (430)	36 (290)	29 (220)	18 (140)	14 (120)	7.4 (58)
19200	Sinc5	72 (560)	50 (390)	39 (320)	23 (180)	17 (130)	8.8 (71)
25600	Sinc5	150 (1300)	100 (870)	79 (640)	42 (350)	26 (220)	13 (110)
40000	Sinc5	250 (2000)	160 (1300)	120 (1000)	65 (530)	37 (310)	19 (150)

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Table 2. Noise in μV_{RMS} (μV_{P-P}) at T_A = 25°C, 2.5-V Reference, Gain = 4 to 128

DATA RATE (SPS)	FILTER MODE	GAIN (V/V)					
		4	8	16	32	64	128
2.5	FIR	0.082 (0.35)	0.051 (0.2)	0.032 (0.14)	0.027 (0.11)	0.027 (0.1)	0.029 (0.12)
2.5	Sinc1	0.088 (0.35)	0.05 (0.19)	0.024 (0.089)	0.024 (0.089)	0.023 (0.098)	0.024 (0.1)
2.5	Sinc2	0.059 (0.24)	0.037 (0.14)	0.021 (0.084)	0.018 (0.072)	0.017 (0.076)	0.019 (0.076)
2.5	Sinc3	0.06 (0.24)	0.034 (0.13)	0.019 (0.075)	0.017 (0.07)	0.016 (0.073)	0.018 (0.075)
2.5	Sinc4	0.054 (0.19)	0.034 (0.13)	0.019 (0.075)	0.016 (0.065)	0.015 (0.062)	0.016 (0.069)
5	FIR	0.12 (0.52)	0.071 (0.33)	0.046 (0.21)	0.038 (0.19)	0.039 (0.17)	0.037 (0.18)
5	Sinc1	0.11 (0.48)	0.061 (0.28)	0.038 (0.18)	0.029 (0.14)	0.029 (0.15)	0.029 (0.13)
5	Sinc2	0.093 (0.43)	0.048 (0.21)	0.029 (0.14)	0.024 (0.11)	0.026 (0.12)	0.023 (0.1)
5	Sinc3	0.081 (0.41)	0.044 (0.2)	0.03 (0.13)	0.023 (0.1)	0.022 (0.1)	0.022 (0.11)
5	Sinc4	0.066 (0.3)	0.043 (0.2)	0.027 (0.13)	0.022 (0.093)	0.022 (0.11)	0.021 (0.096)
10	FIR	0.19 (1)	0.099 (0.51)	0.064 (0.36)	0.053 (0.29)	0.051 (0.3)	0.054 (0.3)
10	Sinc1	0.16 (0.82)	0.086 (0.46)	0.054 (0.3)	0.045 (0.22)	0.043 (0.21)	0.044 (0.23)
10	Sinc2	0.12 (0.56)	0.068 (0.36)	0.044 (0.23)	0.037 (0.2)	0.034 (0.18)	0.033 (0.18)
10	Sinc3	0.11 (0.52)	0.066 (0.31)	0.042 (0.21)	0.032 (0.17)	0.032 (0.16)	0.032 (0.16)
10	Sinc4	0.096 (0.45)	0.059 (0.31)	0.039 (0.2)	0.032 (0.17)	0.031 (0.16)	0.03 (0.15)
16.6	Sinc1	0.19 (1)	0.11 (0.56)	0.075 (0.38)	0.054 (0.3)	0.055 (0.29)	0.056 (0.31)
16.6	Sinc2	0.16 (0.89)	0.086 (0.4)	0.054 (0.27)	0.044 (0.22)	0.049 (0.24)	0.046 (0.24)
16.6	Sinc3	0.15 (0.73)	0.084 (0.41)	0.053 (0.27)	0.041 (0.22)	0.04 (0.22)	0.041 (0.2)
16.6	Sinc4	0.13 (0.67)	0.076 (0.39)	0.053 (0.29)	0.042 (0.24)	0.04 (0.21)	0.036 (0.17)
20	FIR	0.24 (1.2)	0.14 (0.72)	0.088 (0.45)	0.072 (0.38)	0.071 (0.37)	0.074 (0.37)
20	Sinc1	0.22 (1.1)	0.12 (0.58)	0.079 (0.41)	0.064 (0.32)	0.061 (0.32)	0.06 (0.34)
20	Sinc2	0.18 (1)	0.1 (0.57)	0.062 (0.34)	0.049 (0.25)	0.049 (0.26)	0.047 (0.29)
20	Sinc3	0.16 (0.89)	0.089 (0.48)	0.063 (0.32)	0.046 (0.22)	0.045 (0.21)	0.045 (0.23)
20	Sinc4	0.15 (0.82)	0.083 (0.41)	0.056 (0.29)	0.045 (0.23)	0.042 (0.22)	0.046 (0.24)
50	Sinc1	0.35 (2.1)	0.19 (1.1)	0.12 (0.69)	0.097 (0.52)	0.096 (0.57)	0.098 (0.58)
50	Sinc2	0.28 (1.6)	0.15 (0.84)	0.099 (0.56)	0.075 (0.43)	0.077 (0.43)	0.076 (0.46)
50	Sinc3	0.25 (1.5)	0.14 (0.75)	0.093 (0.51)	0.074 (0.41)	0.07 (0.38)	0.071 (0.37)
50	Sinc4	0.23 (1.4)	0.13 (0.76)	0.087 (0.47)	0.066 (0.37)	0.065 (0.35)	0.065 (0.37)
60	Sinc1	0.38 (2.2)	0.21 (1.2)	0.14 (0.79)	0.11 (0.57)	0.1 (0.59)	0.1 (0.6)
60	Sinc2	0.3 (1.7)	0.17 (0.93)	0.11 (0.66)	0.085 (0.47)	0.084 (0.49)	0.083 (0.49)
60	Sinc3	0.27 (1.6)	0.15 (0.79)	0.097 (0.53)	0.078 (0.43)	0.078 (0.43)	0.076 (0.42)
60	Sinc4	0.27 (1.6)	0.14 (0.89)	0.092 (0.5)	0.075 (0.46)	0.076 (0.4)	0.073 (0.4)
100	Sinc1	0.49 (2.8)	0.27 (1.5)	0.17 (1)	0.14 (0.81)	0.14 (0.88)	0.13 (0.81)
100	Sinc2	0.39 (2.3)	0.22 (1.4)	0.14 (0.87)	0.11 (0.63)	0.11 (0.69)	0.11 (0.66)
100	Sinc3	0.35 (2.1)	0.2 (1.2)	0.13 (0.75)	0.1 (0.63)	0.1 (0.61)	0.1 (0.69)
100	Sinc4	0.32 (2)	0.18 (1.2)	0.13 (0.73)	0.094 (0.57)	0.092 (0.56)	0.093 (0.57)
400	Sinc1	0.94 (6)	0.53 (3.5)	0.34 (2.1)	0.27 (1.8)	0.27 (1.7)	0.27 (1.8)
400	Sinc2	0.78 (5.2)	0.44 (3.1)	0.29 (1.8)	0.22 (1.4)	0.22 (1.4)	0.22 (1.4)
400	Sinc3	0.72 (4.6)	0.4 (2.6)	0.26 (1.6)	0.2 (1.3)	0.2 (1.3)	0.2 (1.3)
400	Sinc4	0.67 (4.2)	0.37 (2.4)	0.24 (1.6)	0.19 (1.2)	0.19 (1.2)	0.19 (1.1)
1200	Sinc1	1.6 (12)	0.91 (6.3)	0.59 (4.1)	0.46 (3.1)	0.45 (3.1)	0.45 (3.1)
1200	Sinc2	1.3 (9.3)	0.76 (5.2)	0.49 (3.2)	0.39 (2.6)	0.38 (2.6)	0.38 (2.6)
1200	Sinc3	1.2 (8.2)	0.69 (4.7)	0.45 (3.1)	0.35 (2.4)	0.35 (2.4)	0.35 (2.2)
1200	Sinc4	1.2 (7.6)	0.64 (4.3)	0.41 (2.7)	0.33 (2.3)	0.32 (2.2)	0.32 (2.3)
2400	Sinc1	2.2 (17)	1.2 (8.9)	0.81 (5.8)	0.64 (4.5)	0.62 (4.5)	0.62 (4.6)
2400	Sinc2	1.9 (14)	1.1 (7.7)	0.68 (5)	0.54 (3.9)	0.54 (3.9)	0.54 (4)

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Table 2. Noise in μV_{RMS} (μV_{P-P}) at T_A = 25°C, 2.5-V Reference, Gain = 4 to 128 (continued)

DATA RATE (SPS)	FILTER MODE	GAIN (V/V)					
		4	8	16	32	64	128
2400	Sinc3	1.7 (14)	0.97 (7.1)	0.62 (4.4)	0.49 (3.5)	0.48 (3.4)	0.49 (3.5)
2400	Sinc4	1.6 (12)	0.91 (6.7)	0.59 (4.1)	0.46 (3.5)	0.46 (3.4)	0.46 (3.4)
4800	Sinc1	3 (23)	1.6 (13)	1.1 (7.8)	0.83 (6.2)	0.83 (6.2)	0.82 (6.1)
4800	Sinc2	2.6 (20)	1.5 (12)	0.95 (7.2)	0.75 (5.6)	0.74 (5.4)	0.73 (5.5)
4800	Sinc3	2.4 (19)	1.4 (10)	0.89 (6.4)	0.69 (5)	0.68 (5.2)	0.69 (5.5)
4800	Sinc4	2.3 (17)	1.3 (9.8)	0.82 (6.2)	0.64 (5)	0.65 (4.9)	0.64 (4.9)
7200	Sinc1	3.3 (25)	1.9 (15)	1.2 (9)	0.95 (7)	0.94 (6.9)	0.94 (7.1)
7200	Sinc2	3.1 (24)	1.7 (13)	1.1 (8.7)	0.87 (6.6)	0.86 (6.5)	0.86 (6.4)
7200	Sinc3	2.9 (22)	1.6 (12)	1.1 (7.9)	0.83 (6.1)	0.82 (6.2)	0.82 (6.4)
7200	Sinc4	2.8 (21)	1.6 (12)	1 (7.7)	0.79 (5.8)	0.78 (6)	0.78 (5.8)
14400	Sinc5	3.8 (29)	2.1 (17)	1.4 (11)	1.1 (8.4)	1.1 (8.1)	1 (8.4)
19200	Sinc5	4.6 (36)	2.5 (20)	1.6 (13)	1.2 (9.6)	1.2 (9.3)	1.2 (9.5)
25600	Sinc5	6.7 (56)	3.6 (29)	2.1 (17)	1.5 (13)	1.4 (12)	1.4 (12)
40000	Sinc5	9.6 (80)	5 (43)	2.9 (23)	2 (16)	1.8 (15)	1.8 (15)

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8 Detailed Description

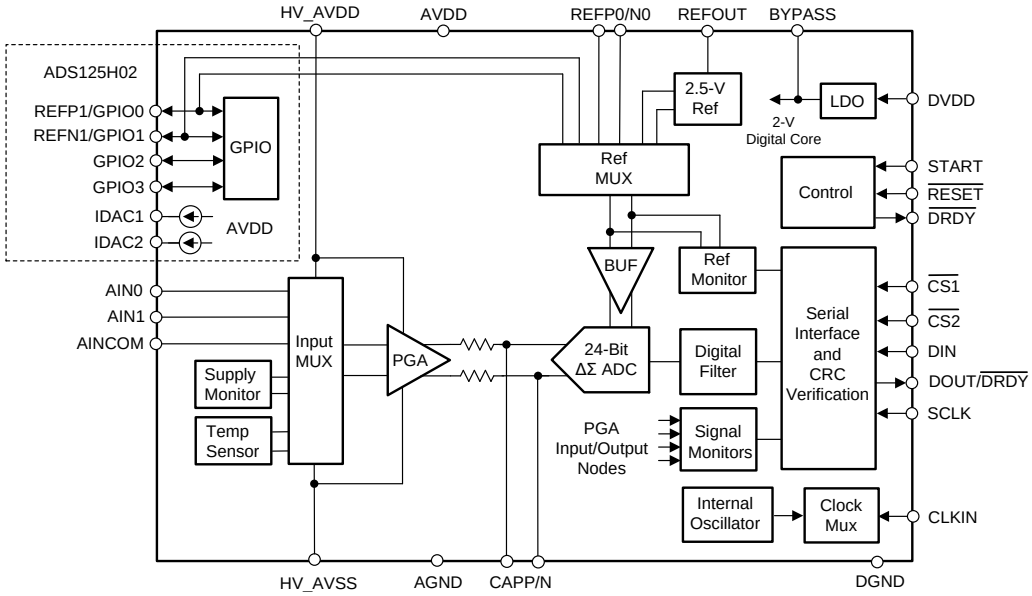
8.1 Overview

The ADS125H01 and ADS125H02 are 2-channel (configurable as two single-ended input channels or one differential input channel), ±20-V differential, ±15.5-V absolute voltage input, 24-bit, 40000-SPS, delta-sigma (ΔΣ) ADCs. The devices also include a Programmable Gain Amplifier (PGA), monitors and voltage reference. The ADCs provide complete, high-accuracy, one-chip measurement solutions over a wide range of common-mode voltages, including ±10-V and 20-mA transmitters, strain-gauge sensors, thermocouples, and resistance temperature detectors (RTD). The ADS125H02 is backward compatible to the ADS125H01. The ADS125H02 includes two sensor excitation current sources (IDACs), four GPIO ports, and one additional reference input.

Key features of the ADC are:

- ±20-V differential, ±15.5-V absolute input voltage range
- High input impedance PGA and high-resolution, 24-bit ΔΣ ADC
- 2.5-V voltage reference
- Internal oscillator
- Signal and voltage reference monitors
- Temperature sensor
- SPI compatible serial interface with CRC error checking
- One or two external voltage reference inputs (ADS125H01 or ADS125H02, respectively)
- Two current sources (ADS125H02)
- Four GPIO with AC-excitation (ADS125H02)

8.2 Functional Block Diagram



Analog inputs (AIN0, AIN1, AINCOM) connect to the input multiplexer (MUX) for input channel selection. The ADC supports one differential or two single-ended input configurations. The input channel multiplexer is powered by the high-voltage analog power supplies.

The programmable gain amplifier (PGA) follows the input multiplexer. The PGA is high input impedance, CMOS differential input – differential output, programmable gain and programmable attenuation amplifier. In attenuation setting, the PGA translates the high-level input voltage to the low-level (5-V) voltage range of the ADC. In gain setting, the PGA amplifies the low-level input voltage to the input range of the ADC. The PGA output connects to pins CAPP and CAPN. The ADC anti-alias filter is formed by PGA output resistors and the external capacitor.

Key nodes of the PGA are monitored for linear operation. Bits in the status register are set when the PGA overrange condition is detected.

Functional Block Diagram (continued)

The delta-sigma modulator measures the input voltage relative to the reference voltage to produce the 24-bit conversion result. The input range of the ADC is $\pm V_{REF}$ / Gain.

The digital filter averages and decimates the modulator output data to produce the final, down-sampled conversion result. The sinc filter is programmable (sinc1 through sinc5) allowing optimization of conversion time, noise and line-cycle rejection. The finite impulse response (FIR) filter mode provides single-cycle settled data while simultaneously rejecting 50/60-Hz frequencies at data rate of 20 SPS.

The ADC reference voltage is internal (2.5 V) or external reference. The REFOUT pin is the buffered, 2.5-V reference output. The reference is monitored for out-of-range operation. The ADS125H02 provides two voltage reference input pin pairs.

The ADS125H02 includes two current sources (IDAC1, IDAC2), that operate from the 5-V analog power supply. The IDACs provide excitation current for resistive sensors (for example, RTD). Additionally, the ADS125H02 provides four GPIO ports. The GPIOs control external multiplexers and input and output of general-purpose logic signals.

The ADC has an internal temperature sensor to monitor device temperature. The high-voltage power supply voltage is available for readback verification through the ADC.

The SPI-compatible serial interface is used to read the conversion data and for ADC configuration. Communication is validated by a CRC. The serial interface consists of the following signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN and DOUT/$\overline{DRDY}$. The dual function DOUT/$\overline{DRDY}$ is the serial data output and the data ready functions combined into one pin. $\overline{DRDY}$ is the dedicated data ready output.

The ADC clock is either the internal oscillator or external. The external clock is selected automatically. The clock frequency is 7.3728 MHz (10.24 MHz in 40000 SPS operation).

ADC conversions are controlled by the START pin or by the START command. The ADC is programmable for continuous mode or one-shot conversions.

The ADC is automatically reset at power-up, by the $\overline{RESET}$ input or by the RESET command.

The input signal multiplexer and PGA are powered by the high-voltage power supplies (HVAVDD and HV_AVSS). The high-voltage power supplies are configurable to either bipolar or unipolar modes (up to ±18 V, or up to 36 V). The modulator, voltage reference and excitation current sources are powered by the AVDD power supply (5 V). The digital I/O is powered by DVDD (3 V to 5 V range). An internal sub-regulator powers the ADC digital core. A external bypass capacitor is required to connect to the sub-regulator output (BYPASS).

ADVANCE INFORMATION

8.3 Feature Description

The following sections describe the ADS125H0x functional blocks.

8.3.1 Analog Inputs

As shown in Figure 8, the analog inputs of the ADC consist of ESD protection diodes and input multiplexer. The multiplexer supports three external input and three internal measurement configurations.

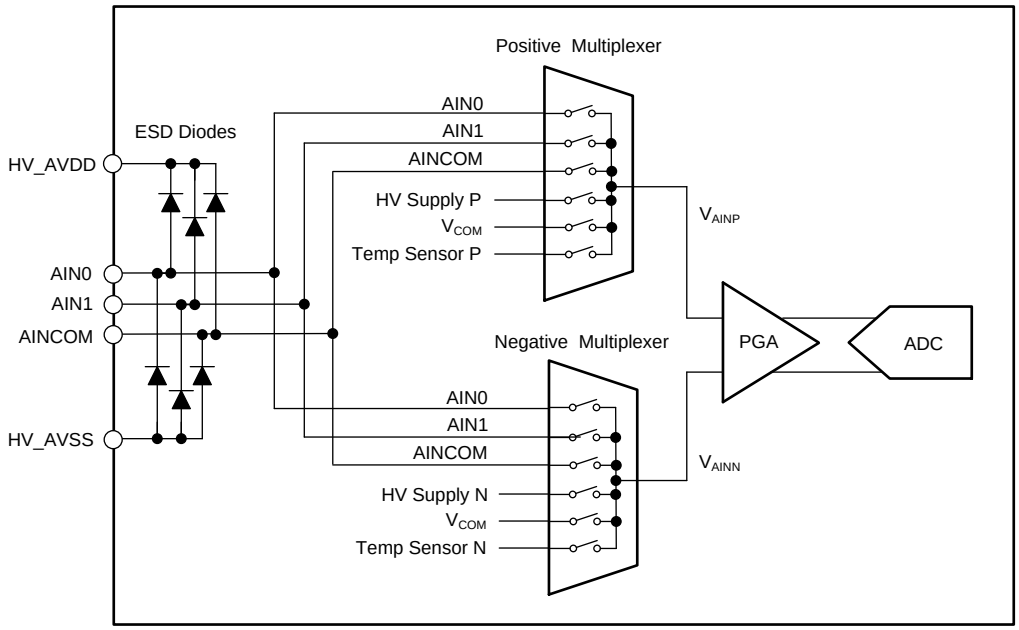


Figure 8. Analog Input Diagram

8.3.1.1 ESD Diodes

ESD diodes are incorporated to protect the ADC inputs from possible ESD events occurring during the manufacturing process and during PCB assembly when manufactured in an ESD-controlled environment. For system-level ESD protection, consider the use of external ESD protection devices for pins that are exposed to ESD, including the analog inputs.

If either input is driven below HV_AVSS – 0.3 V, or above HV_AVDD + 0.3 V, the internal protection diodes may conduct. If these conditions are possible, input current may flow into the inputs. Use external clamp diodes, series resistors, or both to limit the input current to the specified maximum value.

Feature Description (continued)

8.3.1.2 Input Multiplexer

The input multiplexer selects the signal for measurement. The ADC supports two single-ended measurements (AIN0 – AINCOM, or AIN1 – AINCOM) and one differential input measurement (AIN1 – AIN0). The multiplexer is programmed by the MUX[2:0] bits of the MODE4 Register (address = 10h). Use the multiplexer to select the inputs as listed in Table 3.

Table 3. Input Multiplexer Settings

MUX[2:0] BITS OF REGISTER MODE4 (10h)	MEASUREMENT (P – N)
000	AIN1 – AIN0
001	AIN0 – AIN1 (reserved for use with final silicon)
010	AIN1 – AINCOM
011	AIN0 – AINCOM
100	HV supply readback: (HV_AVDD – HV_AVSS) / 36
101	PGA inputs connected to V_{COM}: (HV_AVDD + HV_AVSS) / 2 (default)
110	Temperature sensor
111	Reserved

8.3.2 Temperature Sensor

The ADC has an internal temperature sensor. The temperature sensor is comprised of two internal diodes with one diode having 80 times the current density of the other. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. To measure the temperature sensor, write 110b to select the temperature sensor and then start a new ADC conversion. Equation 2 shows how to convert the temperature sensor reading to degrees Celsius (°C):

$$\text{Temperature (°C)} = [(\text{Temperature Reading (µV)} - 122{,}400) / 420\ \text{µV/°C}] + 25°\text{C} \quad (2)$$

When measuring the temperature sensor, set the gain equal to 1 and disable the chop and AC-excitation modes. As a result of the low package-to-PCB thermal resistance, the internal temperature closely tracks the PCB temperature. Be aware that device self-heating increases the internal temperature relative to the surrounding PCB.

8.3.3 High-Voltage Power-Supply Readback

Read the high-voltage power supply by selection through the input multiplexer. The supply voltage is internally divided by 36 for measurement. Equation 3 shows the supply voltage scaling.

$$\text{High-voltage power supply (V)} = (\text{HV\_AVDD} - \text{HV\_AVSS}) / 36 \quad (3)$$

Measure the high-voltage power supply using the internal or external reference. To measure, disable chop and AC-excitation modes. Write the 100b to the multiplexer control bits to select the input multiplexer and then start a new conversion.

8.3.4 Internal V_{COM} Connection (default)

For this multiplexer configuration, the external inputs are open and the PGA inputs connect to an internal V_{COM} voltage as defined: (HV_AVDD + HV_AVSS) / 2. Use this mode to measure the ADC noise performance and offset voltage, or to short the inputs for offset calibration. Be aware that shorting the inputs to the system yield the best calibration results. Short the V_{COM} input connection by writing the 101b to the Multiplexer Control register. Using the desired ADC configuration, start a new conversion with the inputs shorted.

ADVANCE INFORMATION

8.3.5 PGA

The PGA is a low-noise, programmable gain and programmable attenuation, CMOS differential-input, differential-output amplifier. The PGA operates in gain or attenuation mode depending on the programming. Program the PGA for gain mode when the signal is less than the reference voltage. Program the PGA for attenuation mode when signal is greater than the reference voltage.

Figure 9 shows the PGA block diagram. The PGA consists of two stages. The first stage is a high input impedance, CMOS differential input – differential output, noninverting input amplifier. The stage is powered by the high-voltage analog power supplies (HV_AVDD and HV_AVSS). The first stage provides gain of 1 V/V to 128 V/V.

The second stage is differential input – differential output, inverting amplifier powered by the low-voltage analog supply (AVDD). The second stage provides attenuations from 0.5 V/V to 0.125 V/V. The common-mode voltage of the second stage is regulated to AVDD / 2. The second stage output drives the ADC inputs. The output connects to the CAPP and CAPN pins. Connect an external 1-nF capacitor to these pins to form the ADC antialias filter. The filter also provides a bypass for the modulator sampling pulses. CAPP and CAPN nodes are sensitive to interference from noise. As a result, place the capacitor close to the pins using short, direct traces. Avoid running clock traces or other digital traces in the vicinity of these pins.

Amplifiers A1 and A2 are protected by inverse-parallel diodes connected across the amplifier inputs. The diodes are in addition to the input ESD-protection diodes. When the signal to the PGA is out-of-range, causing the amplifiers to saturate, the diodes may conduct resulting in current flow through the inputs. Additionally, high dV/dt signal conditions, such as caused by switching of a signal multiplexer, may cause a transient turn-on of the protection diodes. Use an RC filter on the PGA inputs to limit the dV/dt of the signal to eliminate transient diode turn-on.

The PGA incorporates filters to improve rejection by RFI and EMI noise interference. Key nodes of the PGA input and output circuit are monitored for possible out-of-range condition. If an out-of-range condition is detected, the monitors set appropriate alarm bits in the status register.

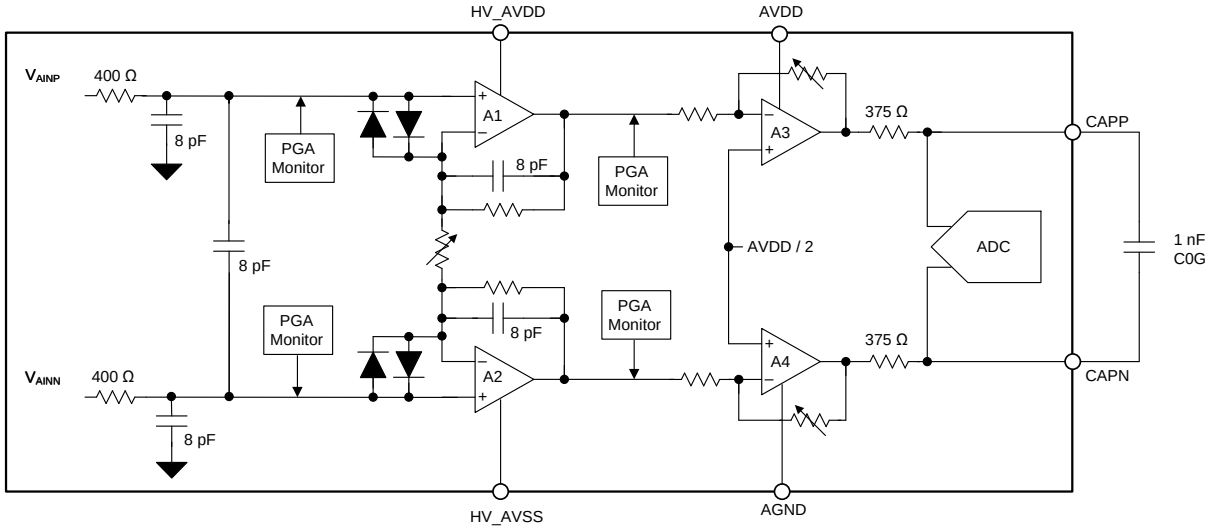


Figure 9. PGA Block Diagram

8.3.5.1 PGA Input Range

The reference voltage and the PGA gain (attenuation) determine the full-scale, differential input range of the ADC. Table 4 lists full-scale input range verses gain (attenuation) when operating with a 2.5-V reference. The full-scale input range scales with the reference voltage. The table shows examples of system-level ranges for differential and single-ended input configurations. The example ranges shown include margin for overrange. The high resolution afforded by the ADC provides accurate measurements for *unipolar* input, single-ended configurations with low loss of resolution.

Table 4. Full-Scale Voltage Range

GAIN[2:0] BITS	GAIN (V/V)	FULL SCALE INPUT RANGE(1)	EXAMPLE DIFFERENTIAL RANGE	EXAMPLE SINGLE-ENDED RANGE (2)
0000	0.125	±20 V(3)	±18 V	0 V to ±15.5 V
0001	0.1875	±13.3 V	±10 V	0 V to ±10 V
0010	0.25	±10 V	±8 V	0 V to ±8 V
0011	0.5	±5 V	±4 V	0 V to ±4 V
0100	1	±2.5 V	±2 V	0 V to ±2V
0101	2	±1.25 V	±1 V	0 V to ±1 V
0110	4	±0.625 V	±0.5 V	0 V to ±0.5 V
0111	8	±0.312 V	±0.25V	0 V to ±0.25 V
1000	16	±0.156 V	±0.125 V	0 V to ±0.125 V
1001	32	±0.078 V	±0.062 V	0 V to ±0.062 V
1010	64	±0.039 V	±0.031 V	0 V to ±0.031 V
1011	128	±0.019 V	±0.015 V	0 V to ±0.015 V

(1) V_{REF} = 2.5 V. HV_AVDD and HV_AVSS = ±18 V.
(2) Bipolar supply operation
(3) Maximum differential input range is limited to ±20 V

As with many amplifiers, the PGA has limits for the maximum input voltage that must not be exceeded. The *absolute input voltage* is defined as the signal and common-mode voltages combined. The maximum input voltage depends on the PGA gain, the maximum expected differential voltage (V_{IN}), and the minimum expected high-voltage power supply. For linear operation of the PGA, maintain the absolute input voltage within range, as given by Equation 4:

Absolute Input Voltage: $HV\_AVSS + 2.5 + V_{IN} \times (Gain - 1) / 2 < V_{(AINx)} < HV\_AVDD - 2.5 - V_{IN} \times (Gain - 1) / 2$

where

- For gain < 1, use gain = 1 in the equation
- $V_{(AINx)}$ = absolute input voltage
- V_{IN} = maximum differential input voltage = $V_{AINP} - V_{AINN}$ (4)

The full available *differential* input voltage is also limited under certain operating conditions. The first condition is operation with reference voltage > AVDD - 1 V (all gains and attenuations). In this case, the differential input voltage is limited to V_{IN} < ± (AVDD - 1 V) / gain. Additionally, the maximum differential input voltage is limited to ±20 V, irrespective of gain (attenuation) factor or reference voltage.

The relationship between PGA input to PGA output is shown in Figure 10 and Figure 11. In attenuation mode, the first PGA stage is configured as a unit-gain follower. The second PGA stage attenuates the differential input and establishes the common-mode output voltage of the signal to AVDD / 2.

In gain mode, first PGA stage amplifies the differential signal. The output voltage of each PGA stage must be maintained within the voltage headroom as shown in the shaded areas of the figures.

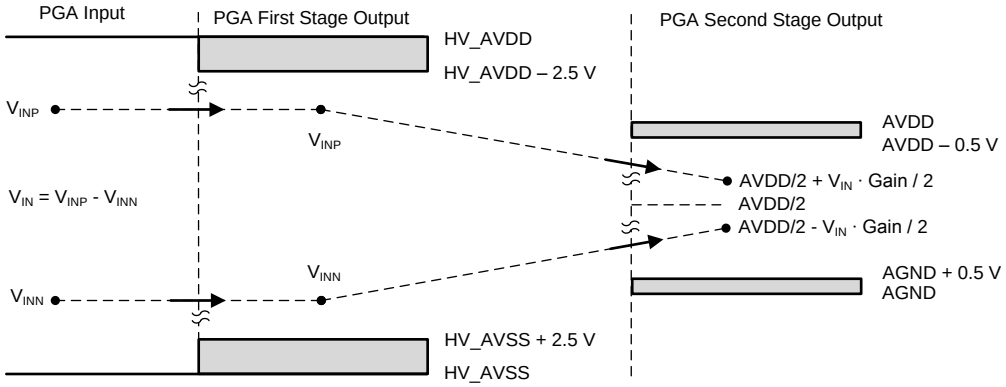


Figure 10. PGA - Attenuation Mode

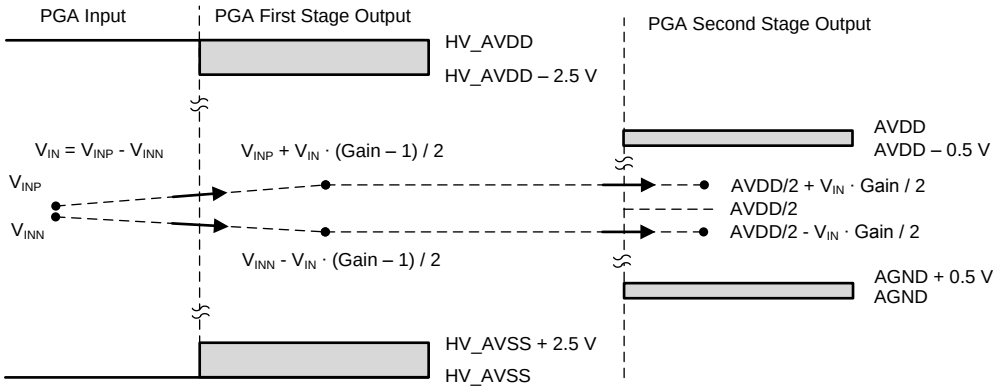


Figure 11. PGA - Gain Mode

8.3.5.2 PGA Monitor

The PGA has a linear operating range that must not be exceeded, otherwise the conversion data are not valid. The ADC includes PGA monitors that flag when the amplifier is in a overload condition. As shown in Figure 12, the input and output nodes of the PGA first stage are monitored by high and low voltage detectors. The low threshold is HV_AVDD – 2 V and the high threshold is HV_AVSS + 2 V. See Figure 13. There are four nodes that are monitored, each with high/low alarm states for a total of 8 monitor flags that are reported in the status byte.

Monitor for the occurrence of a possible PGA overload condition by polling the STAT12 bit (bit 4) of the STATUS0 byte. This flag indicates if one or more PGA alarm flags are set or if a CRC-2 error occurred. Poll STATUS1 and STATUS2 registers (11h and 12h) to determine the source of the error. If the PGA is in an overload condition, the flag bits of the STATUS1 register are set. The PGA status flags are latched in the STATUS1 register. The flags are reset by the read operation (clear-on-read operation). The PGA overload flags, CRC1ERR and CRC2ERR flags must be cleared to clear the global error flag, STAT12. See Table 43 for the description of the PGA alarm bits.

The PGA monitors are fast-responding, analog comparators. Therefore, the monitors are capable of detecting short-transient overload conditions. Be aware that short duration PGA overload events may not result in clipped conversion values because of the data integration operations (averaging) of the digital filter.

Be aware that certain input overload conditions may trigger input alarms without necessarily triggering the corresponding output alarms.

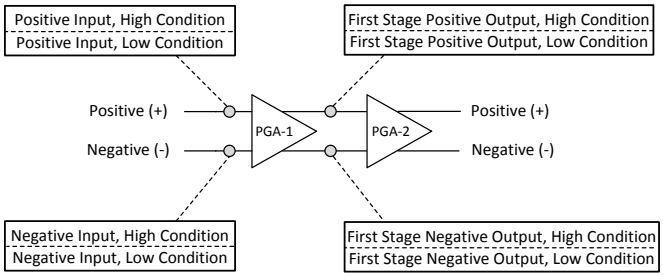


Figure 12. PGA Monitors

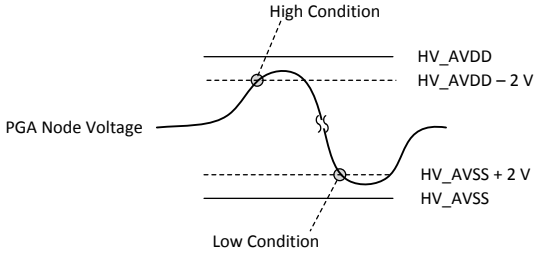
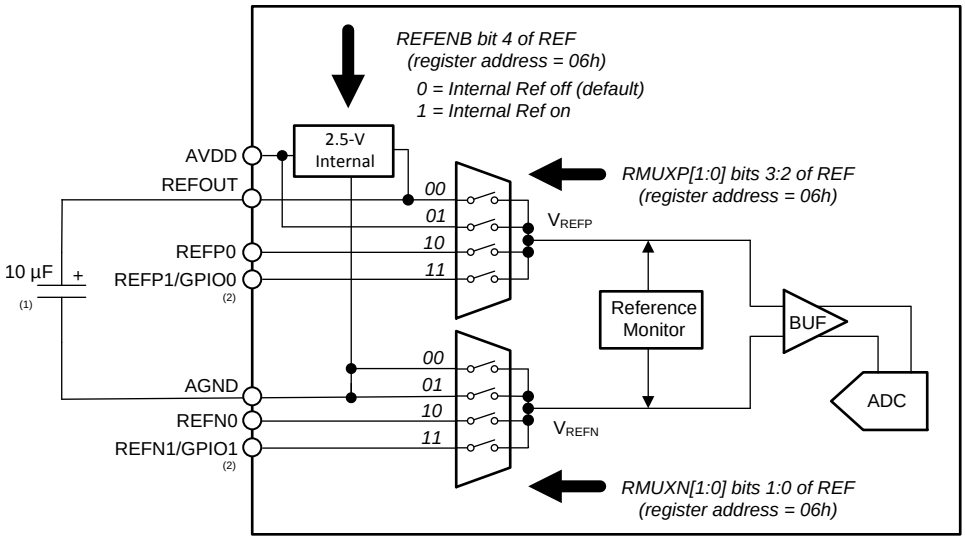


Figure 13. PGA Monitor Thresholds

8.3.6 Reference Voltage

The ADC reference voltage is either 2.5-V internal, one of two external reference pin pairs, or the AVDD power supply (5 V). The reference voltage is defined as $V_{REF} = V_{REFP} – V_{REFN}$, where V_{REFP} and V_{REFN} are the positive and negative reference voltages, respectively. The polarity of V_{REF} must always be positive. Figure 14 shows the block diagram of the reference multiplexer.



(1) The internal reference requires a 10-µF capacitor connected to the REFOUT and AGND pins.

(2) ADS125H02 only provides the second reference input pin pairs.

Figure 14. Reference Multiplexer Diagram

Program RMUXP[1:0] and RMUXN[1:0] bits of the REF Register to select the positive and negative reference voltages, respectively. The positive reference options are internal reference positive, external REFP0, external REFP1, or AVDD. The negative selections are internal reference negative, external REFN0, external REFN1, or AGND.

The reference voltage is monitored for low voltage conditions. See Reference Monitor.

8.3.6.1 Internal Reference

The ADC includes a precision 2.5-V reference. Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to "00" to select the internal reference. The REF_ENB bit of the REF register controls the reference bias (default = off). Enable the reference if using the current sources. A 10-µF capacitor is required between the REFOUT and AGND pins in order to filter reference noise. The capacitor is not required if not using the internal reference.

Be aware of AVDD inrush current when the reference is enabled as a result of charging the 10-µF REFOUT capacitor. Also, when the reference is enabled, be aware of the time for reference stabilization before beginning conversions or before calibrating the ADC. REFOUT is the reference output and AGND is the reference return. Use a star layout connection for the reference return and make this connection close to the AGND pin.

8.3.6.2 External Reference

Use an external reference by applying the reference voltage to one of the reference input pin pairs. The reference inputs are differential with positive and negative inputs. Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to "10" or "11" to select inputs (REFP0, REFN0) and (REFP1, REFN1), respectively. Pins REFP1, REFN1 are available with ADS125H02 only. Follow the specified absolute and differential reference voltage operating conditions. See Recommended Operating Conditions. Use a 10-nF bypass capacitor across the reference input pins to filter noise. Be aware that the reference inputs have input current that lead to voltage errors if large reference impedances are present. When the impedances are present, consider the impact of the error to the reference voltage.

8.3.6.3 AVDD Power-Supply Reference

Use the AVDD power supply as reference by setting the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to "01" (default mode of operation). For 6-wire load cell applications with excitation sense connections, or AC-excitation mode, connect the sense voltage to the reference inputs and program the ADC for *external* reference operation.

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8.3.6.4 Reference Monitor

The ADC incorporates a reference monitor to detect a low or missing reference voltage. As shown in Figure 15 and Figure 16, if the reference voltage (V_{REF} = V_{REFP} – V_{REFN}) is below 0.4 V, the REFALM bit is set in the STATUS0 byte. The alarm is read only and resets at the next conversion after the condition is removed. Use the reference monitor to detect a missing or failed reference voltage.

To implement the reference alarm, use a 100-kΩ resistor across the reference inputs. The resistor biases the P and N reference inputs to 0 V if either input is not connected. Poll bit 3 (REFALM) of the STATUS0 byte to determine if the reference alarm is set.

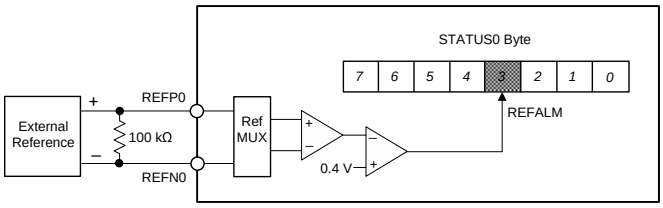

Figure 15. Reference Monitor

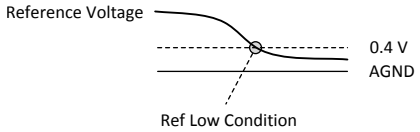

Figure 16. Reference Monitor Threshold

8.3.7 Current Sources (IDAC1 and IDAC2)

The ADS125H02 incorporates two current sources designed to provide excitation current to RTD, thermistor, diode and other sensor types that require constant current biasing. The current source outputs are on pins IDAC1 and IDAC2. The voltage compliance range is governed by the AVDD analog supply (5 V). The currents are individually programmed over the 50 µA to 3000 µA range. As shown in Figure 17, the I_MUX Register controls the connection to the pins.

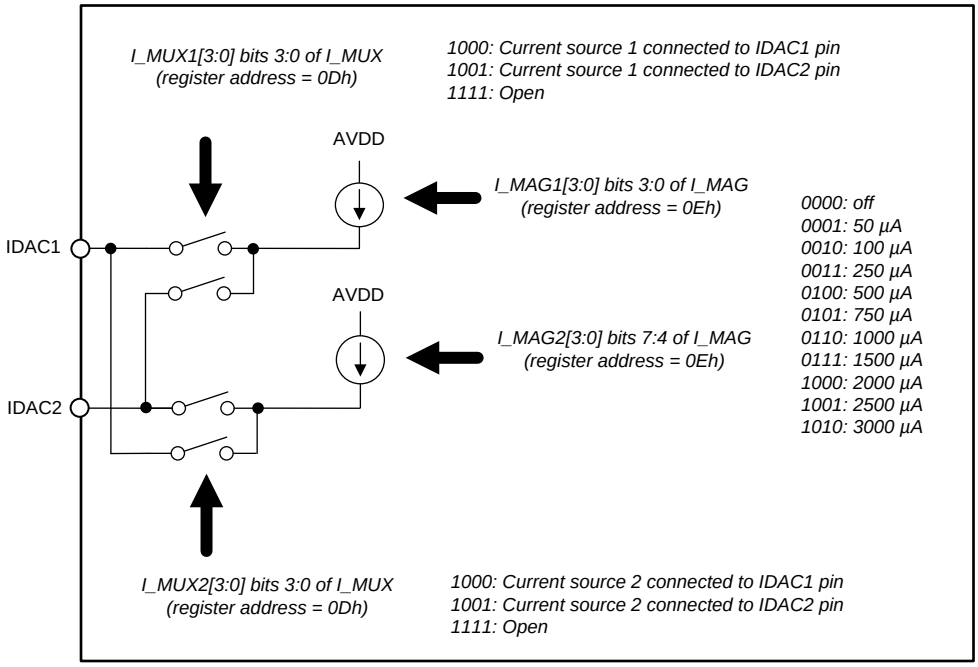

Figure 17. Current Source Output Diagram

Enable the internal voltage reference to operate the current sources. Double the current value or produce an intermediate current value by connecting the current source output pins together. Maintain the compliance voltage of the current sources as specified in Electrical Characteristics.

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8.3.8 General-Purpose Input and Outputs (GPIOs)

The ADS125H02 provides four GPIO pins (GPIO3 through GPIO0), two of which are multiplexed with the external reference REFP1 and REFN1 input pins. The GPIO are digital inputs and outputs with values that are read and written by the GPIO_DAT bits of the MODE3 Register. The GPIO input and output levels are referred to the 5-V analog supply (AVDD and AGND). The input threshold values between values logic 0 and logic 1 is AVDD / 2 (typical). See Figure 18. Bits GPIO_CON[3:0] set the GPIO connection to the designated pin (1 = connect). GPIO_DIR bits program the direction of the GPIO as input (1) or output (0). Bits GPIO_DAT[3:0] are the data values for the GPIO. Observe that if a GPIO pin is programmed as an output, the value read is the register data that is written.

The GPIO provides the output drive signals of the AC-excitation mode. See AC-Excitation Mode.

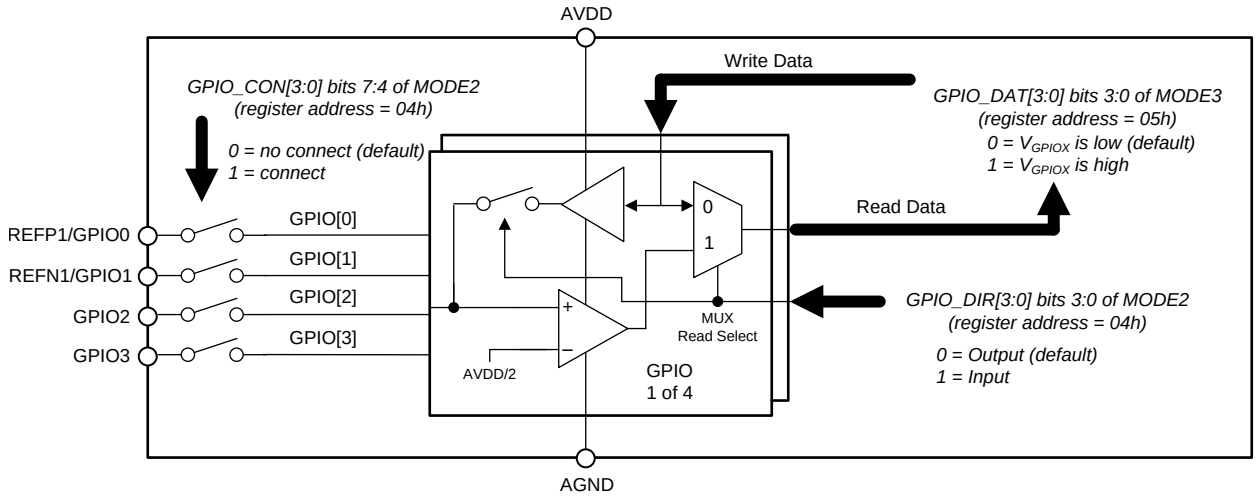

Figure 18. GPIO Block Diagram

8.3.9 ADC Modulator

The modulator is an inherently stable, fourth-order, 2 + 2 pipelined ΔΣ modulator. The modulator samples the analog input voltage at a high sample rate ($f_{MOD} = f_{CLK} / 8$) and converts the analog input to a ones density bit stream for processing by the digital filter.

8.3.10 Digital Filter

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter low-pass filters and decimates the data (data rate reduction), which yields the final data output. By adjusting the type of filtering, tradeoffs are made between resolution, data rate, and line cycle rejection.

The digital filter has two operating modes: sin (x) / x (sinc) mode and finite impulse response (FIR) mode (see the block diagram of Figure 19). The sinc mode provides data rates of 2.5 SPS through 40000 SPS with selectable filter order of sinc1 through sinc5. The FIR filter provides single-cycle settled conversions and simultaneous rejection of 50-Hz and 60-Hz signal interference frequencies with data rates of 2.5 SPS through 20 SPS.

ADVANCE INFORMATION

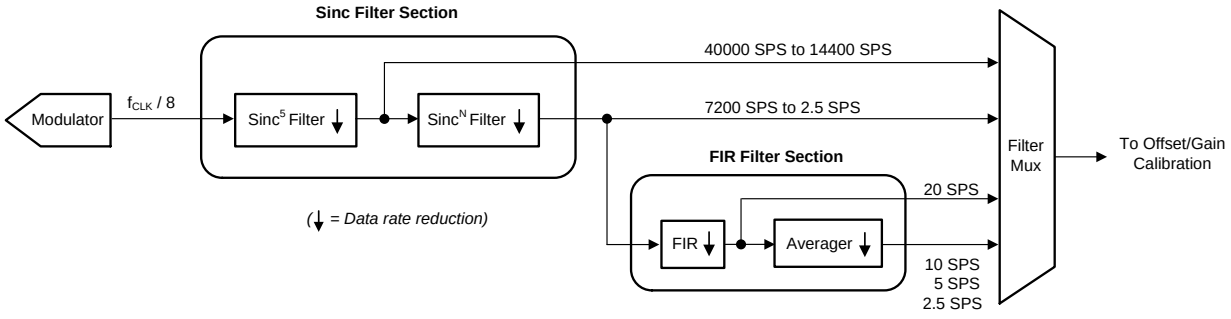

Figure 19. Digital Filter Block Diagram

8.3.10.1 Sinc Filter Mode

The sinc filter consists of two stages: a variable-decimation sinc5 filter followed by a variable-decimation, variable-order sinc filter. The first stage sinc5 filter averages and down-samples the modulator data (f_{CLK} / 8) to produce 40000, 25600, 19200 and 14400 SPS by using decimation ratios of 32, 36, 48, and 64, respectively. These data outputs bypass the second filter stage and as a result have response characteristics of the first-stage sinc5 filter. The second stage receives the first stage output data at 14400 SPS and filters/decimates the data to yield data rates of 7200 SPS to 2.5 SPS. The second stage is a programmable order sinc filter.

The data rate is programmed by the DR[4:0] bits of register MODE0. The filter mode is programmed by the FILTER[2:0] bits of register MODE0 (see Figure 40).

8.3.10.1.1 Sinc Filter Frequency Response

The digital filter reduces noise present in the signal and noise from within the ADC. Adjusting the filter by changing the data rate and filter order changes the filter bandwidth. Through these changes, tradeoffs are made among the filter attributes (noise, bandwidth and conversion latency).

As shown in Figure 20 and Figure 21, the first-stage sinc5 filter has frequency response nulls occurring at N x f_{DATA} = where N = 1, 2, 3 and so on. At the null frequencies, the filter has zero gain.

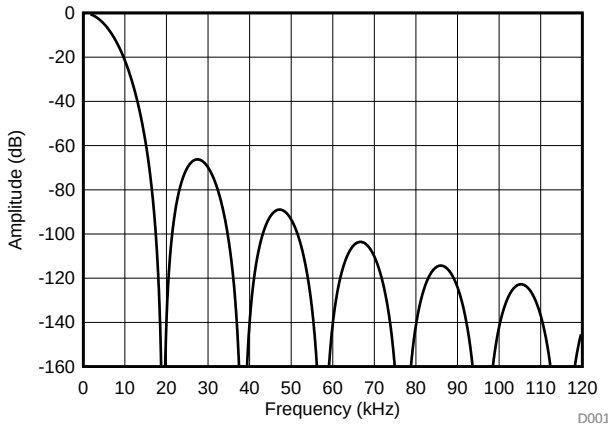

Figure 20. Sinc Frequency Response (19200 SPS)

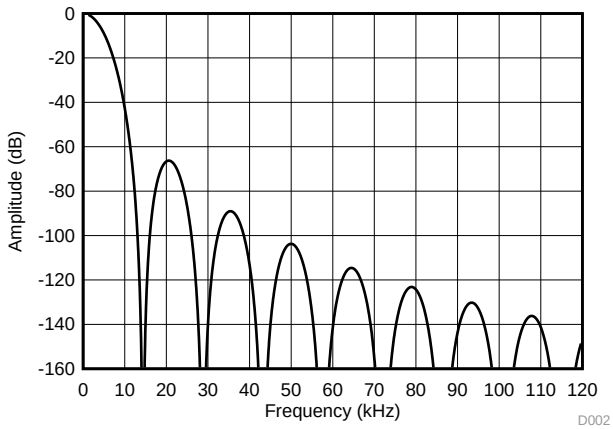

Figure 21. Sinc Frequency Response (14400 SPS)

The second stage superimposes additional nulls to the frequency response with the nulls that are produced by the first stage. The first of the superimposed nulls occur at the output data rate, and by nulls occurring at multiples of the data rate.

Figure 22 shows the frequency response of the combined filter stages at 2400 SPS. This data rate has five equally-spaced nulls residing between the larger nulls at 14400 Hz multiples that are produced by the first stage. This frequency response is similar to that of data rates 2.5 SPS to 7200 SPS. Figure 23 shows the frequency response nulls at 10 SPS.

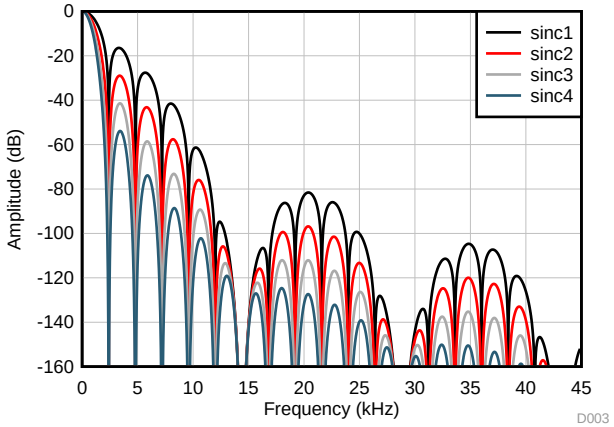

Figure 22. Sinc Frequency Response (2400 SPS)

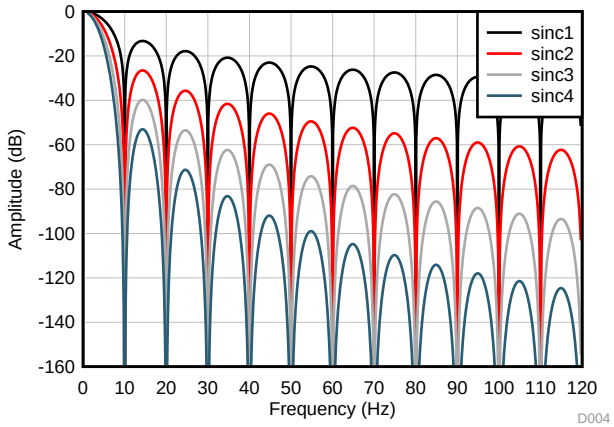

Figure 23. Sinc Frequency Response (10 SPS)

Figure 24 and Figure 25 show the frequency response of data rates 50 SPS and 60 SPS, respectively. The frequency response is plotted to the 50-Hz, 12th harmonic (10th harmonic for 60 Hz). The signal's 50-Hz or 60-Hz fundamental and harmonic noise are reduced by increasing the filter order of the second-stage.

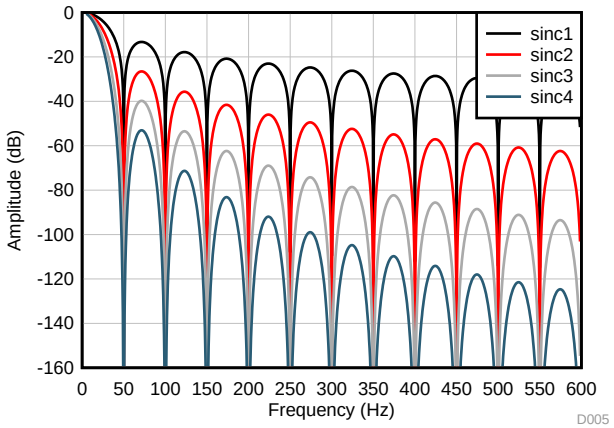

Figure 24. Sinc Frequency Response (50 SPS)

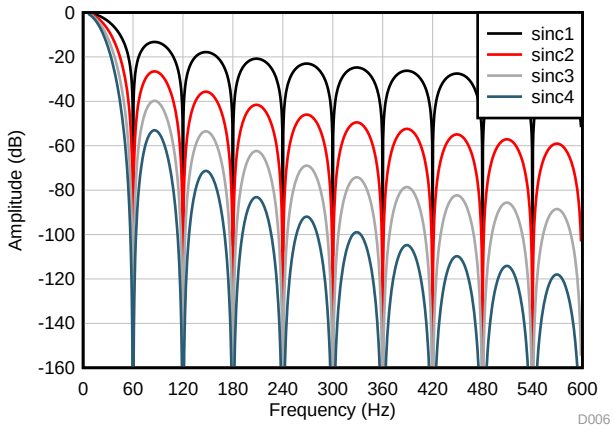

Figure 25. Sinc Frequency Response (60 SPS)

Figure 26 and Figure 27 plot the detailed frequency response of 50-SPS and 60-SPS data rates and show various orders of the sinc filter. The high-order sinc filter increases the frequency width of the null, which improves line cycle rejection. As shown in the plots, the best 50-Hz or 60-Hz rejection occurs using the sinc4 order.

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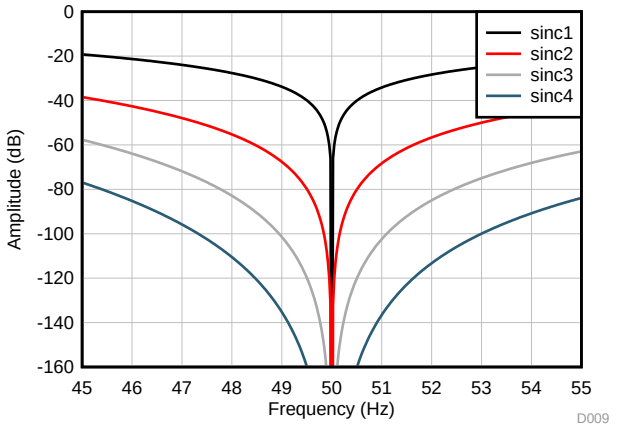

Figure 26. Sinc Frequency Response, Detailed (50 SPS)

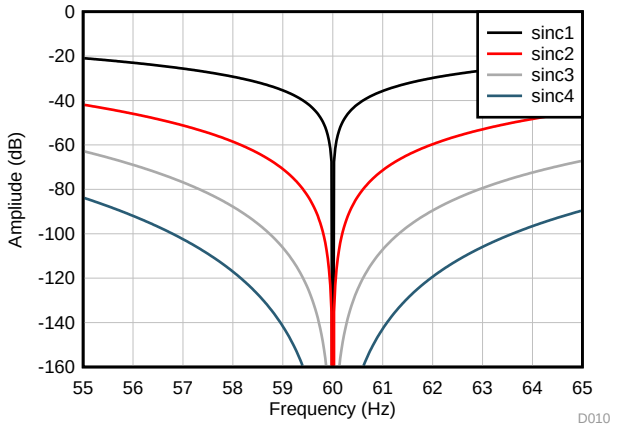

Figure 27. Sinc Frequency Response, Detailed (60 SPS)

The sinc filter has an overall low-pass response that rolls off high-frequency components of the signal. The bandwidth of the filter depends on the output data rate and the order of the output data rate. The overall system bandwidth is the combined responses of the digital filter, the PGA anti-alias filter, and external filters. Table 5 lists the –3-dB bandwidth of the sinc filter. Be aware of the reduced signal bandwidth pertaining to the high-order sinc filters.

Table 5. Sinc Filter Bandwidth

-3-dB BANDWIDTH (Hz)					
DATA RATE (SPS)	SINC1	SINC2	SINC3	SINC4	SINC5
2.5	1.10	0.80	0.65	0.58	—
5	2.23	1.60	1.33	1.15	—
10	4.43	3.20	2.62	2.28	—
16.6	7.38	5.33	4.37	3.80	—
20	8.85	6.38	5.25	4.63	—
50	22.1	16.0	13.1	11.4	—
60	26.6	19.1	15.7	13.7	—
100	44.3	31.9	26.2	22.8	—
400	177	128	105	91.0	—
1200	525	381	314	273	—
2400	1015	751	623	544	—
4800	1798	1421	1214	1077	—
7200	2310	1972	1750	1590	—
14400	—	—	—	—	2940
19200	—	—	—	—	3920
25600	—	—	—	—	5227
40000	—	—	—	—	8167

8.3.10.2 FIR Filter

The finite impulse response (FIR) filter is a coefficient based filter that provides an overall low-pass filter function. The filter provides simultaneous rejection of 50-Hz and 60-Hz line cycle frequencies and harmonics at data rates of 2.5, 5, 10 and 20 SPS. The conversion latency of the FIR filter is a single cycle. (See Table 8 for latency of all filter settings). As shown in Figure 19, the FIR filter section receives data from the second-stage sinc filter at 600 Hz. The FIR filter section decimates by 30 to yield the output data rate of 20 SPS. A first-order variable average (sinc1) yields 10 SPS, 5 SPS, and 2.5 SPS.

As shown in Figure 28 and Figure 29, the FIR filter frequency response has a series of response nulls that are placed close to 50 Hz and 60 Hz. The response nulls repeat near the harmonics of 50 Hz and 60 Hz.

ADVANCE INFORMATION

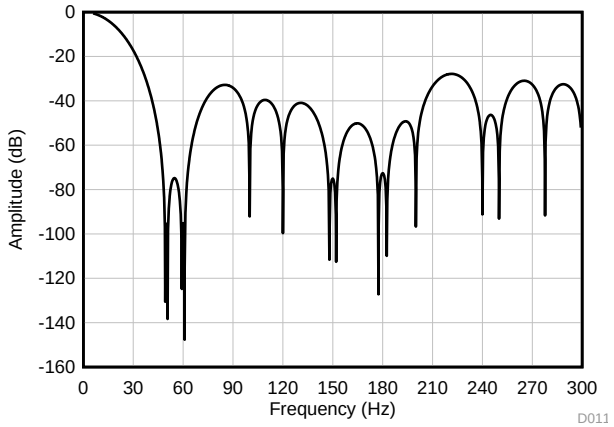

Figure 28. FIR Frequency Response (20 SPS)

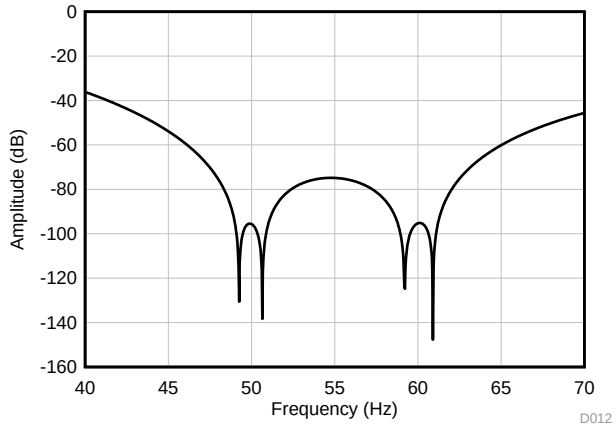

Figure 29. FIR Frequency Response Detail (20 SPS)

Figure 30 shows the FIR filter response at 10 SPS. As a result of the variable average, new frequency nulls are superimposed to the nulls shown in Figure 28. The first of the combined response nulls occur at 10 Hz. Additional nulls occur at folded frequencies around multiples of 20 Hz. The first of the 10 SPS folded null frequencies are seen in Figure 30 at 10 Hz, 30 Hz, 70 Hz, 90 Hz, and so on.

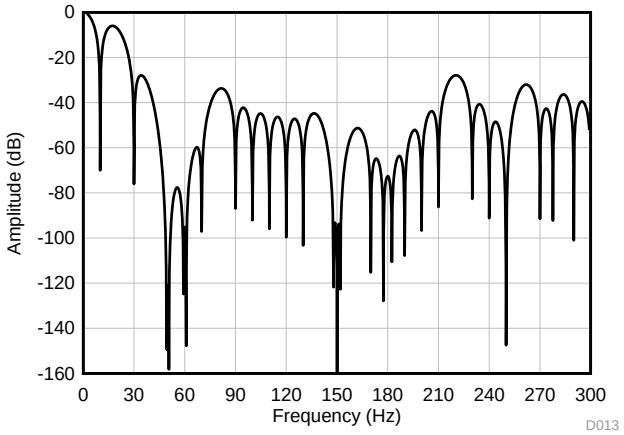

Figure 30. FIR Frequency Response (10 SPS)

Similar to the response of the sinc filter, the overall FIR filter frequency has a low-pass response that rolls off high frequencies. The response is such that the FIR filter limits the bandwidth of the input signal. The signal bandwidth depends on the output data rate. Table 6 lists the –3-dB filter bandwidth of the FIR filter. The total system bandwidth is the combined response of the digital filter, the PGA anti-alias filter, and external filters.

Table 6. FIR Filter Bandwidth

DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)
2.5	1.2
5	2.4
10	4.7
20	13

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8.3.10.3 50-Hz and 60-Hz Normal Mode Rejection

To reduce 50-Hz and 60-Hz noise interference, configure the conversion period to reject the noise at 50 Hz and 60 Hz. 50-Hz and 60-Hz noise rejection depends on the filter type and filter order. Table 7 summarizes the 50-Hz and 60-Hz noise rejection versus data rate and filter type. The table values are based on 2% and 6% tolerance of noise frequency to ADC clock frequency. For the sinc filter mode, 50-Hz and 60-Hz noise rejection is increased by increasing the order of the filter. Common mode noise is also rejected at these frequencies.

Table 7. 50-Hz and 60-Hz Normal Mode Rejection

DIGITAL FILTER AMPLITUDE (dB)					
DATA RATE (SPS)	FILTER TYPE	50 Hz (±2%)	60 Hz (±2%)	50 Hz (±6%)	60 Hz (±6%)
2.5	FIR	–113	–99	–88	–80
2.5	Sinc1	–36	–37	–40	–37
2.5	Sinc2	–72	–74	–80	–74
2.5	Sinc3	–108	–111	–120	–111
2.5	Sinc4	–144	–148	–160	–148
5	FIR	–111	–95	–77	–76
5	Sinc1	–34	–34	–30	–30
5	Sinc2	–68	–68	–60	–60
5	Sinc3	–102	–102	–90	–90
5	Sinc4	–136	–136	–120	–120
10	FIR	–111	–94	–73	–68
10	Sinc1	–34	–34	–25	–25
10	Sinc2	–68	–68	–50	–50
10	Sinc3	–102	–102	–75	–75
10	Sinc4	–136	–136	–100	–100
16.6	Sinc1	–34	–21	–24	–21
16.6	Sinc2	–68	–42	–48	–42
16.6	Sinc3	–102	–63	–72	–63
16.6	Sinc4	–136	–84	–96	–84
20	FIR	–95	–94	–66	–66
20	Sinc1	–18	–34	–18	–24
20	Sinc2	–36	–68	–36	–48
20	Sinc3	–54	–102	–54	–72
20	Sinc4	–72	–136	–72	–96
50	Sinc1	–34	–15	–24	–15
50	Sinc2	–68	–30	–48	–30
50	Sinc3	–102	–45	–72	–45
50	Sinc4	–136	–60	–96	–60
60	Sinc1	–13	–34	–12	–24
60	Sinc2	–27	–68	–24	–48
60	Sinc3	–40	–102	–36	–72
60	Sinc4	–53	–136	–48	–96

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8.4 Device Functional Modes

8.4.1 Conversion Control

The START pin or the START command controls the conversions. If using commands to control conversions, keep the START pin low to avoid contention between the pin and commands. Commands take affect on the 32nd falling SCLK edge. See Switching Characteristics for details on conversion control timing.

The ADC has two conversion control operating modes: continuous-conversion mode and pulse-conversion mode. The continuous-conversion mode performs conversions indefinitely until the user stops the conversions. Pulse-conversion mode performs one conversion and then stops. The CONVRT (bit 4 of the MODE1 Register) programs the mode.

8.4.1.1 Continuous-Conversion Mode

This conversion mode performs continuous conversions until the user stops conversions. To start conversions, take the START pin high or send the START command. $\overline{\text{DRDY}}$ is driven high when the conversion is started. $\overline{\text{DRDY}}$ is driven low when the conversion data are ready. Conversion data is available to read at that time. Take the START pin low or send a STOP command to stop conversions. When conversions are stopped, the conversion in progress runs to completion. To restart a conversion that is in progress, toggle the START pin low-then-high or send a new START command.

8.4.1.2 Pulse-Conversion Mode

In pulse-conversion mode, the ADC performs one conversion when START is taken high or when the START command is sent. When the conversion completes, further conversions stop. The $\overline{\text{DRDY}}$ output is driven high to indicate the conversion is in progress and is driven low when the conversion data are ready. Conversion data is read at that time. To restart a conversion in progress, toggle the START pin low-then-high or send a new START command. Driving START low or sending the stop command does not interrupt the current conversion.

8.4.1.3 Conversion Latency

The digital filter averages data from the modulator to produce the conversion result. The individual stages of the digital filter must have settled data to provide fully-settled output data. The order and the decimation ratio of the digital filter determines the amount of data averaged which affects the latency of the conversion data. The FIR and sinc1 filter modes are zero latency because the ADC provides the conversion result in one conversion cycle. Latency time is an important consideration for data throughput in multiplexed applications.

Table 8 lists the conversion latency values of the ADC. Conversion latency is defined as the time from the start of the *first* conversion by taking the START pin high or sending the start command to when the conversion data is ready. The ADC is designed to provide fully settled data under this condition. The conversion latency values listed in Table 8 include the programmable start-conversion delay = 50 uS before the digital filter starts but does include overhead time for final data processing. After the first conversion completes in continuous conversion mode, the period of the next conversions are equal to 1 / f_{DATA}. The first conversion latency in chop and AC-excitation modes are twice the values listed in Table 8. The period of the next conversions are equal to the values listed in Table 8.

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Device Functional Modes (continued)

Table 8. Conversion Latency

DATA RATE (SPS)	CONVERSION LATENCY ($t_{(STDR)}$ (1) (ms)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	400.4	800.4	1,200	1,600	—	402.2
5	200.4	400.4	600.4	800.4	—	202.2
10	100.4	200.4	300.4	400.4	—	102.2
16.6	60.35	120.4	180.4	240.4	—	—
20	50.35	100.4	150.4	200.4	—	52.22
50	20.35	40.42	60.42	80.42	—	—
60	17.02	33.76	50.42	67.09	—	—
100	10.35	20.42	30.42	40.42	—	—
400	2.855	5.424	7.924	10.42	—	—
1200	1.188	2.091	2.924	3.758	—	—
2400	0.771	1.258	1.674	2.091	—	—
4800	0.563	0.8409	1.049	1.258	—	—
7200	0.494	0.702	0.841	0.980	—	—
14400	—	—	—	—	0.424	—
19200	—	—	—	—	0.337	—
25600	—	—	—	—	0.271	—
40000	—	—	—	—	0.179	—

(1) Chop mode off, conversion-start time delay = 50 µs (DELAY[3:0] = 0001)

If the input signal changes during the conversion phase, the conversion data are a mix of old and new data, as shown in Figure 31. After an input change, the number conversion periods required to provide fully-settled output data are calculated by dividing conversion latency by the nominal period plus one conversion period. In chop mode and AC-excitation modes, use twice the latency values.

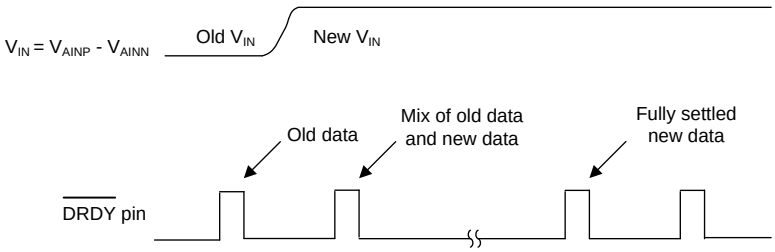

Figure 31. Input Change During Conversions

8.4.1.4 Start-Conversion Delay

At the start of a conversion, the ADC provides a programmable delay to allow for PGA settling or to provide delay for input and configuration changes. The default value is 50 µs. 50 µs provides settling time for the PGA anti-aliasing filter. Use additional delay time as needed to provide settling time of external components. The latency values listed in Table 8 are with start-conversion delay value = 0 µs. As an alternative to this parameter, delay the start of conversion after input and configuration changes.

Start-conversion delay is an important consideration when operating in AC-excitation mode. In this mode, the signal and reference inputs are reversed for each conversion, and as a result, this parameter allows for settling of the PGA anti-alias filter and external filter components. As a general guideline, set the delay time to approximately 15 times the time constant of the signal and reference filters.

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8.4.2 Chop Mode

The PGA and modulator are chopper-stabilized at high frequency to reduce offset voltage, offset voltage drift and 1/f noise. These artifacts are modulated to high frequency and removed by the digital filter. Although chop reduces offset to very low levels, an optional, lower speed chop mode virtually removes all traces of offset errors.

In this mode, the ADC alternates the polarity of consecutive conversions by reversing the input signal. The ADC subtracts the results of two, alternate-phase conversions to yield the final conversion data. The results of subtraction removes the offset. Be aware that chop mode is available only for the AIN0 and AIN1 inputs. See Figure 32 for the chop mode block diagram.

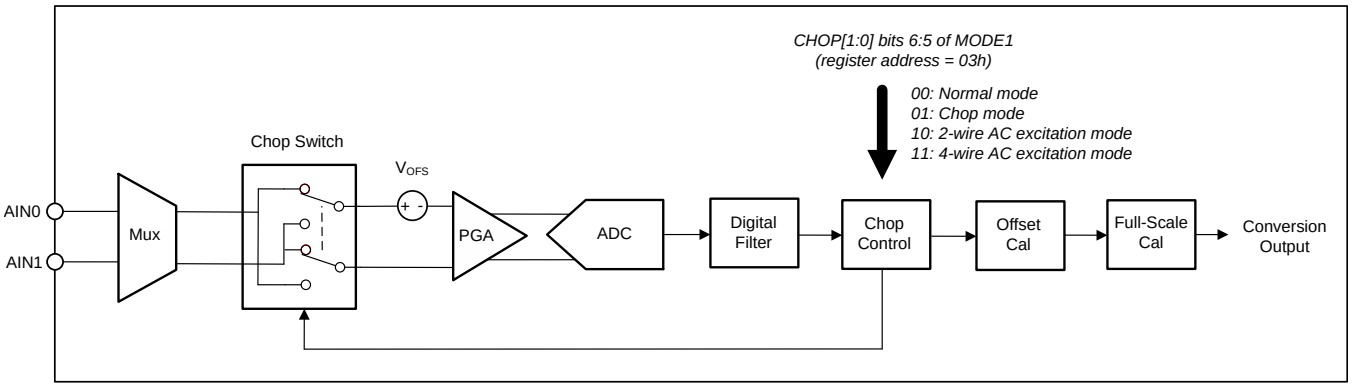

Figure 32. Chop Mode

V_{OFS} models the internal offset voltage. Chop operation is as follows:

Internal Conversion C1: AIN1 – AIN0 + V_{OFS}

(First output withheld)

Internal Conversion C2: AIN0 – AIN1 + V_{OFS}

Output 1 = (C1 – C2) / 2 = AIN1 – AIN0

Internal Conversion C3: AIN1 – AIN0 + V_{OFS}

Output 2 = (C3 – C2) / 2 = AIN1 – AIN0

Internal Conversion C4: AIN0 – AIN1 + V_{OFS}

Output 3 = (C3 – C4) / 2 = AIN1 – AIN0

The sequence repeats for all conversions. Be aware that chop mode changes the normal data rate. The order of the sinc filter determines the new data rate. As Table 8 shows, the new data rate is equal to 1 / latency and the first conversion latency is 2 × latency.

The consequence averaging two data readings in chop reduces noise by $\sqrt{2}$. Divide the noise data in and by 1.4 for the new noise performance data in chop mode. The null frequency(s) of the digital filter response do not change in chop mode. New null frequencies are appear at multiples of f_{DATA} / 2.

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8.4.3 AC-Excitation Mode

There are several methods to provide the excitation supply to a resistive bridge: voltage or current, and DC or AC. AC method can be a sine wave or switched DC voltage or current. Constant DC voltage and is the most common technique. AC excitation in this context refers to reversing the polarity of a DC excitation voltage by the use of external switching components. Similar in operation to chop mode, the result of voltage reversal removes offset voltage from the bridge, including residual offset voltage of the ADC itself. The ADS125H02 provides the signals to drive the external components to reverse the bridge voltage.

The timing of the drive signals is synchronized to the ADC conversion phase. During one conversion phase, the voltage polarity is positive. On the alternate conversion phases the voltage polarity is negative. The ADC compensates the negative polarity by reversing the internal reference voltage. The ADC subtracts the data corresponding to the positive and negative phases to mathematically remove offset voltage from the input.

The ADC output drive signals are non-overlapping to avoid bridge commutation that otherwise can occur during voltage reversal. The AC excitation switching rate is the same as the conversion latency values listed in Table 8. This switch rate avoids unnecessary fast switching. See Figure 6 for output drive timing.

Table 9 shows the AC-excitation drive signals and the associated GPIO pins. Program the AC-excitation mode using the CHOP[1:0] bits in the MODE1 Register. AC excitation is programmed for two-wire or four-wire operation. For two-wire operation, the ADC provides two drive signals. If required, use two external inverters to derive four signals to drive discrete transistors. The GPIO drive levels are referred to the 5-V analog supply. Be aware that AC-excitation mode changes the normal data rate. See Chop Mode for details of the new data rate.

See for operational details.

Table 9. AC-Excitation Drive Pins

DEVICE PIN	GPIO	2-WIRE MODE (CHOP[1:0] = 10)	4-WIRE MODE (CHOP[1:0] = 11)
REFP1/GPIO0	GPIO[0]	$\overline{\text{ACX1}}$	$\overline{\text{ACX1}}$
REFN1/GPIO1	GPIO[1]	$\overline{\text{ACX2}}$	$\overline{\text{ACX2}}$
GPIO2	GPIO[2]		ACX1
GPIO3	GPIO[3]		ACX2

8.4.4 Clock Mode

Operate the ADC with an external clock or with the internal oscillator. For external clock operation, apply the clock signal to CLKIN. The ADC detects the presence of the external clock and selects the clock automatically. The frequency of the external clock depends on the data rate used. See Table 10. Be sure the external clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. For internal clock operation, connect CLKIN to DGND. Be aware of the accuracy of the internal oscillator as shown in Electrical Characteristics. The internal oscillator begins operating immediately at device power-on. Read the CLOCK bit in the STATUS0 Register to verify the clock mode.

Table 10. External Clock vs Data Rate

DATA RATE	CLOCK FREQUENCY
2.5 to 25600 SPS	7.3728 MHz
40000 SPS	10.24 MHz

8.4.5 Reset

The ADC is reset in three ways:

1) Power-on reset

2) $\overline{\text{RESET}}$ pin

3) RESET command

At reset, the serial interface, conversion-control logic, digital filter and register map values are reset. The RESET bit of the STATUS0 Register is set to indicate reset occurs. Clear the bit to detect the next device reset. If the START pin is high after RESET, the ADC begins conversions.

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8.4.5.1 Power-on Reset

At power-on, the ADC is reset and 2^{16} f_{CLK} cycles later is ready for communication after all the supply voltages cross the respective reset voltage thresholds. Until this time, $\overline{DRDY}$ is held low .$\overline{DRDY}$ is then driven high to indicate when ADC communication begins. The conversion cycle starts 512 / f_{CLK} cycle after $\overline{DRDY}$ asserts high. Figure 4 shows the power-on reset behavior.

8.4.5.2 Reset by Pin

Reset the ADC by taking the $\overline{RESET}$ pin low for a minimum four f_{CLK} cycles, and then return the pin high. After reset, the conversion starts 512 / f_{CLK} cycles later. See Figure 5 for RESET pin timing.

8.4.5.3 Reset by Command

Reset the ADC through the serial interface by the RESET command. Toggle $\overline{CS1}$ high-to-low first, to reset the serial interface before sending the command. After reset, the conversion starts 512 / f_{CLK} cycles later. See Figure 5 for reset command timing.

8.4.6 Calibration

The ADC incorporates calibration registers and associated commands to calibrate offset and full-scale errors. Calibrate the ADC by using calibration commands, or calibrate by writing to the calibration registers directly (user calibration). To calibrate by command, send the offset or full-scale calibration commands. To user calibrate, write to the calibration registers with values based on collecting conversion data. Perform offset calibration before full-scale calibration.

8.4.6.1 Offset and Full-Scale Calibration

Use the offset and full-scale (gain) registers to correct offset or full-scale errors, respectively. As shown in Figure 33, the offset calibration register is subtracted from the output data before multiplication by the full-scale register, which is divided by 400000h. After the calibration operation, the final value of the output data is clipped to 24 bits.

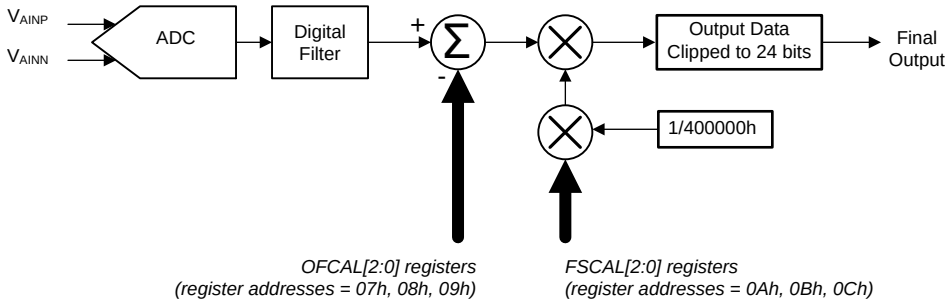

Figure 33. Calibration Block Diagram

Equation 5 shows the internal calibration.

$$\text{Final Output Data} = (\text{Pre Data} - \text{OFCAL}[2:0]) \times \text{FSCAL}[2:0] / 400000h \quad (5)$$

8.4.6.1.1 Offset Calibration Registers

The offset calibration word is 24 bits, consisting of three 8-bit registers, as listed in Table 11. The offset value is subtracted from the conversion result. The offset value is in two's-complement format with a maximum positive value equal to 7FFFFFh and a maximum negative value equal to 800000h. A register value equal to 000000h has no offset correction. Although the calibration registers provide a wide range of offset values, the input signal cannot exceed ±106% of the precalibrated range. Otherwise, the ADC is overranged. Table 12 lists example values of the offset register.

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Table 11. Offset Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
OFCAL0	LSB	07h	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFCAL1	MID	08h	B15	B14	B13	B12	B11	B10	B9	B8
OFCAL2	MSB	09h	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 12. Offset Calibration Register Values

OFCAL[2:0] REGISTER VALUE	OFFSET CALIBRATED OUTPUT VALUE
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h

8.4.6.1.2 Full-Scale Calibration Registers

The full-scale calibration word is 24 bits consisting of three 8-bit registers, as listed in Table 13. The full-scale calibration value is straight binary and normalized to a unity-gain at a value of 400000h. Table 14 lists register values for selected gain factors. Gain errors greater than unity are corrected by full-scale values less than 400000h. Although the calibration registers provide a wide range of possible values, the input signal must not exceed ±106% of the precalibrated input range. Otherwise, the ADC is overranged.

Table 13. Full-Scale Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
FSCAL0	LSB	0Ah	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSCAL1	MID	0Bh	B15	B14	B13	B12	B11	B10	B9	B8
FSCAL2	MSB	0Ch	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 14. Full-Scale Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1
3CCCCCh	0.95

8.4.6.2 Offset Calibration (OFSCAL)

The offset calibration command corrects offset errors. To calibrate offset errors, short the inputs to the ADC or short the inputs to the system. When the command is sent, the ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. When calibration is complete, the ADC performs one conversion using the new calibration value. The new calibration value is written to the offset calibration register.

8.4.6.3 Full-Scale Calibration (GANCAL)

The full-scale calibration command corrects gain errors. To calibrate, apply a positive calibration voltage to the ADC, wait for the signal to settle, and then send the command. The ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. The ADC computes the full-scale calibration value so that the applied calibration voltage is scaled to equal positive full scale output code. The computed result is written to the calibration register. The ADC performs one new conversion using the new calibration value.

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8.4.6.4 Calibration Command Procedure

Use the following calibration procedure using the calibration commands. The register-lock mode must be UNLOCK prior to using the calibration commands. When calibrating at power-on, make sure the reference voltage has stabilized. Perform offset calibration operation prior to full-scale calibration.

1. Select the desired input channel, gain, reference mode and related ADC configurations as required.
2. Apply the appropriate calibration signal (zero or full-scale) to the system inputs.
3. Take the START pin high or send the start command to start conversions. $\overline{\text{DRDY}}$ is driven high.
4. Before the first conversion completes, send the appropriate calibration command. Keep $\overline{\text{CS1}}$ low. Otherwise, the command is cancelled. Do not send other commands during the calibration period.
5. The calibration time depends on the data rate and digital filter mode. See Table 15. $\overline{\text{DRDY}}$ is driven low when calibration is complete. As a result, offset or full-scale calibration registers are updated with new values. New conversion data is available immediately using the new calibration value.

Table 15. Calibration Time (ms)

DATA RATE (SPS)	FILTER MODE (1)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	6801	7601	8401	9201	—	6805
5	3401	3801	4201	4601	—	3405
10	1701	1901	2101	2300	—	1705
16.6	1021	1141	1261	1381	—	—
20	850.7	951	1051	1151	—	854.5
50	340.9	380.9	421	460.9	—	—
60	284.1	317.7	350.9	384.4	—	—
100	170.8	190.9	210.9	230.8	—	—
400	43.27	48.43	53.42	58.41	—	—
1200	14.93	16.72	18.4	20.07	—	—
2400	7.845	8.816	9.643	10.48	—	—
4800	4.302	4.858	5.276	5.692	—	—
7200	3.123	3.534	3.815	4.095	—	—
14400	—	—	—	—	1.941	—
19200	—	—	—	—	1.49	—
25600	—	—	—	—	1.133	—
40000	—	—	—	—	0.738	—

(1) Nominal clock frequency. Chop and AC-excitation modes are disabled.

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8.4.6.5 User Calibration Procedure

To user calibrate, apply the calibration voltage, acquire conversion data, and compute the calibration value. Write the computed value to the corresponding calibration registers. Before starting calibration, preset the offset and full-scale registers to 000000h and 400000h, respectively.

To offset calibrate, short the inputs to the system and average n number of the conversion data. Averaging conversion data reduces noise to increase calibration accuracy. Write the average value of the conversion data to the offset registers.

To gain calibrate using a full-scale calibration signal, temporarily reduce the full scale register 95% to avoid output clipped codes (set FSCAL[2:0] to 3CCCCCh). Acquire n number of conversions and average the conversions to increase calibration accuracy. Compute the full-scale calibration value as shown in Equation 6:

Full-Scale Calibration Value = (Expected Code / Actual Code × 400000h (6)

where

- Expected code = 799998h using full-scale calibration signal and 95% precalibration scale factor

8.5 Programming

8.5.1 Serial Interface

The SPI-compatible serial interface reads conversion data, configuration of registers, and control of the ADC. The CRC is used to validate error-free transmission of input and output data. The serial interface consists of the following control signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT / $\overline{DRDY}$. Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed on SCLK rising edges; data are latched or read on SCLK falling edges. Timing details of the SPI protocol are found in Figure 1 and Figure 2.

8.5.1.1 Chip Select ($\overline{CS1}$ and $\overline{CS2}$)

$\overline{CS1}$ and $\overline{CS2}$ are active-low inputs that enable the device for communication. The device has two serial interfaces, one for the PGA and one for the ADC. The interfaces are selected (active) by asserting the individual chip selects low ($\overline{CS1}$ or $\overline{CS2}$). $\overline{CS1}$ is used to access the device ADC registers, conversion data and to send control commands. $\overline{CS2}$ is used to access the device PGA registers.

The device is designed such that operationally, $\overline{CS1}$ and $\overline{CS2}$ can be combined together to access both ADC or PGA registers. However, when the device is used in environments where high noise levels are present, control $\overline{CS2}$ independently from $\overline{CS1}$ when accessing the PGA registers. That is, assert $\overline{CS1}$ separately low when accessing the ADC registers and assert $\overline{CS2}$ separately low when accessing PGA registers. See Figure 34 for the chip select control options.

Figure 34. Chip Select Control Options

When controlling chip select in either combined or individual control modes, use $\overline{CS1}$ to access conversion data and for ADC control commands. Chip select must be low during the entire data transaction. When chip select is taken high, the serial interfaces reset, SCLK activity is ignored (blocking applicable commands), and if both $\overline{CS1}$ and $\overline{CS2}$ are high, DOUT/$\overline{DRDY}$ enters the high-impedance state. Drive both chip selects high between command operations. The data ready output ($\overline{DRDY}$) remains active independent of the state of chip select.

8.5.1.2 Serial Clock (SCLK)

SCLK is an input that clocks data into and out of the ADC. Output data is updated on the rising edge of SCLK and input data latches on the falling edge of SCLK. Return SCLK low after the data operation is completed. SCLK is a Schmidt-triggered input designed to improve noise immunity. Even though SCLK is noise resistant, keep SCLK noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. Use a series termination resistor at the SCLK drive pin to reduce ringing.

8.5.1.3 Data Input (DIN)

DIN is the ADC serial data input. DIN inputs commands and register data to the ADC. Input data latches on the falling edge of SCLK.

8.5.1.4 Data Output/Data Ready (DOUT/$\overline{DRDY}$)

DOUT/$\overline{DRDY}$ pin is a dual-function output pin. The two functions are data output and conversion-data ready. The functionality changes depending on whether there is a read data operation in progress. During a read data operation, the function of the pin is data output. After the read operation is completed, the function of the pin returns to conversion-data ready. Data is updated on the SCLK rising edge, therefore the user latches the data on the falling edge.

Be aware that $\overline{CS1}$ must be low for DOUT/$\overline{DRDY}$ to provide the data ready function. When both chip selects are high, DOUT/$\overline{DRDY}$ enters the high-impedance mode (tri-state).

ADVANCE INFORMATION

Programming (continued)

8.5.2 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ asserts low to indicate that new conversion data are ready for readback. The operation of $\overline{\text{DRDY}}$ depends on the mode (continuous or pulse) and whether or not the conversion data are retrieved.

8.5.2.1 $\overline{\text{DRDY}}$ in Continuous-Conversion Mode

In continuous-conversion mode, $\overline{\text{DRDY}}$ is driven high when conversions are started and is driven low when conversion data are ready. During data readback, $\overline{\text{DRDY}}$ returns high, which signals completion of the read operation. If the conversion data are not read, $\overline{\text{DRDY}}$ pulses high 16 f_{CLK} cycles prior to the next falling edge.

To read back the current (old) conversion data before the next conversion completes, send the read data command 16 f_{CLK} cycles prior to the next $\overline{\text{DRDY}}$ falling edge. If the readback command is sent *less than* 16 f_{CLK} cycles prior to the $\overline{\text{DRDY}}$ falling edge, *either* old or new conversion data is provided. Whether old or new data provided for readback depends on the timing of the command. In the case that old data are provided, the assertion of $\overline{\text{DRDY}}$ corresponding to the new data is delayed until after the read data operation has completed. In this case, the DRDY bit of the STATUS0 byte is cleared to indicate the old data has been read. In the case that new conversion data are provided, $\overline{\text{DRDY}}$ transitions low with no delay. In this case, the DRDY bit of the STATUS0 byte is set to 1 to indicate new data is read. To ensure readback of new conversion data, wait until $\overline{\text{DRDY}}$ asserts low before starting the data read operation.

8.5.2.2 $\overline{\text{DRDY}}$ in Pulse-Conversion Mode

$\overline{\text{DRDY}}$ is driven high at conversion start and is driven low when the conversion data are ready. $\overline{\text{DRDY}}$ remains low until a new conversion is started.

Figure 35 shows $\overline{\text{DRDY}}$ operation with and without data retrieval in two conversion modes.

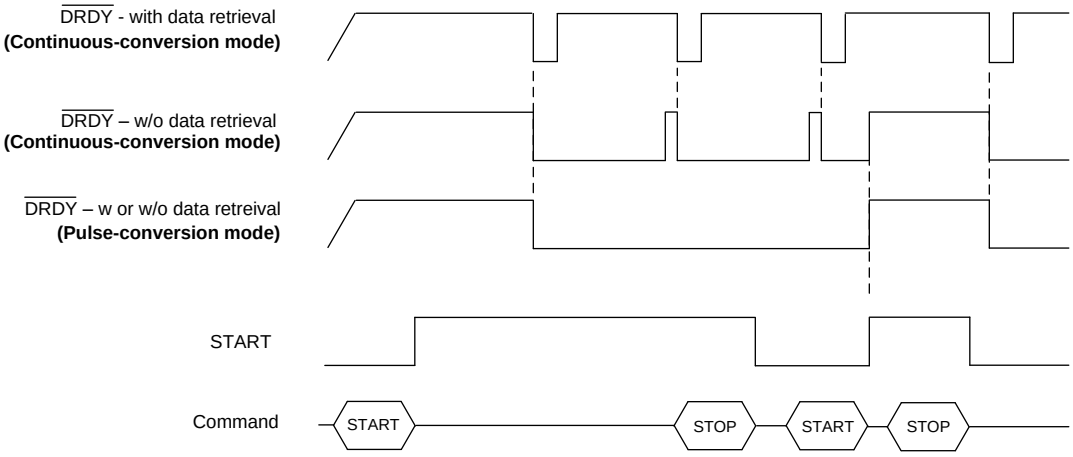

Figure 35. $\overline{\text{DRDY}}$ Operation

8.5.2.3 Data Ready by Software Polling

Software polling of when data is ready is an option to replace hardware polling of $\overline{\text{DRDY}}$. To software poll, read the STATUS0 byte and poll the DRDY bit. In order to not miss conversion data when in free-running operation, poll the bit at least as often as the period of the data rate. If the DRDY bit is set, then conversion data is new since the last data read operation. If the DRDY bit is clear, conversion data is not new since the last data read operation. In this case, the previous conversion data are returned.

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Programming (continued)

8.5.3 Conversion Data

Conversion data are is read by the RDATA command. To read data, take $\overline{CS1}$ low and issue the read data command. The conversion data field consists of an optional STATUS0 byte, three data bytes, and the CRC byte. The CRC byte is computed over the combination of STATUS0 byte and conversion data bytes. See RDATA Command for details to read conversion data.

8.5.3.1 Main Status Byte (STATUS0)

The status byte contains information on the operating state of the ADC. The STATUS0 byte is optionally included with the conversion data by enabling the STATENB bit of the MODE3 Register. Read the STATUS0 Register directly to read status information without the need to read conversion data with the optional embedded status information.

8.5.3.2 Conversion Data Format

The conversion data are 24 bits, in two's-complement format to represent positive and negative values. The data begins with the most significant bit (sign bit) first. The data are scaled so that V_{IN} = 0 V results in an uncalibrated code value of 000000h, positive full scale input is equal to an uncalibrated value of 7FFFFFh and negative full scale input is equal to an uncalibrated code value of 800000h; see Table 16 for the code values. The data are clipped to 7FFFFFh and 800000h during positive and negative signal overdrive, respectively.

Table 16. ADC Conversion Data Codes

DESCRIPTION	INPUT SIGNAL (V)	24-BIT CONVERSION DATA (1)
Positive Full Scale	$\geq V_{REF}$ / Gain × (2^{23} – 1) / 2^{23}	7FFFFFh
1 LSB	V_{REF} / (Gain × 2^{23})	000001h
Zero scale	0	000000h
–1 LSB	$-V_{REF}$ / (Gain × 2^{23})	FFFFFFh
Negative Full Scale	$\leq -V_{REF}$ / Gain	800000h

(1) Ideal (calibrated) output code

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8.5.4 CRC

Cyclic Redundancy Check (CRC) is an error detection byte value that detects communication errors to and from the host and ADC. CRC is the division remainder of the payload data by the prescribed CRC polynomial. The payload data is 1, 2, 3 or 4 bytes depending on the data transfer operation.

The host computes the CRC over the two required command bytes and appends the CRC to the command string (3rd byte). A 4th, zero-value byte completes the command field to the ADC. The ADC performs the CRC calculation and compares the result to the CRC transmitted by the host. If the host and ADC CRC values match, the command executes and the ADC responds by transmitting the valid CRC during the 4th byte of the command. If the operation is data read, the ADC responds with a second CRC that is computed for the requested data byte payload. The response data payload is 1, 3, or 4 bytes depending on the type of operation.

If the host and ADC CRC values *do not* match, the command does not execute and the ADC responds with an *inverted* CRC value, calculated over the received command bytes. The inverted CRC is intended to signal the host of the failed operation. The host terminates transmission of further bytes to stop the command operation. The CRC1ERR bit is set in the STATUS0 Register when a error pertaining to ADC registers occur. STAT12 and CRC2ERR flags are set when an error pertaining to PGA registers occur.

The ADC is ready to accept the next command after all required bytes are transmitted when no CRC error occurs, or after a CRC error occurs when terminated at the end of the 4th command byte.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are: 100000111.

The following is a general procedure to compute the CRC value:

1. Left shift the concatenated one, two, three, or four byte argument (if required) to create a new 40-bit data value (the starting data value). The shifted data is padded with ones to the right of the argument.
2. Align the MSB of the CRC polynomial (100000111) to the left-most, logic-one value of the data.
3. Perform an XOR operation on the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.
4. When the XOR result is less than 100000000b, the procedure ends, yielding the 8-bit CRC value. Otherwise, continue with the XOR operation shown in step 2 using the current data value. The number of loop iterations depends on the value of the initial data.

The following sections detail the input and output data of each command. In the descriptions that follow, these CRC mnemonics apply:

- **CRC-2**: Input CRC of command bytes 1 and 2. Except for WREG command, the value of byte 2 is arbitrary
- **Out CRC-1**: Output CRC of one register data byte
- **Out CRC-2:** Output CRC of two command bytes, inverted value if input CRC error detected
- **Out CRC-3:** Output CRC of three conversion data bytes
- **Out CRC-4:** Output CRC of three conversion data bytes plus STATUS0 byte
- **Echo Byte 1:** Echo of received input byte 1
- **Echo Byte 2:** Echo of received input byte 2

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8.5.5 Commands

Commands are used to read conversion data, control the device, and read and write register data. See Table 17 for the list of commands and the corresponding command byte sequence. Only send the commands that are listed in Table 17. The column labeled *BLOCK* shows the corresponding ADC or PGA block within the device that applies to the commands. $\overline{CS1}$ addresses the ADC register block, $\overline{CS2}$ addresses the PGA register block. See Chip Select ($\overline{CS1}$ and $\overline{CS2}$) for the description of chip select operation. The ADC validates the command operation by the CRC sent from the host. If a CRC error occurs, the ADC rejects the command.

Table 17. Command Byte Summary

MNEMONIC	BLOCK (1)	DESCRIPTION	BYTE 1	BYTE 2 (2)	BYTE 3	BYTE 4
CONTROL COMMANDS						
NOP	ADC, PGA	No operation	00h	Arbitrary	CRC-2	00h
RESET	ADC	Reset	06h	Arbitrary	CRC-2	00h
START	ADC	Start conversion	08h	Arbitrary	CRC-2	00h
STOP	ADC	Stop conversion	0Ah	Arbitrary	CRC-2	00h
READ DATA COMMAND						
RDATA	ADC	Read conversion data	12h	Arbitrary	CRC-2	00h
CALIBRATION COMMANDS						
OFSCAL	ADC	Offset calibration	16h	Arbitrary	CRC-2	00h
GANCAL	ADC	Gain calibration	17h	Arbitrary	CRC-2	00h
REGISTER COMMANDS						
RREG	ADC, PGA	Read register data	20h + rrh (3)	Arbitrary	CRC-2	00h
WREG	ADC, PGA	Write register data	40h + rrh (3)	Register data	CRC-2	00h
PROTECTION COMMANDS						
LOCK	ADC, PGA	Register data lock	F2h	Arbitrary	CRC-2	00h
UNLOCK	ADC, PGA	Register data unlock	F5h	Arbitrary	CRC-2	00h

(1) $\overline{CS1}$ addresses the ADC block. $\overline{CS2}$ addresses the PGA block
(2) Excluding the write-register command, the value of the second byte is arbitrary (any value) but *is* included in the CRC calculation.
(3) rrh = 5-bit register address.

8.5.5.1 General Command Format

The ADC executes the command after transmission of the 4th byte in the sequence. The value of the second command byte is arbitrary but is included in the CRC calculation (two-byte CRC payload). Forcing chip select high before the command has completed results in termination of the command. Figure 36 is an example of the register write operation by writing data to register address 02h (command opcode 42h). The host calculates CRC of the two command bytes. Out CRC-2 byte is the output (ADC calculated) CRC based on the received command bytes. Because the example shows access to register address = 02h which belongs to the ADC register block, take $\overline{CS1}$ low, or optionally, both $\overline{CS1}$ and $\overline{CS2}$ low. The first byte output from the ADC is always 0FFh. The chip select input must be toggled between command operations.

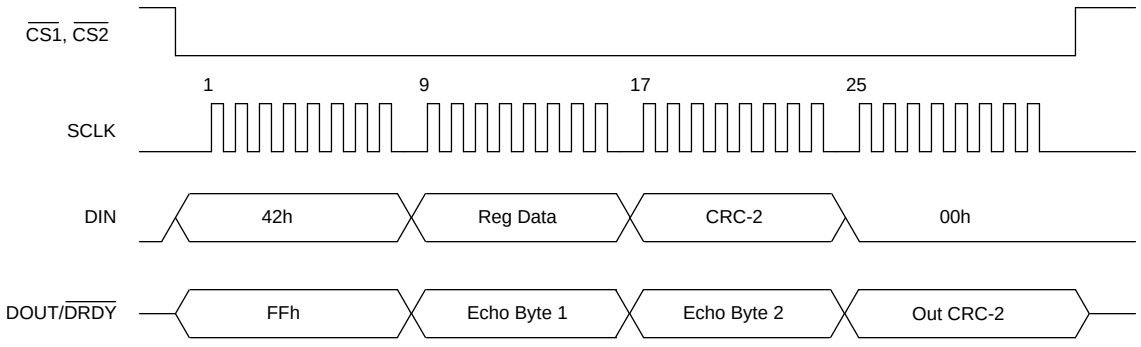

Figure 36. Register Write Command Sequence (Address = 02h)

The following sections detail the input and output byte sequence corresponding to each command. See the CRC section for the notation used for CRC.

8.5.5.2 NOP Command

This command is no operation. Use the NOP command to validate the CRC response byte and error detection without affecting normal operation. Table 18 shows the NOP command byte sequence.

Table 18. NOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	00h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.3 RESET Command

The RESET command resets ADC operation and resets all registers to default. See Reset by Command for details. Table 19 lists the RESET command byte sequence.

Table 19. RESET Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	06h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.4 START Command

This command starts a conversions. See Conversion Control for details. Table 20 lists the START command byte sequence.

Table 20. START Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	08h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.5 STOP Command

This command is used to stop conversions. See Conversion Control for details. Table 21 lists the STOP command byte sequence.

Table 21. STOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	0Ah	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.6 RDATA Command

This command reads conversion data. Because the data are buffered, the data can be read at any time during the conversion sequence. If data is read *near* the completion of the conversion phase, old or new conversion data are returned. See Data Ready ($\overline{\text{DRDY}}$) for details.

The response data of the ADC varies in length depending on inclusion of the optional STATUS0 byte. See Conversion Data Format for details of the format of the conversion data. Figure 37 lists the RDATA command byte sequence that includes the STATUS0 byte.

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Table 22. RDATA Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
DIN	12h	Arbitrary	CRC-2	00h	00h	00h	00h	00h	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	STATUS0 (1)	MSB data	MID data	LSB data	Out CRC-3 or Out CRC-4 (2)

(1) Optional STATUS0 byte shown
(2) Out CRC-4 (4-byte CRC = STATUS0 + data) if STATUS0 byte is included in the data packet

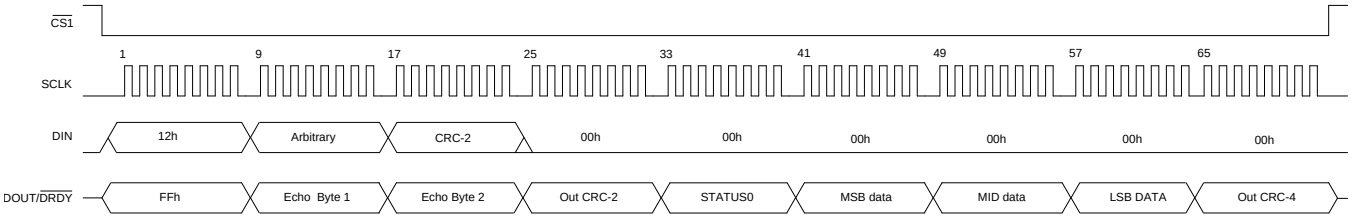

Figure 37. Conversion Data Read Operation

8.5.5.7 OFSCAL Command

This command is used for offset calibration. See Calibration for details. Table 23 lists the OFSCAL command byte sequence.

Table 23. OFSCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	16h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.8 GANCAL Command

This command is used for gain calibration. See Calibration for details. Table 24 lists the GANCAL command byte sequence.

Table 24. GANCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	17h	Arbitrary	CRC-2	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.9 RREG Command

Use the RREG command to read register data. Take $\overline{\text{CS1}}$ low to access registers within the ADC register block. Take $\overline{\text{CS2}}$ low to access registers within the PGA register block (see Register Map for the register block map). Register data are read one byte at a time using the RREG command for each operation. Add the register address (rrh) to the base opcode (20h) to complete the command byte (20h + rrh). Table 25 lists the RREG command byte sequence. The ADC responds with the register data byte, most significant bit first. Data for registers addressed outside the range is 00h. Out CRC-2 is the output CRC corresponding to the received command bytes. Out CRC-1 is the output CRC corresponding to the single register data byte.

Table 25. RREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
DIN	20h + rrh	Arbitrary	CRC-2	00h	00h	00h
DOUT/$\overline{\text{DRDY}}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2	Register data	Out CRC-1

8.5.5.10 WREG Command

Use the WREG command to write register data. Take $\overline{CS1}$ low to access registers within the ADC register block. Take $\overline{CS2}$ low to access registers within the PGA register block (see Register Map for the register block map). The WREG command writes the register data one byte at a time using the WREG command for each operation. Add the register address (rrh) to the base opcode (40h) to complete the command byte (40h + rrh). Table 22 lists the WREG command byte sequence. Writing to certain registers results in conversion restart. Table 29 lists the affected registers. Do not write to registers outside the address range.

Register-write access is enabled and disabled by the UNLOCK and LOCK commands, respectively. The default mode is register UNLOCK. See LOCK Command.

Table 26. WREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	40h + rrh	Register data	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.11 LOCK Command

Use the LOCK command to prevent write operations with unintended data. The ADC register blocks and PGA register blocks are locked and unlocked from write access by assertion of the corresponding chip select. Locking the registers disables register write-access including the calibration registers. The default mode is unlock. Register reads are allowed in LOCK mode. Table 27 lists the LOCK command byte sequence.

Table 27. LOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F2h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.12 UNLOCK Command

Use the UNLOCK command to allow writing register data. The ADC register blocks and PGA register blocks are locked and unlocked from write access by assertion of the corresponding chip select. Register unlock allows register write access including calibration registers. Table 28 lists the UNLOCK command byte sequence.

Table 28. UNLOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F5h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

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8.6 Register Map

The register map consists of 19 single-byte registers. Collectively, the registers are used to configure the ADC to the desired operating mode. Access the registers by using the RREG and WREG commands (register-read and register-write, respectively). Register data are accessed one register byte at a time for each command operation. The register addresses are assigned to either the ADC register block or to the PGA register block. $\overline{CS1}$ selects registers within the ADC register block 1. $\overline{CS2}$ selects registers within the PGA register block. At power-on, the registers reset to default values, as shown in the *Default* column of Table 29. Changing the data of certain registers results in restart of conversions in progress. The *ADC Restart* column in Table 29 lists these registers.

Table 29. Register Map Summary

(rrh)	REGISTER	DEFAULT	RESTART	BLOCK	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	xxh		ADC	DEV_ID[3:0]				REV_ID1[3:0]			
01h	STATUS0	01h		ADC	LOCK1	CRC1ERR	0	STAT12	REFALM	DRDY	CLOCK	RESET
02h	MODE0	24h	Yes	ADC	DR[4:0]				FILTER[2:0]			
03h	MODE1	01h	Yes	ADC	0	CHOP[1:0]		CONVRT	DELAY[3:0]			
04h	MODE2	00h		ADC	GPIO_CON[3:0]				GPIO_DIR[3:0]			
05h	MODE3	00h		ADC	0	STATENB	0	0	GPIO_DAT[3:0]			
06h	REF	05h	Yes	ADC	0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
07h	OFCAL0	00h		ADC	OFC[7:0]							
08h	OFCAL1	00h		ADC	OFC[15:8]							
09h	OFCAL2	00h		ADC	OFC[23:16]							
0Ah	FSCAL0	00h		ADC	FSC[7:0]							
0Bh	FSCAL1	00h		ADC	FSC[15:8]							
0Ch	FSCAL2	40h		ADC	FSC[23:16]							
0Dh	I_MUX	FFh		ADC	I_MUX2[3:0]				I_MUX1[3:0]			
0Eh	I_MAG	00h		ADC	I_MAG2[3:0]				I_MAG1[3:0]			
0Fh	RESERVED	00h		ADC	00h							
10h	MODE4	50h		PGA	0	MUX[2:0]			GAIN[3:0]			
11h	STATUS1	xxh		PGA	PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
12h	STATUS2	0xh		PGA	0	0	LOCK2	CRC2ERR	REV_ID2[3:0]			

8.6.1 Device Identification (ID) Register (address = 00h) [reset = xxh]

ID is shown in Figure 38 and described in Table 30.

Return to Register Map Summary.

Figure 38. ID Register (1)(2)

7	6	5	4	3	2	1	0
DEV_ID[3:0]				REV_ID1[3:0]			
R-xh				R-xh			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset
(2) Reset values are dependent on the device.

Table 30. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DEV_ID[3:0]	R	xh	**Device ID** 0100: ADS125H01 0110: ADS125H02
3:0	REV_ID1[3:0]	R	xh	**Revision ID1** *There are two revision ID fields: REV_ID1 and REV_ID2. The revision IDs can change without notification*

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8.6.2 Main Status (STATUS0) Register (address = 01h) [reset = 01h]

STATUS0 is shown in Figure 39 and described in Table 31.

Return to Register Map Summary.

Figure 39. STATUS0 Register (1)

7	6	5	4	3	2	1	0
LOCK1	CRC1ERR	0	STAT12	REFALM	DRDY	CLOCK	RESET
R-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-xh	R/W-1h

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOCK1	R	0h	**ADC Register Block Lock1 Status** This bit indicates the lock status of the ADC section register block. Writes to the ADC register block are locked by the LOCK command and unlocked by the UNLOCK command. 0: ADC section registers not locked (default) 1: ADC section registers block locked See Table 44 for the PGA section of the register block status
6	CRC1ERR	R/W	0h	**ADC Register Block CRC1 Error** Indicates CRC1 error to commands addressing the ADC block of the device. Write 0 to clear the CRC1 error. 0: No CRC1 error to ADC block of device 1: CRC1 error to the ADC block of the device See Table 44 for the PGA section CRC error status
5	0	R	0h	**Reserved** Always write 0.
4	STAT12	R	0h	**STAT12 Error Flag** Indicates one or more error bits are logged to the PGA error registers STATUS1 or STATUS2. Read the STATUS1 and STATUS2 registers to determine the source of the error. This bit clears after the errors are cleared. 0: No error 1: Error logged to the STATUS1 or STATUS2 registers
3	REFALM	R	0h	**Reference Alarm** This alarm is set if the reference voltage is < 0.4 V. The alarm updates at each new conversion cycle (auto-reset). 0: No reference low alarm 1: Reference low alarm
2	DRDY	R	0h	**Data Ready** Indicates new conversion data. 0: Conversion data **not new** since the last data read 1: Conversion data **new** since the last data read
1	CLOCK	R	xh	**Clock** Indicates internal or external clock mode. The ADC automatically selects the clock mode. 0: ADC clock is internal 1: ADC clock is external
0	RESET	R/W	1h	**Reset** Indicates ADC reset has occurred. Clear the bit to detect the next device reset. 0: No reset 1: Reset (default)

ADVANCE INFORMATION

8.6.3 Mode 0 (MODE0) Register (address = 02h) [reset = 24h]

MODE0 is shown in Figure 40 and described in Table 32.

Return to Register Map Summary.

Figure 40. MODE0 Register (1)

7	6	5	4	3	2	1	0
DR[4:0]					FILTER[2:0]		
R/W-4h					R/W-4h		

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. MODE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	DR[4:0]	R/W	4h	**Data Rate** Select the data rate 00000: 2.5 SPS 00001: 5 SPS 00010: 10 SPS 00011: 16.$\overline{6}$ SPS 00100: 20 SPS (default) 00101: 50 SPS 00110: 60 SPS 00111: 100 SPS 01000: 400 SPS 01001: 1200 SPS 01010: 2400 SPS 01011: 4800 SPS 01100: 7200 SPS 01101: 14400 SPS 01110: 19200 SPS 01111: 25600 SPS 10000 - 11111: 40000 SPS (f_{CLK} = 10.24 MHz)
2:0	FILTER[2:0]	R/W	4h	**Digital Filter (See Digital Filter)** Select the digital filter mode 000: sinc1 001: sinc2 010: sinc3 011: sinc4 100: FIR (default) 101 -111: Reserved

ADVANCE INFORMATION

8.6.4 Mode 1 (MODE1) Register (address = 03h) [reset = 01h]

MODE1 is shown in Figure 41 and described in Table 33.

Return to Register Map Summary.

Figure 41. MODE1 Register (1)

7	6	5	4	3	2	1	0
0	CHOP[1:0]		CONVRT	DELAY[3:0]			
R/W-0h	R/W-0h		R/W-0h	R/W-1h			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0
6:5	CHOP[1:0]	R/W	0h	**Chop and AC-Excitation Modes** Select the Chop or ac-excitation operating modes. See Chop Mode and AC-Excitation Mode. 00: Normal mode (default) 01: Chop mode 10: 2-wire AC-excitation mode (ADS125H02 only) 11: 4-wire AC-excitation mode (ADS125H02 only)
4	CONVRT	R/W	0h	**Conversion Mode** Select the ADC conversion mode. See Conversion Control 0: Continuous conversions (default) 1: Pulse (one shot) conversion
3:0	DELAY[3:0]	R/W	1h	**Conversion Start Delay** Program the time delay at conversion start. See Start-Conversion Delay 0000: 0 us (not for 25600 SPS or 40000 SPS operation) 0001: 50 µs (default) 0010: 59 µs 0011: 67 µs 0100: 85 µs 0101: 119 µs 0110: 189 µs 0111: 328 µs 1000: 605 µs 1001: 1.16 ms 1010: 2.27 ms 1011: 4.49 ms 1100: 8.93 ms 1101: 17.8 ms 1110 - 1111: Reserved

ADVANCE INFORMATION

8.6.5 Mode 2 (MODE2) Register (address = 04h) [reset = 00h]

MODE2 is shown in Figure 42 and described in Table 34.

Return to Register Map Summary.

Figure 42. MODE2 Register (1)

7	6	5	4	3	2	1	0
GPIO_CON[3:0]				GPIO_DIR[3:0]			
R/W-0h				R/W-0h			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. MODE2 Register Field Descriptions (1)

Bit	Field	Type	Reset	Description
7	GPIO_CON[3]	R/W	0h	**GPIO[3] Pin Connection** Connect GPIO[3] to pin GPIO3 0: GPIO[3] not connected to GPIO3 (default) 1: GPIO[3] connected to GPIO3
6	GPIO_CON[2]	R/W	0h	**GPIO[2] Pin Connection** Connect GPIO[2] to pin GPIO2 0: GPIO[2] not connected to GPIO2 (default) 1: GPIO[2] connected to GPIO2
5	GPIO_CON[1]	R/W	0h	**GPIO[1] Pin Connection** Connect GPIO[1] to pin REFN1/GPIO1 0: GPIO[1] not connected to REFN1/GPIO1 (default) 1: GPIO[1] connected to REFN1/GPIO1
4	GPIO_CON[0]	R/W	0h	**GPIO[0] Pin Connection** Connect GPIO[0] to pin REFP1/GPIO0 0: GPIO[0] not connected to REFP1/GPIO0 (default) 1: GPIO[0] connected to REFP1/GPIO0
3	GPIO_DIR[3]	R/W	0h	**GPIO[3] Pin Direction** Configure GPIO[3] as a GPIO input or GPIO output to pin GPIO3 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	GPIO_DIR[2]	R/W	0h	**GPIO[2] Pin Direction** Configure GPIO[2] as a GPIO input or GPIO output to pin GPIO2 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	GPIO_DIR[1]	R/W	0h	**GPIO[1] Pin Direction** Configure GPIO[1] as a GPIO input or GPIO output to pin REFN1/ GPIO1 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	GPIO_DIR[0]	R/W	0h	**GPIO[0] Pin Direction** Configure GPIO[0] as a GPIO input or GPIO output to pin REFP1/GPIO0 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

(1) ADS125H02 only

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8.6.6 Mode 3 (MODE3) Register (address = 05h) [reset = 00h]

MODE3 is shown in Figure 43 and described in Table 35.

Return to Register Map Summary.

Figure 43. MODE3 Register (1)

7	6	5	4	3	2	1	0
0	STATENB	0	0	GPIO_DAT[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. MODE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0h
6	STATENB	R/W	0h	**STATUS0 Byte Enable** Enable the STATUS0 byte for inclusion during conversion data read operation 0: Exclude STATUS0 byte during conversion data read (default) 1: Include STATUS0 byte during conversion data read
5,4	0	R/W	0h	**Reserved** Always write 0h
3	GPIO_DAT[3]	R/W	0h	**GPIO[3] Data (1)** Read or write the GPIO data on pin GPIO3 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	GPIO_DAT[2]	R/W	0h	**GPIO[2] Data (1)** Read or write the GPIO data on pin GPIO2 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	GPIO_DAT[1]	R/W	0h	**GPIO[1] Data (1)** Read or write the GPIO data on pin REFN1/GPIO1 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	GPIO_DAT[0]	R/W	0h	**GPIO[0] Data (1)** Read or write the GPIO data on pin REFP1/GPIO0 0: GPIO[0] is low (default) 1: GPIO[0] is high

(1) ADS125H02 only

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8.6.7 Reference Configuration (REF) Register (address = 06h) [reset = 05h]

REF is shown in Figure 44 and described in Table 36.

Return to Register Map Summary.

Figure 44. REF Register (1)

7	6	5	4	3	2	1	0
0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-1h	

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	0	R/W	0h	**Reserved** Always write 0h
4	REFENB	R/W	0h	**Internal Reference Enable** Enable the Internal reference 0: Internal reference disabled (default) 1: Internal reference enabled
3:2	RMUXP[1:0]	R/W	1h	**Reference Positive Input (See Reference Voltage)** Select the positive reference input 00: Internal reference positive 01: AVDD (default) 10: REFP0 external 11: REFP1/GPIO0 external (1)
1:0	RMUXN[1:0]	R/W	1h	**Reference Negative Input (See Reference Voltage)** Select the negative reference input 00: Internal reference negative 01: AGND (default) 10: REFN0 external 11: REFN1/GPIO1 external (1)

(1) ADS125H02 only

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8.6.8 Offset Calibration (OFCALx) Registers (address = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

OFCALx is shown in Figure 45 and described in Table 37.

Return to Register Map Summary.

Figure 45. OFCAL0, OFCAL1, OFCAL2 Registers (1)

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. OFCAL0, OFCAL1, OFCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration** These three registers are the 24-bit offset calibration word. The offset calibration is in two's-complement data format. The offset value is subtracted from the conversion result before the full-scale operation.

8.6.9 Full-Scale Calibration (FSCALx) Registers (address = 0Ah, 0Bh, 0Ch) [reset = 00h, 00h, 40h]

FSCALx is shown in Figure 46 and described in Table 38.

Return to Register Map Summary.

Figure 46. FSCAL0, FSCAL1, FSCAL2 Registers (1)

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSCAL[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSCAL[23:16]							
R/W-40h							

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. FSCAL0, FSCAL1, FSCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	FSCAL[23:0]	R/W	400000h	**Full-Scale Calibration** These three registers are the 24-bit full scale calibration word. The full-scale calibration is in straight binary data format. The full-scale value is divided by 400000h and multiplied with the conversion data. The scaling operation occurs after the offset operation.

8.6.10 Current Source Multiplexer (I_MUX) Register (address = 0Dh) [reset = FFh]

I_MUX is shown in Figure 47 and described in Table 39.

Return to Register Map Summary.

Figure 47. I_MUX Register (1)

7	6	5	4	3	2	1	0
I_MUX2[3:0]				I_MUX1[3:0]			
R/W-Fh				R/W-Fh			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. I_MUX Register Field Descriptions (1)

Bit	Field	Type	Reset	Description
7:4	I_MUX2[3:0]	R/W	Fh	**Current Source 2 Output Multiplexer** Select IDAC2 pin connection 0000 - 0111: No connection 1000: Connect current source 2 to pin IDAC1 1001: Connect current source 2 to pin IDAC2 1010 -1111: No connection (default = 1111)
3:0	I_MUX1[3:0]	R/W	Fh	**Current Source 1 Output Multiplexer** Select IDAC1 pin connection 0000 - 0111: No connection 1000: Connect current 1 to pin IDAC1 1001: Connect current 1 to pin IDAC2 1010 - 1111: No connection (default = 1111)

(1) ADS125H02 only

8.6.11 Current Source Magnitude (I_MAG) Register (address = 0Eh) [reset = 00h]

I_MAG is shown in Figure 48 and described in Table 40.

Return to Register Map Summary.

Figure 48. I_MAG Register (1)

7	6	5	4	3	2	1	0
I_MAG2[3:0]				I_MAG1[3:0]			
R/W-0h				R/W-0h			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. I_MAG Register Field Descriptions (1)

Bit	Field	Type	Reset	Description
7:4	I_MAG2[3:0]	R/W	0h	**Current Source 2 Magnitude** Select current source 2 magnitude 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011 - 1111: Off
3:0	I_MAG1[3:0]	R/W	0h	**Current Source 1 Magnitude** Select current source 1 magnitude 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011 - 1111: Off

(1) ADS125H02 only

8.6.12 Reserved (RESERVED) Register (address = 0Fh) [reset = 00h]

RESERVED is shown in Figure 49 and described in Table 41.

Return to Register Map Summary.

Figure 49. RESERVED Register (1)

7	6	5	4	3	2	1	0
00h							
R/W-00h							

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	0	R	0h	**Reserved bits** Always write 00h

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8.6.13 MODE4 (MODE4) Register (address = 10h) [reset = 50h]

MODE4 is shown in Figure 50 and described in Table 42.

Return to Register Map Summary.

Figure 50. MODE4 Register (1)

7	6	5	4	3	2	1	0
0	MUX[2:0]			GAIN[3:0]			
R/W-0h	R/W-5h			R/W-0h			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. MODE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0h	**Reserved** Always write 0h
6:4	MUX[2:0]	R/W	5h	**Input Multiplexer** Input multiplexer control 000: AIN1 – AIN0 001: AIN0 – AIN1 (reserved for use with final silicon) 010: AIN1 – AINCOM 011: AIN0 – AINCOM 100: HV supply readback (HV_AVDD – HV_AVSS) / 36 101: Internal short to V_{COM} (HV_AVDD + HV_AVSS) / 2 (default) 110: Temperature sensor reading 111: Reserved
3:0	GAIN[3:0]	R/W	0h	**PGA Gain** PGA gain setting 0000: 0.125 V/V (default) 0001: 0.1875 V/V 0010: 0.25 V/V 0011: 0.5 V/V 0100: 1 V/V 0101: 2 V/V 0110: 4 V/V 0111: 8 V/V 1000: 16 V/V 1001: 32 V/V 1010: 64 V/V 1011: 128 V/V 1100 - 1111: reserved

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8.6.14 PGA Alarm (STATUS1) Register (address = 11h) [reset = xxh]

STATUS1 is shown in Figure 51 and described in Table 43.

Return to Register Map Summary.

Figure 51. STATUS1 Register (1)

7	6	5	4	3	2	1	0
PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
R-xxh							

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGA_ONL	R	xh	**PGA Output Negative Low Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
6	PGA_ONH	R	xh	**PGA Output Negative High Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
5	PGA_OPL	R	xh	**PGA Output Positive Low Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
4	PGA_OPH	R	xh	**PGA Output Positive High Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
3	PGA_INL	R	xh	**PGA Input Negative Low Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
2	PGA_INH	R	xh	**PGA Input Negative High Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
1	PGA_IPL	R	xh	**PGA Input Positive Low Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active
0	PGA_IPH	R	xh	**PGA Input Positive High Alarm** The bit is cleared on register read (clear-on-read) 0: No alarm 1: Alarm active

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8.6.15 Status 2 (STATUS2) Register (address = 12h) [reset = 0xh]

STATUS2 is shown in Figure 52 and described in Table 44.

Return to Register Map Summary.

Figure 52. STATUS2 Register (1)

7	6	5	4	3	2	1	0
0	0	LOCK2	CRC2ERR	REV_ID2[3:0]			
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-xh			

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	0	R/W	0h	**Reserved** Always write 0
5	LOCK2	R	0h	**PGA Register Block Lock2 Status** This bit indicates the lock status of the PGA section of the register block. Writes to the PGA register block are locked by the LOCK command and unlocked by the UNLOCK command. 0: PGA registers not locked (default) 1: PGA registers block locked See Table 31 for the ADC section of the register block status
4	CRC2ERR	R/W	0h	**CRC2 Error** Indicates a CRC2 error to the PGA section of the device. CRC2 error is latched until cleared by the user. Write 0 to clear the error. 0: No error 1: CRC2 error
3:0	REV_ID2[3:0]	R	x	**Revision ID2** *Revision ID 2 field. The revision ID1 and ID2 can change without notification.*

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Range

Linear operation of the PGA requires that the maximum and minimum input signal voltage is not exceeded. The following example shows how to verify the ADC input range specification. For this example, the input signal is ±10 V with 15% overrange. The negative input lead of the sensor is connected to AGND. The ADC gain is 0.1875 V/V using a 2.5-V reference voltage and ±15 V power supplies with 5% tolerance. The summary of conditions to verify the ADC range are:

- $V_{(AINx\_MAX)}$ = 11.5 V
- $V_{(AINx\_MIN)}$ = –11.5 V
- $V_{(AINCOM)}$= AGND
- HV_AVDD = 14.25 V
- HV_AVSS = –14.25 V
- Gain = 0.1875
- V_{REF} = 2.5 V

Evaluation of Equation 4, (case of gain < 1) results in:

–11.75 V < –11.5 V and 11.5 V < **11.75 V**

The inequality is satisfied, and as a result, the absolute input voltage is within the ADC input range requirement.

9.1.2 Input Overload

Observe the input overvoltage precautions as shown in the ESD Diodes section. If an overvoltage condition occurs on an unused channel, the overvoltage channel may crosstalk to the measurement channel. One solution is to externally clamp the inputs with low-forward voltage diodes as shown in Figure 53. The external diodes shunt the overvoltage current flow around the ADC inputs. Be aware of the reverse leakage current that can cause measurement errors.

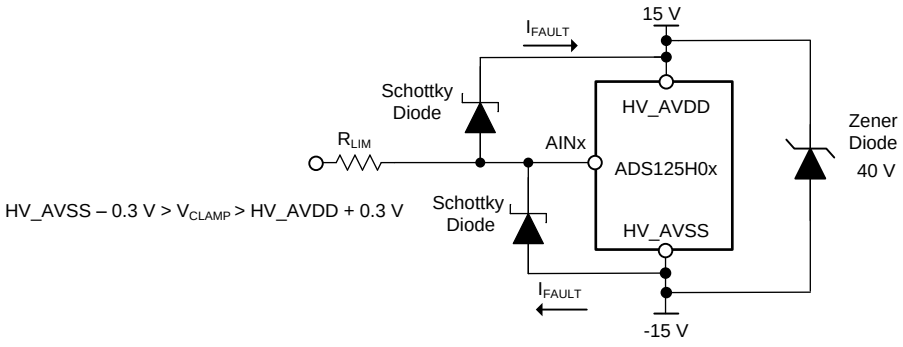

Figure 53. Optional Diode Clamps

Application Information (continued)

9.1.2.1 Input dV/dt

Use an RC filter on the device inputs to limit the signal dV/dt at the ADC inputs. Filtering the dV/dt of the signal prevents transient turn-on the amplifier''s protection diodes.

9.1.3 Unused Inputs and Outputs

- **Analog Input**
  To minimize input leakage current of the measurement channel, connect the unused input to HV_AVDD. Be sure to connect unused reference inputs to AVDD, and do not connect to the HV power supplies.
- **Analog Outputs**
  REFOUT does not require a capacitor if the internal reference is not used. Otherwise, REFOUT requires the 10-µF capacitor that connects to AGND.
- **Digital I/O**
  Not all connections to the digital I/O are required. All unused digital inputs must be tied high or low to DVDD or DGND, as appropriate. Do not float (tri-state) the digital inputs or power supply leakage current can occur. The following is a summary of digital I/O with optional connections:
  - **CLKIN:** Tie CLKIN low to operate the ADC using the internal oscillator. Connect to a clock source for external clock operation.
  - **START:** Tie START low to control conversions by command. Tie START high to free-run conversions.
  - **RESET:** Tie RESET high if desired. The ADC is reset at power on and is reset by the RESET command.
  - **DRDY:** The data ready function is provided by the DOUT/DRDY pin. This functionality is only available when CS1 is low. Alternatively, data ready is determined by software polling of the DRDY bit within the STATUS0 byte. Leave DRDY disconnected when using either method.
- **GPIO**
  Program unused GPIO as outputs. If GPIO is programmed as inputs, the GPIO must not be allowed to float or power supply leakage current may result.

9.2 Typical Application

Figure 54 shows an circuit example of a ±10 V analog input PLC module utilizing the ADS125H02. The ±10 V input signal from the field transmitter is first clamped by external ESD diodes to help protect the ADC inputs. The positive input signal is connected to the ADC input AIN1 through an RC filter to help filter RFI interference that may be picked up in noisy environments. The resistor also acts to limit input current in the event of an overvoltage or during loss of module power when the signal is present. The negative input signal is connected to input AIN0, which is also connected to AGND.

The ADC is programmed to measure between inputs AIN1 and AIN0. This input configuration allows the input voltage to swing 10 V to –10 V above and below AGND. In this example, the high voltage ADC power supply voltage is ±15 V. ±15 V power supply operation allows an input signal headroom of up to ±12.5 V. Using reference voltage = 2.5 V and gain = 0.1875, yields a nominal lull scale input range = ±13.3 V, except as limited by the input signal headroom.

If the internal reference is used, connect a 10-µF capacitor to the REFOUT as shown. Otherwise, apply an external reference to pins REFP0 and REFN0. A 100-kΩ resistor biases the differential reference voltage to 0 V in the event the reference fails. The resistor allows the ADC to detect a failed or missing reference voltage condition.

The excitation current sources and GPIO are not used in this example and are left unconnected.

The ADC internal clock is activated by connecting the CLKIN input pin to ground. The serial interface and ADC control lines are connected the host.

The zener diode clamps the high-voltage supply (HV_AVDD - HV_AVSS) to 40 V to provide protection to the ADC from possible over-voltage supply conditions.

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Typical Application (continued)

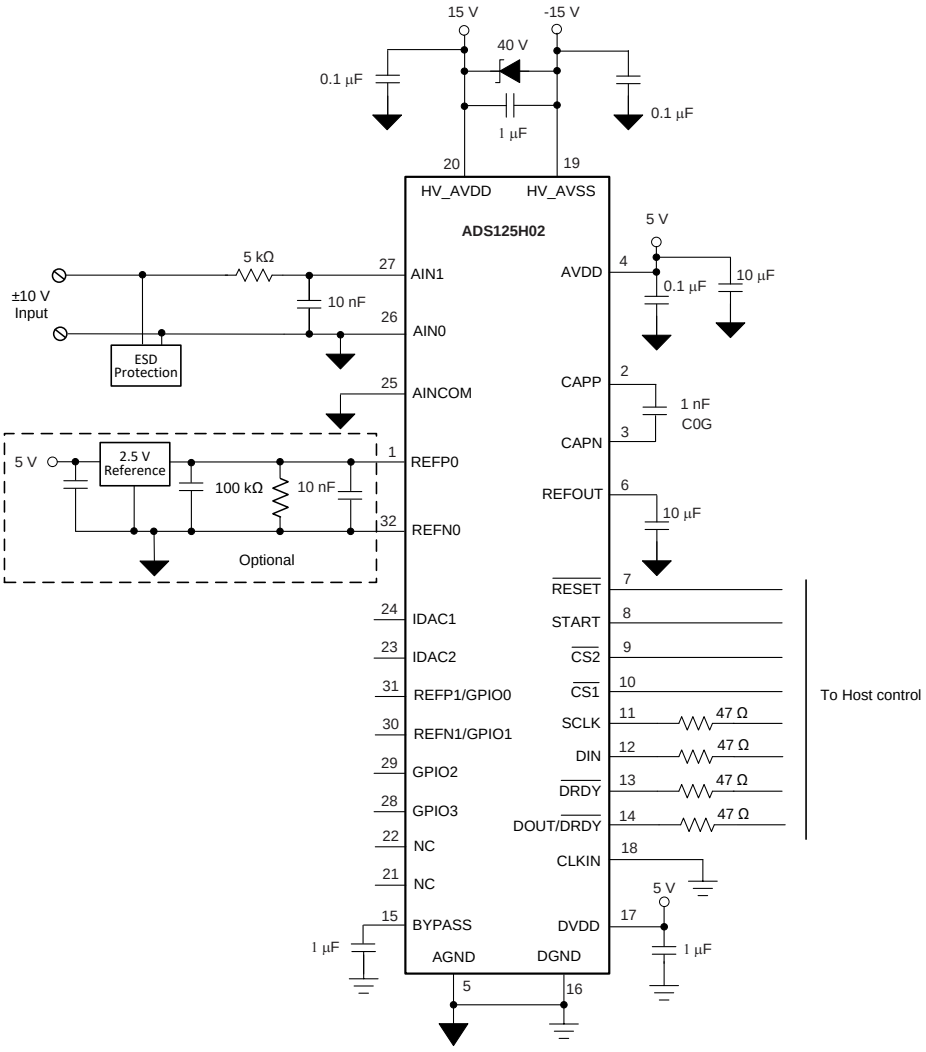

Figure 54. ±10 V Analog Input PLC Module

9.2.1 Design Requirements

Table 45 shows the design goals of the analog input PLC module. The ADC's programmability allows tradeoffs of sample rate, conversion noise and conversion latency. Table 46 shows the design parameters of the analog input PLC module.

Table 45. Design Goals

DESIGN GOAL	VALUE
Accuracy (0°C to 85°C)	±0.1 %
Basic Resolution	>0.01%
Sample Rate	>20000 SPS
Conversion latency	< 500 us

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Table 46. Design Parameters

DESIGN PARAMETER	VALUE
Input Signal Range	±10 V
Over Range	±12 V
Input Impedance	>100 MΩ
Over Voltage Tolerance	±35 V

9.2.2 Detailed Design Procedure

A key consideration in the design of an analog input module is to evaluate the ADC parameters that affect accuracy for operation over the specified temperature range. Table 47 shows the key ADC parameters that effect accuracy. The values shown in Table 47 are after calibration at T_A = 25°C. As summarized by the total accuracy calculation, the target accuracy value of ±0.1% is met by the ADC. Be aware the maximum values of ADC parameters are estimates values. Contact Texas Instruments to obtain the final maximum values.

Table 47. ADC Accuracy

PARAMETER	ACCURACY over 0°C to 105°C
Offset Drift	0.001%
Gain Drift	0.03%
Reference drift	0.06%
Total Accuracy	0.091%

Table 1 shows the conversion noise performance data for gain = 0.1875 expressed as an input-referred noise quantity. The table shows various tradeoffs among gain, sample rate and order of the digital filter order. Noise performance is optimize for a given design by considering the various parameters. In this example, the configuration of the ADC that yields the lowest noise while meeting the sample rate and settling time requirement is 25600 SPS, gain = 0.1875 V/V (default Sinc5 filter mode). This data rate yields conversion latency value of 250 uS.

The input-referred noise under this ADC configuration is <100 uV RMS. The ADC noise yields basic resolution of 100 uV / ±10 V = 0.001%

The ADC gain is programmed to gain = 0.1875 V/V, when used with a 2.5-V reference yields a nominal ADC input range of ±2.5 V / 0.1875 = ±13.3 V, except in this example using ±15-V power supplies, the input signal headroom is limited to ±12.5 V (excluding tolerance of the ±15-V power supplies). The input range satisfies the overrange design target requirement of ±12 V. Since the ADC input is a CMOS-input buffer, the input impedance is typically 1 GΩ.

ADVANCE INFORMATION

9.3 Initialization Setup

Figure 55 is a general configuration and measurement procedure.

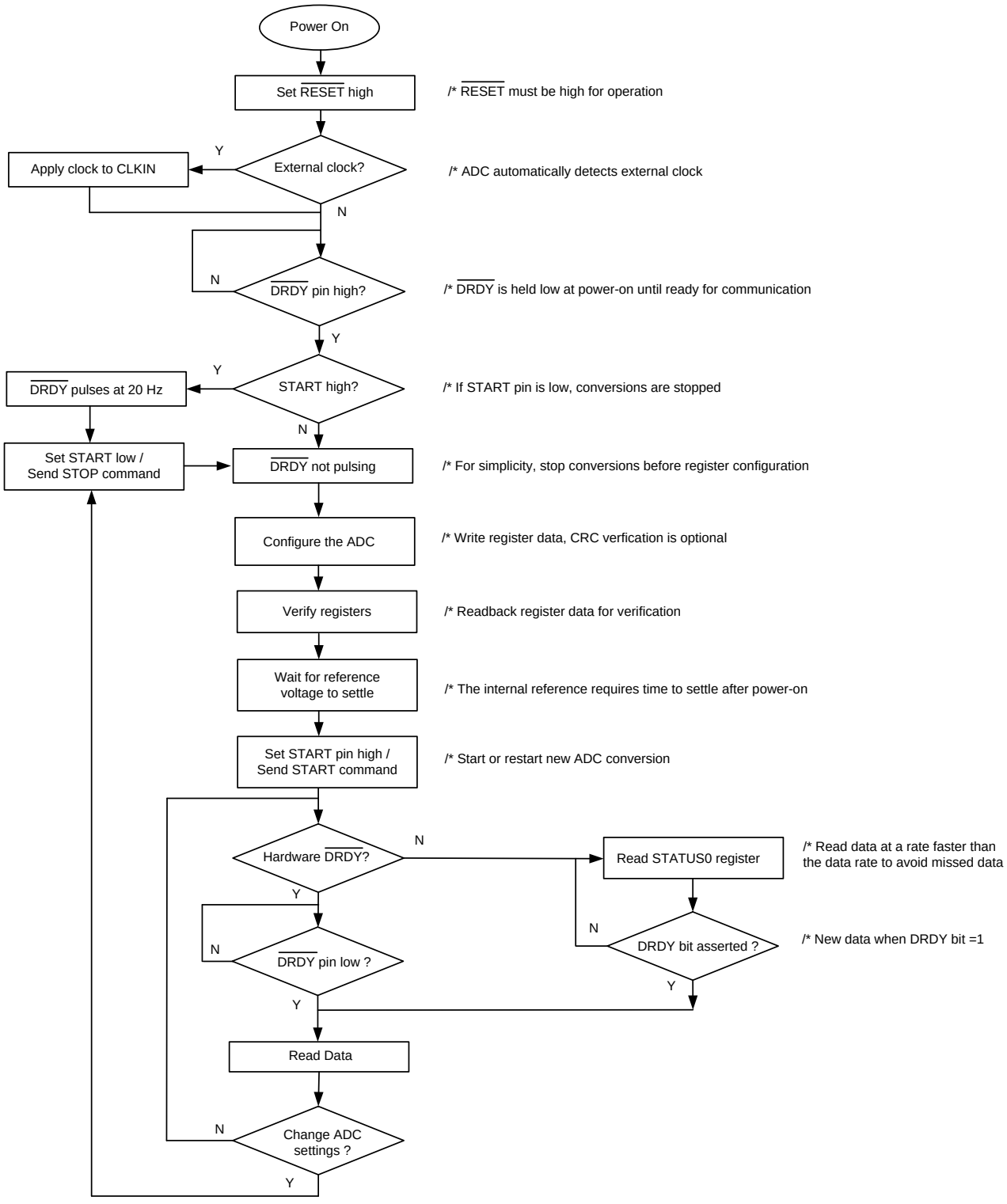


Figure 55. ADC Configuration and Measurement Procedure

ADVANCE INFORMATION

10 Power Supply Recommendations

The ADC requires three analog power supplies (high-voltage HV_AVDD and HV_AVSS, and low-voltage AVDD) and one digital power supply (DVDD). The high voltage analog power supply configuration is either bipolar (±5 V to ±18 V) or unipolar (10 V up to 36 V, with HV_AVSS tied to AGND). The AVDD power supply is 5 V. The digital supply range is 2.7 V to 5.25 V. AVDD and DVDD can be tied together as long as the 5-V power supply is free from excessive noise and glitches that can affect conversion results. An internal LDO regulator powers the digital core by the DVDD power supply. DVDD is the digital I/O voltage. Keep in mind that the GPIO I/O are at AVDD and AGND voltage potentials.

Voltage ripple produced by switch-mode power supplies may interfere with the ADC conversion accuracy. Use low-dropout regulators (LDOs) at the switching regulator output to reduce power-supply ripple.

Due to charging the 10-uF external capacitor at the reference output pin (REFOUT), be aware of the AVDD in-rush current when the internal reference is enabled. Be sure the AVDD voltage transient droop does not exceed 4.5 V under this condition.

10.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve optimum performance. Power supplies must be decoupled close to the power supply. For the high voltage analog supply (HV_AVDD and HV_AVSS), place a 1-µF capacitor between the pins and place 0.1-µF capacitors from each supply to the ground plane. Connect 0.1-µF and 10-µF capacitors in parallel at AVDD to the ground plane. Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. Use a multilayer ceramic chip capacitors (MLCCs) that offers low equivalent series resistance (ESR) and equivalent series inductance (ESL) characteristics for power-supply decoupling purposes.

10.2 Analog Power-Supply Clamp

It is important to evaluate circumstances when an input signal is present with the ADC, both powered and unpowered. When the input signal exceeds the power-supply voltage, it is possible to *backdrive* the analog power-supply voltage with the input signal through a conduction path of the internal ESD diodes. Backdriving the ADC power supply can also occur when the power-supply is on. The backdrive fault-current path is illustrated in Figure 53. Depending on how the power supply responds during a backdrive condition, it is possible to exceed the maximum rated ADC supply voltage. The ADC voltage must not be exceeded at all times. One solution is to clamp the analog supply to safe voltage using an external Zener diode.

10.3 Power-Supply Sequencing

The power supplies can be sequenced in any order, but do not allow and analog or digital voltage inputs to exceed the respective analog or digital power-supplies without providing a limit to possible input fault currents.

11 Layout

Good layout practices are crucial to realize the full-performance of the ADC. Poor grounding can quickly degrade the noise performance. The following layout recommendations help provide the best results.

11.1 Layout Guidelines

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from the CAPP and CAPN pins, away from the REFOUT pin, and away from all analog inputs and associated components in order to minimize interference.

Avoid long traces on DOUT/$\overline{\text{DRDY}}$, because high capacitance on this pin can lead to increased ADC noise levels. Use a series resistor or a buffer if long traces are used.

The internal reference output return shares the same pin as the AGND pin. To minimize coupling between the power supply and reference-return trace, route the traces separately; ideally, as a star connection to the AGND pin.

Use C0G capacitors on the analog inputs and for the CAPP to CAPN capacitor. Use ceramic capacitors (for example, X7R grade) for the power supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. The REFOUT pin requires a 10-μF capacitor and can be either ceramic or tantalum type. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

ADVANCE INFORMATION

11.2 Layout Example

Figure 56 shows an example layout of the ADS125H02, requiring a minimum of three PCB layers. The example circuit is shown with bi-polar supply operation (±15 V) and using the internal reference. In this example, the inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, dedicate the additional inner layer as the power plane. In this example, the ADC is oriented in such a way to minimize crossover of the analog and digital signal traces.

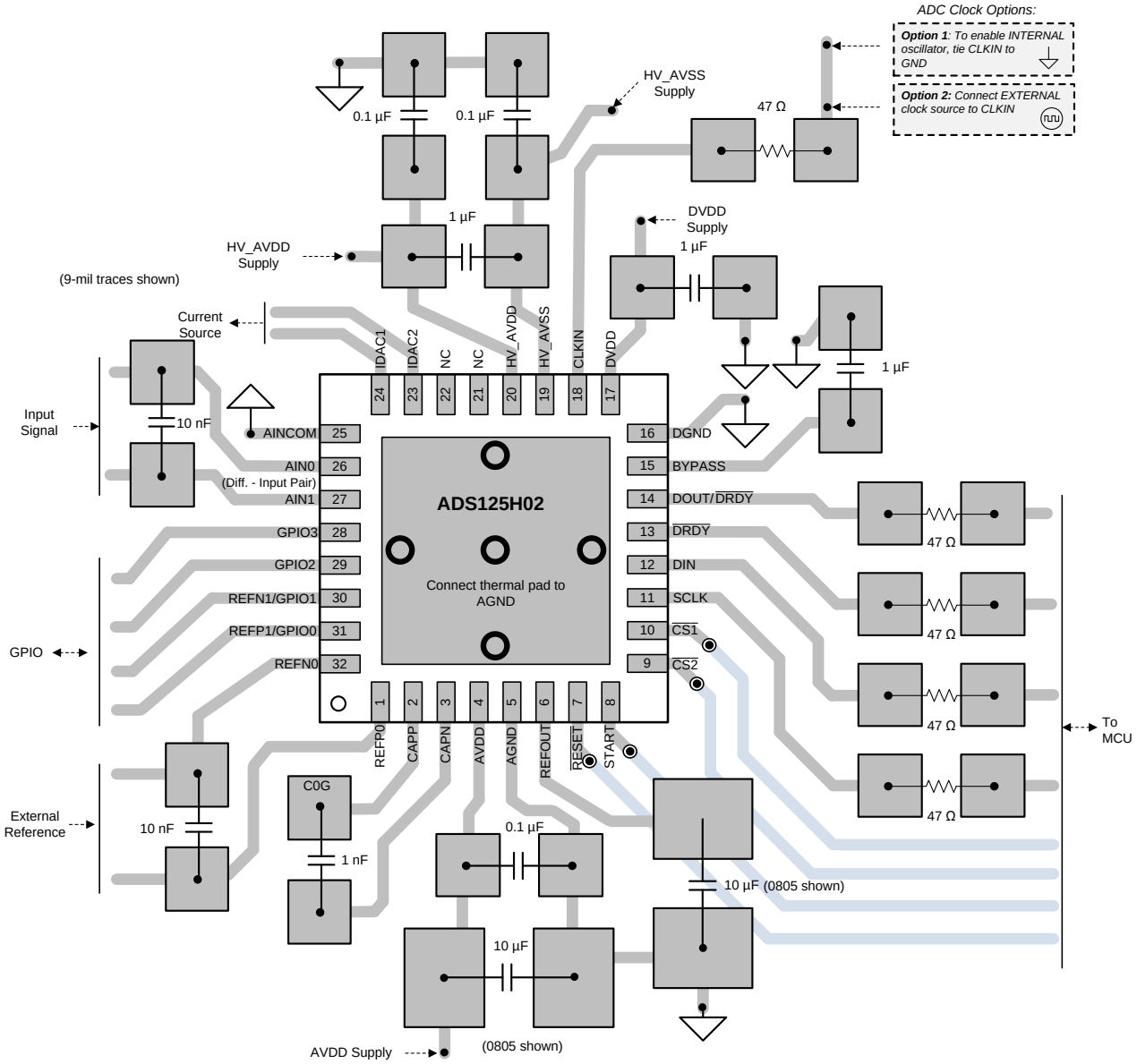


Figure 56. PCB Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 48. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS125H01	Click here	Click here	Click here	Click here	Click here
ADS125H02	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

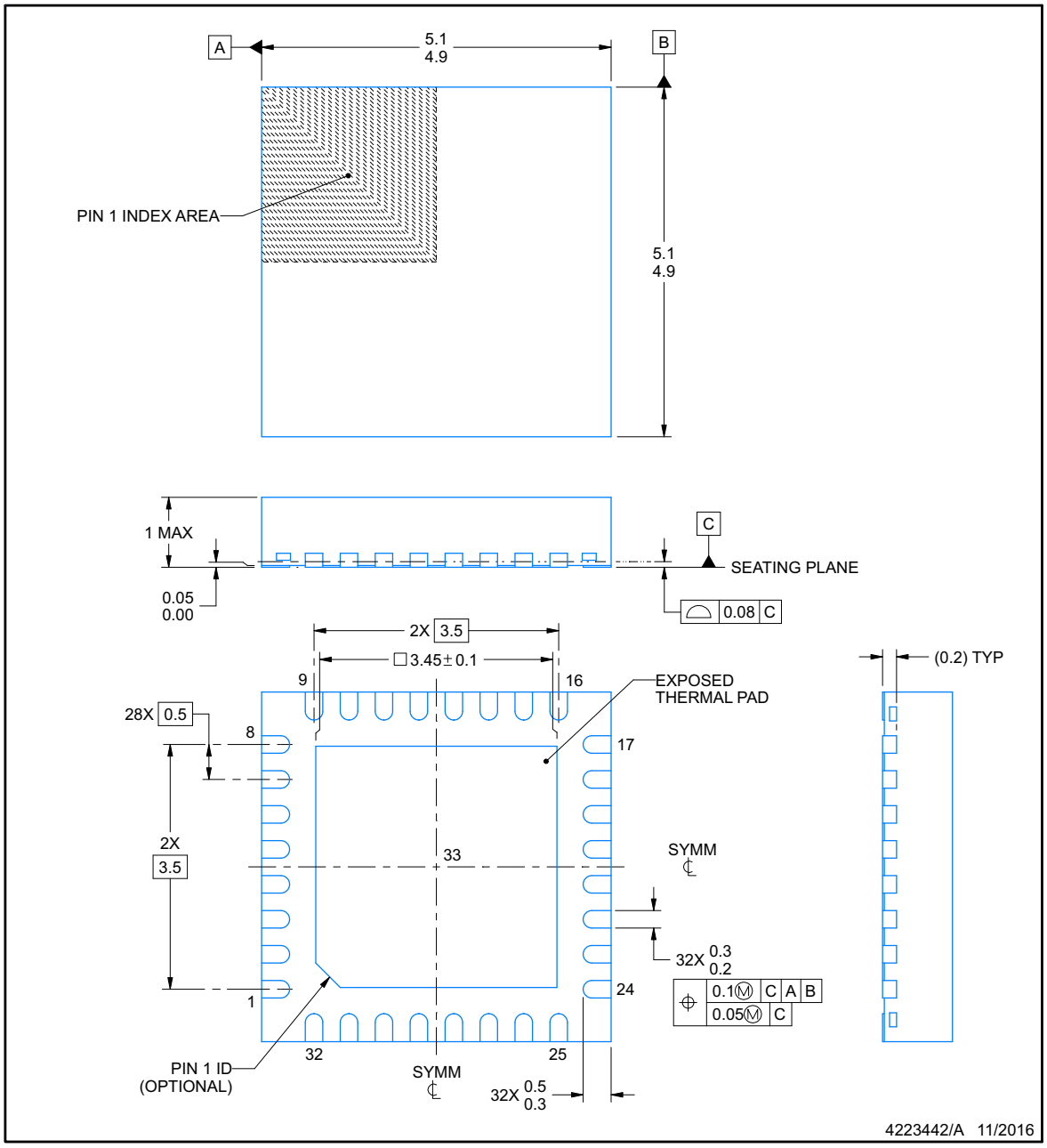
ADVANCE INFORMATION

PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

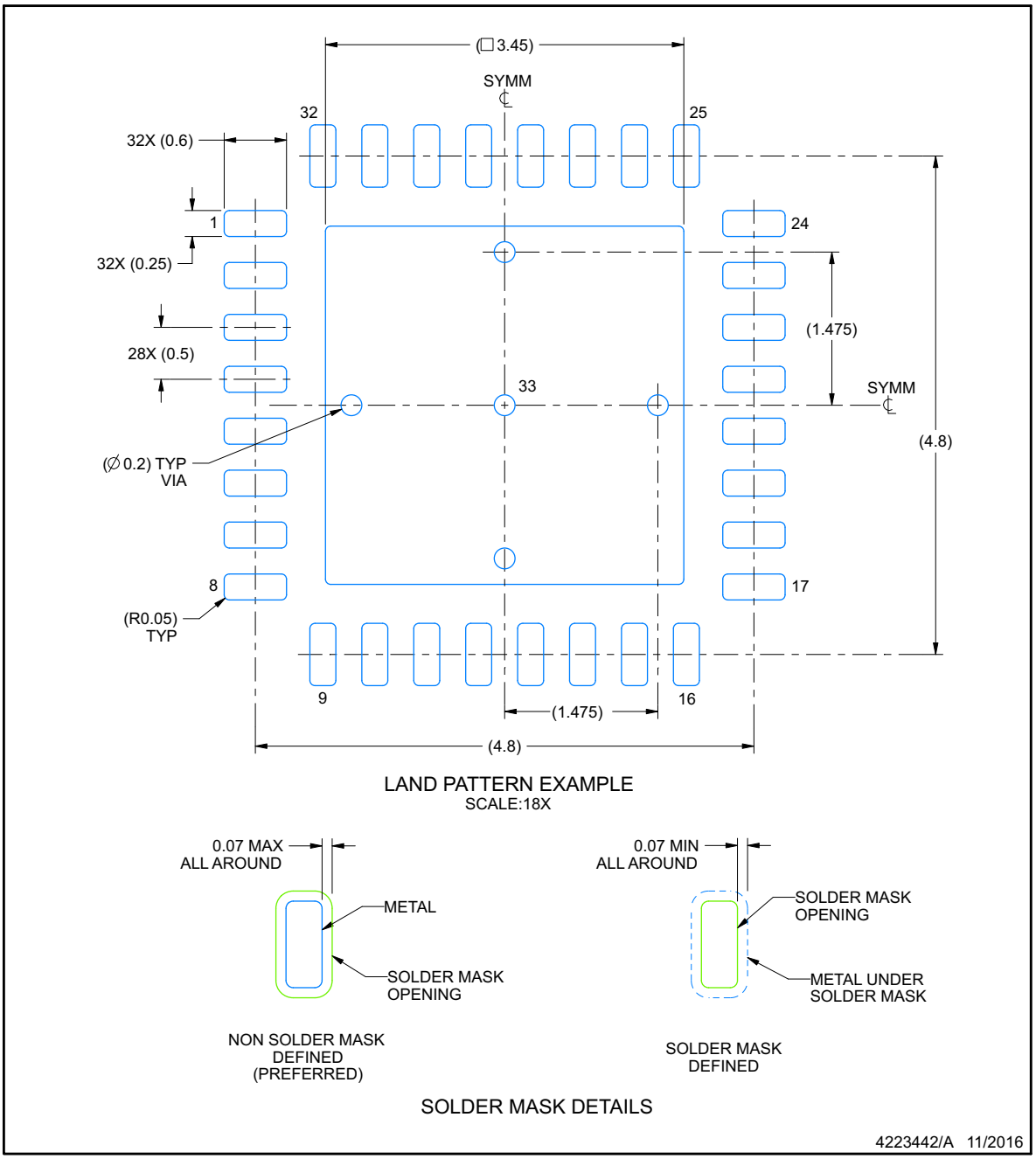
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

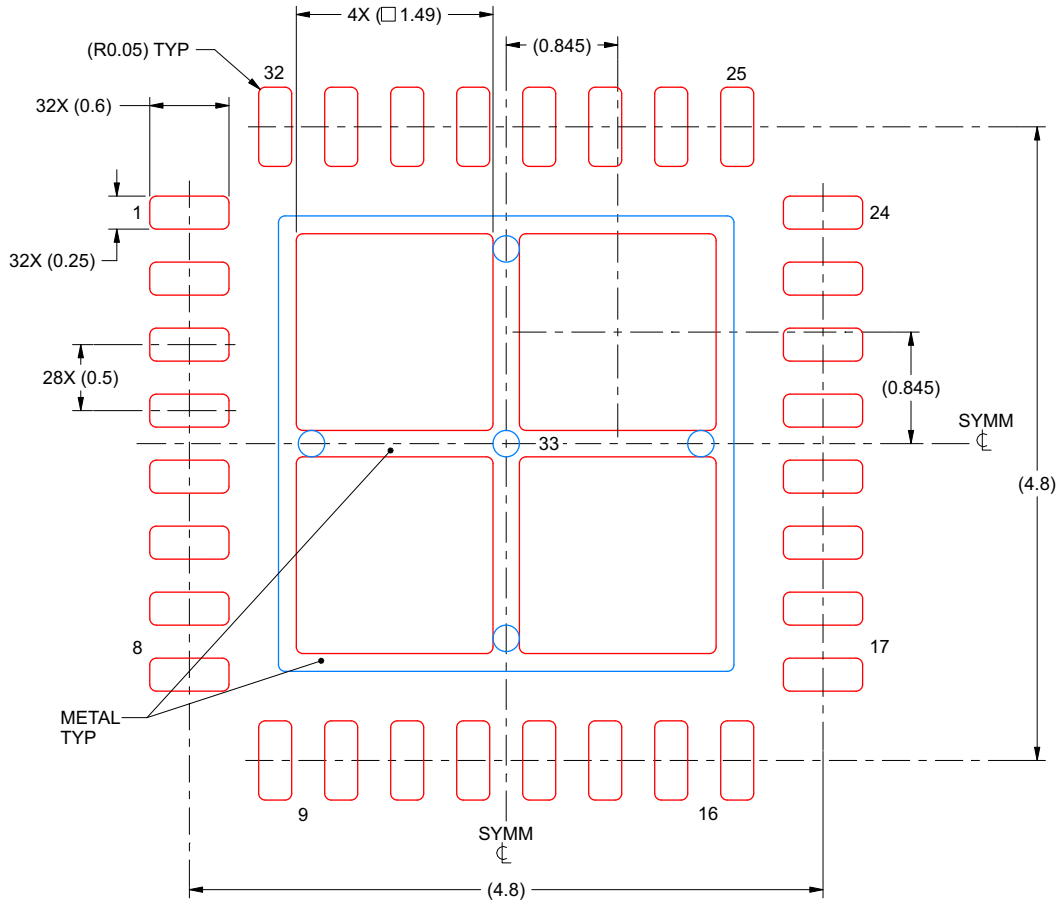
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS125H02IRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		
ADS125H02IRHBT	PREVIEW	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 125		
PADS125H02IRHBR	ACTIVE	VQFN	RHB	32	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

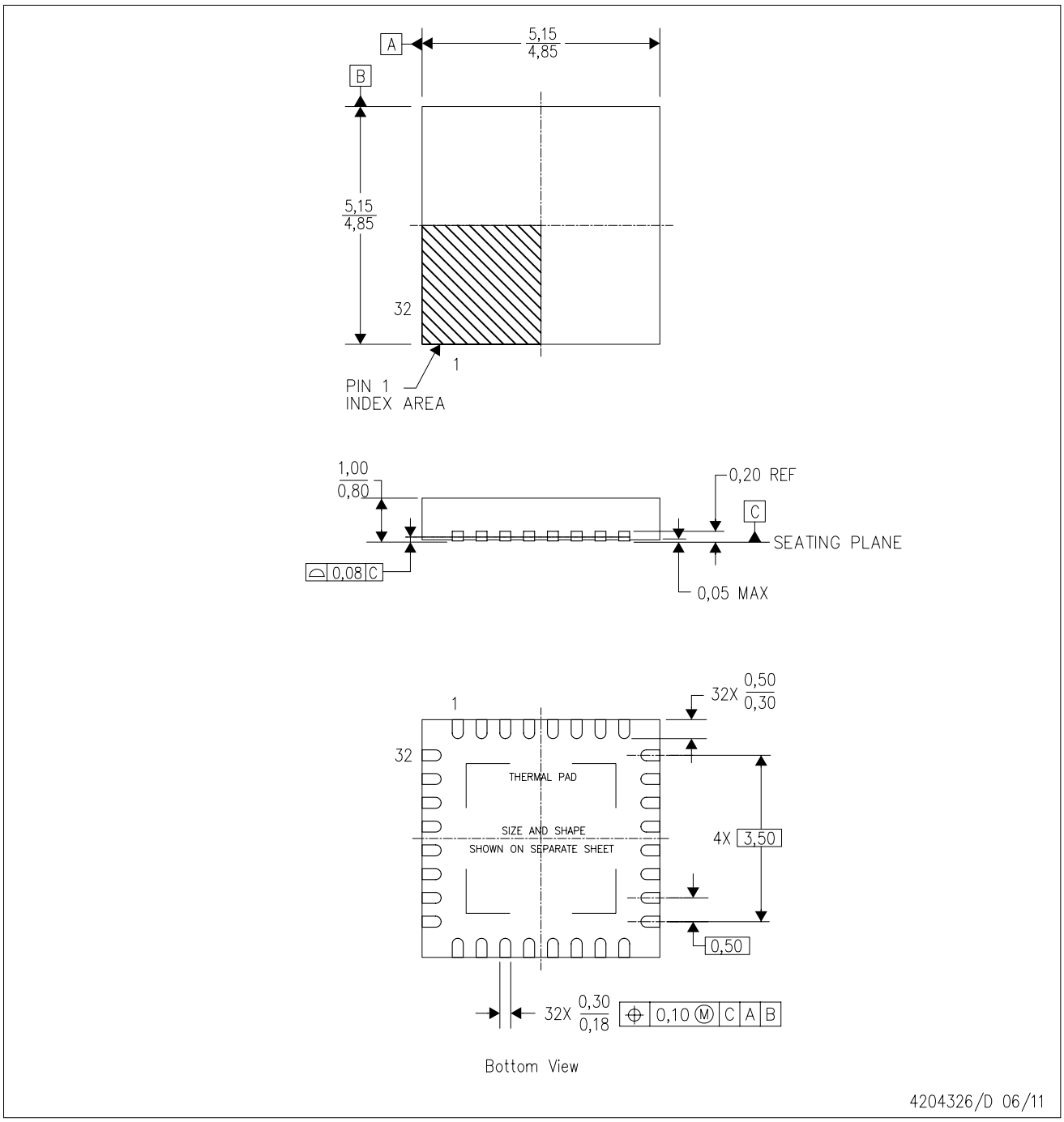
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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