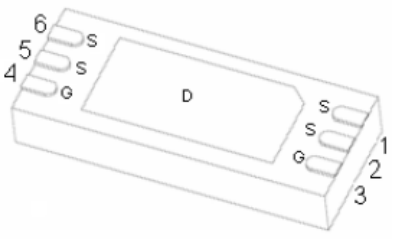
DFNWB5×2-6L-A Plastic-Encapsulate MOSFETS

DFNWB5×2-6L-A

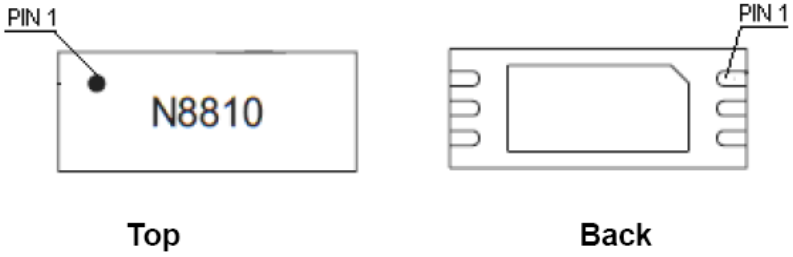


CJND2007 Dual N-Channel MOSFET

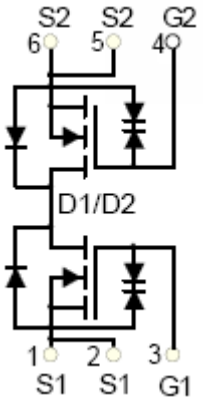
DESCRIPTION

The CJND2007 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch,facilitated by its common-drain configuration.

MARKING:



Top Back



MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	7	A
Pulsed Drain Current	I_{DM} *	30	A
Thermal Resistance from Junction to Ambient(note1)	$R_{\theta JA}$	175	℃/W
Thermal Resistance from Junction to Ambient(note2)		70	℃/W
Junction Temperature	T_j	150	℃
Storage Temperature	T_{stg}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

*Repetitive rating：Pluse width limited by junction temperature.

Note：1.When mounted on a minimum pad.

2.When mounted on 1 in^2 of 2oz copper board.

ELECTRICAL CHARACTERISTICS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =16V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±4.5V, V_{DS} = 0V			±1	μA
		V_{GS} =±8V, V_{DS} = 0V			±10	μA
Gate threshold voltage (note 1)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.4		1	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	V_{GS} =10V, I_D =7A			20	mΩ
		V_{GS} =4.5V, I_D =6.6A			22	mΩ
		V_{GS} =3.8V, I_D =6A			24	mΩ
		V_{GS} =2.5V, I_D =5.5A			26	mΩ
		V_{GS} =1.8V, I_D =5A			35	mΩ
Forward tranconductance (note 1)	g_{FS}	V_{DS} =5V, I_D =7A	9			S
Diode forward voltage(note 1)	V_{SD}	I_S=1A, V_{GS} = 0V			1	V
DYNAMIC PARAMETERS (note 2)						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		1150		pF
Output Capacitance	C_{oss}			185		pF
Reverse Transfer Capacitance	C_{rss}			145		pF
Total gate charge	Q_g	V_{DS} =10V,V_{GS} =4.5V,I_D =7A		15		nC
Gate-source charge	Q_{gs}			0.8		nC
Gate-drain charge	Q_{gd}			3.2		nC
SWITCHING PARAMETERS(note 2)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=5V,V_{DD}=10V, R_L=1.35Ω,R_{GEN}=3Ω		6		ns
Turn-on rise time	t_r			13		ns
Turn-off delay time	$t_{d(off)}$			52		ns
Turn-off fall time	t_f			16		ns

Notes :

1. Pulse Test : Pulse width≤300μs, duty cycle≤0.5%.
2. Guaranteed by design, not subject to production testing.