

THC63LVD827-Q

LOW POWER / SMALL PACKAGE / 24Bit COLOR LVDS TRANSMITTER

General Description

The THC63LVD827-Q transmitter is designed to support pixel data transmission between Host and Flat Panel Display and Dual Link transmission between Host and Flat Panel Display up to 1080p/1920x1200 resolutions.

The THC63LVD827-Q converts 27bits (RGB 8 bits + Hsync, Vsync, DE) of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

For dual LVDS out, LVDS clock frequency of 87MHz, 51bits of RGB data are transmitted at an effective rate of 609Mbps per LVDS channel.

For single LVDS out, LVDS clock frequency of 174MHz, 27bits of RGB data are transmitted at an effective rate of 1218Mbps per LVDS channel.

21bits (RGB 6 bits + Hsync, Vsync, DE) mode is also selectable for 6bit color transmission with lower power.

Features

- Low power 1.8V CMOS design
- 7mm x 7mm/72pin/0.65mm pitch/TFBGA package applicable to non-HDI PCB.
- Wide dot clock range, 10-174MHz, suited for TV Signal: up to 1080p(74.25MHz dual) PC Signal: up to 1920x1200(77MHz dual)
- Supports 1.8V single power supply
- 1.8V/2.5V/3.3V TTL/CMOS inputs are supported by setting IOVCC=1.8V/2.5V/3.3V
- LVDS swing reducible by RS-pin to reduce both EMI and power consumption
- PLL requires No external components
- Flexible Input / Output mode
- 1. Single in / Dual LVDS out
- 2. Single in / Single LVDS out
- 3. Double edge Single in / Dual LVDS out $% \mathcal{D}_{\mathcal{D}}$
- 2 LVDS data mapping to simplify PCB layout
- Power down mode
- Input clock triggering edge selectable by R/F pin
- 6bit / 8bit modes selectable by 6B/8B pin
- AEC-Q100 Grade 2 (-40 to 105degC)

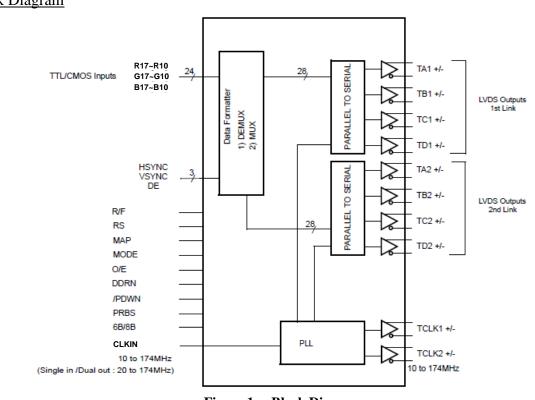


Figure 1. Block Diagram

Block Diagram



Pin Diagram (top view)

_										_
[1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1 +	TD1+	TA2+	TB2+	TC2+	TCLK2 +	A
в	TA1-	TB1-	TC1-	TCLK1	TD1-	TA2-	TB2-	TC2-	TCLK2 -	в
с	PRBS	N/C	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	с
D	R11	R10	LVDS VCC				GND	PDWN	OÆ	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B/8B	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	IOACC	R/F	DE	G
н	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	н
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
\neg	1	2	3	4	5	6	7	8	9	\square

TOP VIEW

Figure 2. Pin Diagram



Pin Description

TA1+,TA1A1,B1TB1+,TB1-A2,B2TC1+,TC1-A3,B3TD1+,TD1-A5,B5TCLK1+, TA2-A6,B6TB2+,TB2-A7,B7TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TD2-, TC2-A8,B8TC2+,TC2-A8,B8TC2+,TC2-A8,B8TD2-,TC2-B1,C2,F1,F2E1,C2,D1,D2IVDS Clock Out for 1st Link.Ri7-R10E1,E2,D1,D2E1,C2,D1,D2INDEG9DEG9DEG9NData Enable Input.VSYNCH9INVsync Input.HSVNCJ9INHsync Input.R/FG8INInput Clock Triggering Edge Select.RSF8INMAPE8MODEF7O/ED9INMODEO/ED9INOutput enable.L: Output data mode. See Fig.10 and Fig.13.MODED9INMODEE7INMODED9O/ED9 </th <th></th> <th>1</th> <th></th> <th>Pin Description</th>		1		Pin Description					
TB1+,TB1-A2,B2 TC1+,TC1-A3,B3TD1+,TD1-A5,B5TCLK1+,TCLK1-A4,B4TA2+,TA2-A6,B6TB2+,TB2-A7,B7TC2+,TC2-A8,B8TD2+,TD2-C9,C8TCLK2+, TCLK2-A9,B9VEXP, TD2-C9,C8TCLK2+,TCLK2-A9,B9INB17-B10J6,HG,J,H3B17-B10J6,HG,J,H3J6,HG,J,H3DEG9VSYNCH9INVsync Input.VSYNCH9INVsync Input.CLKINF9INClock Triggering Edge Select.R/FG8RNINHsync Input.CLKINF9INUVDS swing mode select.R/FG8INInput Clock Triggering Edge Select.HHMAPE8INIVDS swing mode select.MODEE7INIVDS mapping table select. See Fig.12 and Fig.13.MODED9INPixel data mode. See Fig.10 and Fig.11.MODED9INIVDI disable (all outputs are Hi-Z).OVED9INCouput disable (all outputs are Hi-Z).Power Down enable H: Normal operation.	Pin Name	Pin #	Туре	Description					
IBI+, IBI+, TCI+, TCI-A2,B2 A3,B3TD1+, TD1-A5,B5TCLK1+, TCLK1-A4,B4TA2+,TB2-A7,B7TC2+,TC2-A8,B8TD2+,TD2-C9,C8TCLK2+, TCLK2-A9,B9TCLK2+, TCLK2-A9,B9TCLK2+, TCLK2-A9,B9R17-R10E1,E2,D1,D2G17-G10J4,H4,J3,H3J2,H2,J1,H1J3,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7B17-B10J8,H8,J7,H7J10,HC,D2J9INClock Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.HSYNCJ9INHsync Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeR/FE8INE8ININMODEE7ININMODEE7ININMODED9INClock and Geration.MODED9INClouput disable (all outputs are Hi-Z).Power Down enable H: Normal operation.<	TA1+,TA1-			The 1st Link					
$ \begin{array}{c c c c c c c } \hline A3,B3 \\ \hline TD1+, TD1- & A3,B3 \\ \hline TD1+, TD1- & A3,B3 \\ \hline TD2+, TD2- & A3,B8 \\ \hline TD2+, TD2- & A3,B8 \\ \hline TD2+, TD2- & C9,C8 \\ \hline TCLK2+, TCLK2- & A9,B9 \\ \hline TCLK1+ & F1, F1, F1 \\ \hline TCLK1+ & F19 \\ \hline TC$,	A2,B2							
TOLH, IDI-, A3,83TCLK1+, TDL-, A4,B4LVDS OUTTA2+,TA2-A6.B6TB2+,TB2-A7,B7TC2+,TC2-A8,B8TD2+,TD2-C9,C8TCLK2+, TCLK2-A9,B9R17-R10G1,G2,F1,F2G17-G10J2,H2,J1,H1J2,H2,J1,H1INB17-B10J8,H8,J7,H7J6,H5,S1,H5Pixel Data Input.DEG9DEG9DEG9INData Enable Input.VSYNCH9INUND Storek Triggering Edge Select.R/FG8RSF8F8INMAPE8MODEF7O/ED9O/ED9NPixel data mode. See Fig.10 and Fig.8)MODEE7NDiata mode. See Fig.10 and Fig.11.MODED9NOutput data mode. See Fig.10 and Fig.12.O/ED9NOutput data mode. See Fig.10 and Fig.12.O/ED9NOutput data mode. See Fig.10 and Fig.11.MODEE7NOutput data mode. See Fig.10 and Fig.11.MODED9NOutput data mode. See Fig.10 and Fig.12.Power Down enable.HSingle out (Single-in / Single-out)IND9NOutput disable (all outputs are Hi-Z).Power Down enable.HNormal operation.	TC1+,TC1-	A3,B3							
TA2+,TA2A6,B6 TB2+,TB2-LVDS 001TB2+,TB2-A7,B7 TC2+,TC2-A8,B8 TD2+, TD2- C9,C8The 2nd Link. The 2nd pixel output data when Dual out.TD2+,TD2- C9,C8C9,C8LVDS Clock Out for 2nd Link. The 2nd pixel output data when Dual out.R17-R10G1,G2,F1,F2 E1,E2,D1,D2LVDS Clock Out for 2nd Link.G17-G10J4,H4,J3,H3 J2,H2,J1,H1INB17-B10J8,H81,7,H7Pixel Data Inputs.B17-B10J8,H81,7,H7INB17-B10J8,H81,7,H7VSYNCH9INVSYNCH9INVSYNCH9INK/FG8INR/FG8INR/FG8INMAPE8INMODEE7INMODEE7INMODEE7INMODED9INMODED9INPixel data mode. See Fig.10 and Fig.11.MODED9INPower Down enable H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enable H: Normal operation.	TD1+, TD1-	A5,B5		Output data when Single out.					
TA2+,TA2- A6.B6 TB2+,TB2- A7.B7 TC2+,TC2- A8.B8 TD2+,TD2- C9.C8 TLK2+,TCLK2- A9.B9 R17-R10 G1,G2,F1,F2 E1,E2,D1,D2 F1,E2,D1,D2 G17-G10 J4,H4,J3,H3 J2,H2,J1,H1 IN B17-B10 J8,H8,7,H7 J6,H6,J5,H5 DE OE G9 IN VSYNC H9 IN VSyNC J9 IN HSync J9 IN CLKIN F9 IN Clock Input. Input Clock Triggering Edge Select. R/F G8 IN MAP E8 IN MAP Mapping Mode H 350mV L 200mV MODE E7 IN MODE M	TCLK1+, TCLK1-	A4,B4		LVDS Clock Out for 1st Link.					
TC2+,TC2-A8,B8 TD2+,TD2-The 2nd pixel output data when Dual out.TD2+,TD2- TCLK2+,TCLK2- $A9,B9$ LVDS Clock Out for 2nd Link.R17-R10 $G1,G2,F1,F2$ E1,E2,D1,D2LVDS Clock Out for 2nd Link.G17-G10 $J4,H4,J3,H3$ J2,H2,J1,H1INPixel Data Inputs.B17-B10 $J8,H8,J7,H7$ J6,H6,J5,H5INData Enable Input.DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeR/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMAPE8INPixel data mode. See Fig.12 and Fig.13.MAPE8ININMODEE7INPixel data mode. See Fig.10 and Fig.13.O/ED9INOutput enable H: Single out (Single-in / Dual-out)O/ED9INOutput enable. H: Output enable. L: Output disable (all outputs are Hi-Z). Power Down enable H: Sormal operation.	TA2+,TA2-	A6,B6							
TD2+, TD2- C9,C8 TCLK2+, TCLK2- A9,B9IVDS Clock Out for 2nd Link.R17-R10G1,G2,F1,F2 G1,G2,F1,F2 [E,E2,D1,D2]IVDS Clock Out for 2nd Link.R17-R10G1,G2,F1,F2 G1,G2,F1,F3IVDS Clock Out for 2nd Link.G17-G10J4,H4,J3,H3 J2,H2,J1,H1IN J8,H8,J7,H7 J6,H6,J5,H5Pixel Data Inputs.DEG9IN J8,H8,J7,H7 J6,H6,J5,H5Data Enable Input.VSYNCH9IN H9Vsync Input.Mapping Input.CLKINF9IN G8Clock Input.Mapping Edge Select. H: Rising edgeR/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8IN $\frac{\mathbb{R}S}{1.VDS swing Woop. see Fig.7 and Fig.8)}{\frac{1}{1.0000000000000000000000000000000000$	TB2+,TB2-	A7,B7		The 2nd Link.					
TCLK2-A9,B9IVDS Clock Out for 2nd Link.R17-R10G1,G2,F1,F2 E1,E2,D1,D2 J2,H2,J1,H1IVDS Clock Out for 2nd Link.G17-G10J4,H4,J3,H3 J2,H2,J1,H1INPixel Data Inputs.B17-B10J8,H8,J7,H7 J6,H6,J5,H5INData Enable Input.DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INLVDS swing(Vop. see Fig.7 and Fig.8) 3 50mV LMAPE8INEsLVDS swing(Vop. see Fig.12 and Fig.8) 3 200mVMODEE7INPixel data mode. See Fig.10 and Fig.13.MODEE7INOutput enable H: Single out (Single-in / Single-out) LO/ED9INOutput enable. H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enableFormal operation.Power Down enable H: Normal operation.	TC2+,TC2-	A8,B8		The 2nd pixel output data when Dual out.					
TCLK2- A9.B9R17-R10G1,G2,F1,F2 E1,E2,D1,D2G17-G10J4,H4,3,H3 J2,H2,J1,H1INB17-B10J8,H8,J7,H7 J6,H6,J5,H5Pixel Data Inputs.DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INClock Ange.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMAPE8INExperimental String Control DODEMODEE7INVDS mapping table select. See Fig.12 and Fig.8) H Mapping MODE1 LMODEE7INOutput enable HO/ED9INOutput enable H: Output enable. L: Output disable (all outputs are Hi-Z).OWND9INOutput enable H: Normal operation.OWND9INCuput disable (all outputs are Hi-Z).OWND9INH: Normal operation.	TD2+, TD2-	C9,C8							
R17-R10E1,E2,D1,D2 J4,H4,J3,H3 J2,H2,J1,H1INPixel Data Inputs.B17-B10J8,H8,J7,H7 J6,H6,J5,H5INData Enable Input.DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Swing(Vop.see Fig.7 and Fig.8) H 1 350mV LMAPE8INIVDS swing mode select.MODEE7INIVDS mapping table select. See Fig.12 and Fig.13.MODEE7INInput Mode H H Dual out (Single-in / Single-out) LO/ED9INOutput enable H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enableH: Normal operation.		A9,B9		LVDS Clock Out for 2nd Link.					
R17-R10E1,E2,D1,D2G17-G10J4,H4,J3,H3J2,H2,J1,H1J2,H2,J1,H1B17-B10J8,H8,J7,H7J6,H6,J5,H5NDEG9INVSYNCH9INHSYNCJ9INHSYNCH9INCLKINF9INCLKINF9INCLKINF8INInput Clock Input.Input Clock Input.RFG8ININLVDS swing mode select.RSF8INE8INInput Stime Clock See Fig.7 and Fig.8) H 200mVMAPE8INMODEE7INO/ED9INO/ED9INHOutput enable H: Output disable (all outputs are Hi-Z).Power Down enable H: Normal operation.Power Down enableH: Normal operation.H: Normal operation.	D17 D10	G1,G2,F1,F2		LVDS Clock Out for 2nd Link.					
G17-G10J2,H2,J1,H1 J8,H8,J7,H7 J6,H6,J5,H5INPixel Data Inputs.B17-B10J8,H8,J7,H7 J6,H6,J5,H5J8,H8,J7,H7 J6,H6,J5,H5Data Enable Input.DEG9INData Enable Input.WSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMAPE8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMAPE8INPixel Data InputsMODEF8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMODEF8INPixel Data InputsMODEF8INInput Clock Triggering Edge Select. Single out Single out LMODEF8INInput Clock Triggering Edge Select. Select. LMODEF8INPixel data mode. See Fig.10 and Fig.13.MODEE7INPixel data mode. See Fig.10 and Fig.11.MODED9INOutput enable. H: Output enable. L: Output disable (all outputs are Hi-Z).MOWND9INH: Normal operation.	K17~K10								
G17-G10J2,H2,J1,H1INPixel Data Inputs.B17-B10J8,H8,J7,H7J8,H8,J7,H7J6,H6,J5,H5ODEG9INDEG9INVSYNCH9INVSYNCJ9INHSYNCJ9INCLKINF9INCLKINF9INCLKINF9INCLKINF9INCLKINF8INImput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INImput Clock Swing(Vop-see Fig.7 and Fig.8) LImput Clock Triggering Edge Select. HRSF8INImput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeMAPE8INImput Clock Swing(Vop-see Fig.7 and Fig.8) LImput Clock Triggering Edge Select. Swing mode select.RSF8INImput Clock Swing(Vop-see Fig.7 and Fig.8) LImput Clock Triggering Edge Select. Swing Mode LRSF8INImput Clock Select.Imput Clock Select See Fig.12 and Fig.13.MODEE7INImput Clock See Fig.10 and Fig.11.MODED9INH: Output enable H: Output enable. L: Output disable (all outputs are Hi-Z).Imput ClockD9INH: Normal Operation.		J4,H4,J3,H3	DI						
B17-B10J8,H8,J7,H7 J6,H6,J5,H5DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeR/FG8INLVDS swing mode select. HRSF8INEsLVDS swing mode select. UVDS swing mode select.MAPE8INEvon select. HSton V 200mVMODEE7INPixel data mode. See Fig.10 and Fig.13.MODEE7INOutput enable H Single out (Single-in / Single-out) LO/ED9INOutput enable. H: Output enable. L: Output disable (all outputs are Hi-Z).OWND8INOutput figure on.	GI7~GI0	J2,H2,J1,H1	IIN	Pixel Data Inputs.					
B17-B10J6,H6,J5,H5DEG9INData Enable Input.VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeR/FG8INLVDS swing mode select. HRSF8INLVDS swing dege, L: Falling edgeMAPE8INEVDS mapping table select. See Fig.7 and Fig.8) HMODEE8INMAPMODEE7INPixel data mode. See Fig.10 and Fig.11.MODEE7INOutput enable H: Single out (Single-in / Single-out) LO/ED9INOutput enable. H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enable H: Normal operation.Pixel disale (all outputs are Hi-Z).	D17 D14								
VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8IN $\frac{RS}{IVDS swing mode select.}$ RSF8IN $\frac{RS}{IVDS swing(V_{OD}, see Fig.7 and Fig.8)}{IVDS swingV}$ L 200mVMAPE8IN $\frac{RS}{IVDS swing(V_{OD}, see Fig.7 and Fig.8)}{IVDS swing mode select.}$ MAPE8IN $\frac{MAP}{Mapping Mode}$ H L DomvMODEE7IN $\frac{MAP}{Mapping MODE1}$ L L Dual out (Single-in / Single-out) L Dual out (Single-in / Single-out) LO/ED9IN $\frac{MODE}{H}$ H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enableH: Normal operation.	B17~B10	J6,H6,J5,H5							
VSYNCH9INVsync Input.HSYNCJ9INHsync Input.CLKINF9INClock Input.R/FG8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8INInput Clock Swing(V _{OD} , see Fig.7 and Fig.8) H 200mVRSF8ININMAPE8INIVDS swing(V _{OD} , see Fig.7 and Fig.8) H 200mVMAPE8INIVDS mapping table select. See Fig.12 and Fig.13.MAPE8INMAPMapping Mode H Mapping MODE1 L LMODEE7INMODEModes H Single out (Single-in / Single-out) L Dual out (Single-in / Dual-out)0/ED9INH: Output enable H: Output enable. L: Output disable (all outputs are Hi-Z).Power Down enable H: Normal operation.Power Iown enable H: Normal operation.	DE	G9	IN	Data Enable Input.					
CLKIN F9 IN Clock Input. R/F G8 IN Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge RS F8 IN $IVDS$ swing mode select. H: Rising edge, L: Falling edge RS F8 IN $IVDS$ swing mode select. H: Rising edge, L: Falling edge MAP F8 IN $IVDS$ swing mode select. H: DOWN MAP E8 IN $IVDS$ mapping table select. See Fig.12 and Fig.13. L: DOWN MAP E8 IN MAP Mapping Mode H: Mapping MODE1 L: Mapping MODE2 MODE E7 IN $MODE$ Modes H: Single out (Single-in / Single-out) L: Dual out (Single-in / Dual-out) O/E D9 IN Output enable H: Output enable. L: Output enable. L: Output denable. H: Normal operation.	VSYNC	H9	IN						
CLKINF9INClock Input. R/F G8INInput Clock Triggering Edge Select. H: Rising edge, L: Falling edgeRSF8IN $\frac{RS}{LVDS swing mode select.}$ RSF8IN $\frac{RS}{H}$ LVDS Swing(V _{QD} , see Fig.7 and Fig.8) HMAPE8IN $\frac{RS}{H}$ LVDS mapping table select. See Fig.12 and Fig.13.MAPE8IN $\frac{MAP}{H}$ Mapping Mode HMODEE7IN $\frac{MODE}{H}$ Modes Single-out) LO/ED9INOutput enable H: Output enable L: Output disable (all outputs are Hi-Z).Power Down enable H: Normal operation.Power Down enable H: Normal operation.	HSYNC	J9	IN	Hsync Input.					
R/F G8 IN Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge RS F8 IN RS LVDS swing mode select. RS F8 IN RS LVDS Swing(V _{OD} , see Fig.7 and Fig.8) H 350mV MAP E8 IN RS LVDS mapping table select. See Fig.12 and Fig.13. MAP E8 IN MAP Mapping Mode H Mapping MODE1 Mapping MODE2 MODE E7 IN MODE Modes H Single out (Single-in / Single-out) Dual out (Single-in / Dual-out) O/E D9 IN Output enable Coutput disable (all outputs are Hi-Z). Power Down enable H: Normal operation. Power and Pieration.	CLKIN	F9	IN						
K/F G8 IN H: Rising edge, L: Falling edge RS F8 IN IVDS swing mode select. RS F8 IN IVDS swing(V _{OD} , see Fig.7 and Fig.8) H MAP E8 IN IVDS mapping table select. See Fig.12 and Fig.13. MAP E8 IN MAP Mapping Mode H MODE E7 IN MODE Modes MODE E7 IN Output enable H: Output enable H: Output enable. L: Output disable (all outputs are Hi-Z). OVE D9 IN Output disable (all outputs are Hi-Z). Power Down enable H: Normal operation. Power Down enable H: Normal operation.	D/E	C 9	DI						
RSF8IN $RS \\ H \\ 350mV \\ 1 \\ 200mV$ MAPE8INLVDS mapping table select. See Fig.12 and Fig.13.MAPE8IN $MAP \\ H \\ Mapping MODE1 \\ L \\ Mapping MODE2MODEE7INPixel data mode. See Fig.10 and Fig.11.MODEE7INMODE \\ H \\ Mapping out (Single-in / Single-out) \\ L \\ Dual out (Single-in / Dual-out)O/ED9INOutput enable \\ H \\ Single (all outputs are Hi-Z).MOWND9INPower Down enable \\ H \\ Normal operation.$	R/F	G8	IIN						
MAP E8 IN MAP Mapping Mode H Mapping MODE1 L Mapping MODE2 MODE E7 IN Pixel data mode. See Fig.10 and Fig.11. MODE E7 IN MODE MODE Modes H Single out (Single-in / Single-out) U Dual out (Single-in / Dual-out) Dual out (Single-in / Dual-out) O/E D9 IN Output enable L: Output disable (all outputs are Hi-Z). Power Down enable H: Normal operation. H: Normal operation.	RS	F8	IN	RS LVDS Swing(V _{OD} , see Fig.7 and Fig.8) H 350mV					
MODE E7 IN MODE Modes H Single out (Single-in / Single-out) L Dual out (Single-in / Dual-out) O/E D9 IN Output enable H: Output disable (all outputs are Hi-Z). Power Down enable H: Normal operation.	МАР	E8	IN	MAP Mapping Mode H Mapping MODE1					
O/E D9 IN H: Output enable. L: Output disable (all outputs are Hi-Z). OPWIN D8 Power Down enable H: Normal operation.	MODE	E7	IN	MODE Modes H Single out (Single-in / Single-out)					
H: Normal operation.	O/E	D9	IN	H: Output enable. L: Output disable (all outputs are Hi-Z).					
L: Power down (all outputs are Hi-Z and all circuits a stand-by mode with minimum current (I _{TCCS})).	/PDWN	D8	IN	H: Normal operation.L: Power down (all outputs are Hi-Z and all circuits are					
PRBS ^(*a) C1 IN Must be tied to GND.	PRBS ^(*a)	C1	IN	-					

Table 1. Pin Description



Pin Name	Pin #	Туре	Description
Reserved1	C3	IN	Must be tied to GND.
6B/8B	F7	IN	6bit / 8bit mode select.H: 6bit mode (21bit mode),L: 8bit mode (27bit mode).
DDRN	E9	IN	DDR function is active when MODE=L (Dual-out mode) H: DDR (Double Edge input) function disable (Fig.7). L: DDR (Double Edge input) function enable (Fig.8).
N/C	C2	-	Must be Open.
VCC	G3,G5		Power Supply Pins for digital circuitry.
IOVCC	G7	Power	Power Supply Pins for IO inputs circuitry.
LVDSVCC	C5,D3	Power	Power Supply Pins for LVDS Outputs.
PLLVCC	C7		Power Supply Pins for PLL circuitry.
GND	F3,G4,G6,C4, E3,C6,D7	Ground	Ground Pins.

Pin Description (Continued)

(*a) : Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2²³-1. The generated PRBS is fed into input data latches, encoded and serialized into LVDS OUT.

This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.



Absolute Maximum Ratings

Table 2.	Absolute	Maximum	Rating
	TRODUCATE		

Parameter	Min	Max	Unit
Power Supply Voltage (IOVCC)	-0.3	+4.0	V
Power Supply Voltage (VCC,PLLVCC,LVDSVCC)	-0.3	+2.1	V
CMOS/TTL Input Voltage	-0.3	IOVCC+0.3	V
LVDS Transmitter Output Voltage	-0.3	LVDSVCC+0.3	V
Output Current	-50	+50	mA
Junction Temperature	-	+125	°C
Storage Temperature Range	-55	+125	°C
Reflow Peak Temperature / Time	-	+260 / 10sec	°C
Maximum Power Dissipation @+25°C	-	1.3	W

Recommended Operating Conditions

Table 3. Operating Condition										
Symbol		Р	arameter		Min	Тур	Max	Unit		
Та	Operating A	mbient Temper		-40	25	+105	°C			
IOVCC	Power Supp	Power Supply Voltage					3.6	v		
PLLVCC LVDSVCC VCC	Power Supp	Power Supply Voltage					1.98	V		
	MODE = Clock Dual - o Frequency		Single Edge Input (DDRN=H)	Input	20	-	174 87			
		MODE = L	Double Edge	LVDS Output Input	10 10	-	87 174			
F _{clk}		Duai - Out	Input (DDRN=L)	LVDS Output	10	-	174	MHz		
				Input	10	-	174			
				LVDS Output	10	-	174			

Table 3. Operating Condition



Electrical Characteristics

CMOS/TTL (Pin type "IN") DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit				
V _{IH18}	High Level Data Input Voltage	IOVCC=1.62V~1.98V	0.65*IOVCC	-	IOVCC	V				
V _{IL18}	Low Level Data Input Voltage	10 VCC-1.02 V~1.98 V	GND	-	0.35*IOVCC	V				
V _{IH25}	High Level Data Input Voltage	IOVCC=2.3V~2.7V	1.7	-	IOVCC	V				
V _{IL25}	Low Level Data Input Voltage	10vcc=2.3v~2.7v	GND	-	0.7	V				
V _{IH33}	High Level Data Input Voltage	IOVCC=3.0V~3.6V	2.0	-	IOVCC	V				
V _{IL33}	Low Level Data Input Voltage	10 v CC=3.0 v~3.0 v	GND	-	0.8	V				
I _{INC}	Input Current	VIN=GND~IOVCC	-10	-	+10	μΑ				

Table 4. CMOS/TTL DC Specifications

LVDS Transmitter (Pin type "LVDS OUT") DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Co	onditions	Min	Тур	Max	Unit
		D 1000	Normal swing RS=H	250	350	450	
V _{OD}	Differential Output Voltage	$R_L = 100\Omega$ Reduced swing RS=L	140	200	300	mV	
ΔV_{OD}	Change in V _{OD} between complementary output states	$R_L = 100\Omega$ $V_{OUT}=GND, R_L = 100\Omega$		-	-	35	
Voc	Common Mode Voltage			1.125	1.25	1.375	v
ΔV _{oc}	Change in V _{OC} between complementary output states			-	-	35	mV
Ios	Output Short Circuit Current			-	-	100	mA
I _{OZ}	Output TRI-State Current	/PDWN=L, V _{OUT} = GNI	O ~ LVDSVCC	-20	-	+20	μΑ

Table 5. LVDS Transmitter DC Specifications



Electrical Characteristics (Continued)

Power Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter Conditions Symbol Тур. Max Unit 33 24 CLKIN=37MHz (18)(26)MODE = H29 43 CLKIN=65MHz Single - out (23)(37) 30 46 CLKIN=72MHz (24)(40)48 65 CLKIN=89MHz (36)(53) MODE = L53 75 $R_L = 100\Omega$ Dual - out CLKIN=119MHz (41) (63) CL=5pF 56 Operating 82 DDRN = HCLKIN=139MHz \mathbf{I}_{TCCW} mA Current (44) (70)RS=H DDR Input Off 58 88 (RS=L) CLKIN=154MHz (46)(76) 47 64 CLKIN=44.5MHz (35) (52) MODE = L51 74 Dual - out CLKIN=59.5MHz (39) (62) 54 80 DDRN = LCLKIN=69MHz (42)(68) DDR Input On 56 85 CLKIN=77MHz (44)(73)Power Down /PDWN = L, All Inputs = Fixed L or H 140 1 **I**_{TCCS} μΑ Current

Table 6. Power Supply Current

(a) All Typ. values are at VCC=1.8V, Ta=25°C. The 256 Grayscale Test Pattern inputs test for a typical display pattern. (b) All Max. values are at VCC=1.98V, Ta=105°C . Worst Case Test Pattern produces maximum switching frequency for all the LVDS outputs (Fig.3).

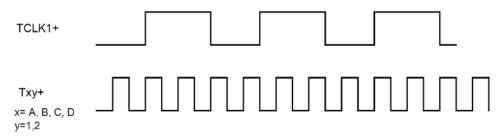


Figure 3. Test Pattern (LVDS Output Full Toggle Pattern)



Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwis	e specified.
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Table 7. Switching Characteristics											
Symbol	Parameter		Min	Тур	Max	Unit					
t _{TCIP}	CLKIN Period (Fig.7,8)		5.75	-	100	ns					
t _{TCH}	CLKIN High Time (Fig.7,8)	$0.35t_{TCIP}$	0.5t _{TCIP}	0.65t _{TCIP}	ns						
t _{TCL}	CLKIN Low Time (Fig.7,8)	$0.35t_{TCIP}$	0.5t _{TCIP}	0.65t _{TCIP}	ns						
t _{TS}	TTL Data Setup to CLK IN (Fig.7,8)	0.8	-	-	ns					
t _{TH}	TTL Data Hold to CLK IN (Fig.7,8))	0.8	-	-	ns					
	CLKIN to TCLK+/-	MODE=L,DDRN=H	9t _{TCIP} +3.1	-	9t _{TCIP} +8.0	ns					
t _{TCD}	Delay (Fig7,8)	Others	5t _{TCIP} +3.1	-	5t _{TCIP} +8.0	ns					
t _{TCOP}	TCLK1,2 Period (Fig.6)	5.75	-	100	ns						
t _{LVT}	LVDS Transition Time (Fig.4)	-	0.6	1.5	ns						
t _{TOP1}	Output Data Position0 (Fig.9)		-0.15	0.0	+0.15	ns					
t _{TOP0}	Output Data Position1 (Fig.9)		$\frac{t_{TCOP}}{7}$ -0.15	t _{TCOP} 7	$\frac{t_{TCOP}}{7}$ +0.15	ns					
t _{TOP6}	Output Data Position2 (Fig.9)		$2\frac{t_{TCOP}}{7}$ -0.15	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7}+0.15$	ns					
t _{TOP5}	Output Data Position3 (Fig.9)	$t_{\text{TCOP}} = 5.75 \text{ns} \sim 15 \text{ns}$	$3\frac{t_{TCOP}}{7}$ -0.15	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7}+0.15$	ns					
t _{TOP4}	Output Data Position4 (Fig.9)		$4\frac{t_{TCOP}}{7}$ -0.15	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7}+0.15$	ns					
t _{TOP3}	Output Data Position5 (Fig.9)		$5\frac{t_{TCOP}}{7}$ -0.15	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7}+0.15$	ns					
t _{TOP2}	Output Data Position6 (Fig.9)		$6\frac{t_{TCOP}}{7}$ -0.15	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7}+0.15$	ns					
t _{TPLL}	Phase Lock Time (Fig.5)		-	-	10.0	ms					
t _{DEINT}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		4t _{TCIP}	$t_{TCIP} * (2n)^{(a)}$	-	ns					
t _{DEH}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		2t _{TCIP}	$t_{TCIP} * (2m)^{(a)}$	-	ns					
t _{DEL}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		2t _{TCIP}	-	-	ns					

 Table 7. Switching Characteristics

(a) Refer to Fig.6 for details.



AC Timing Diagrams

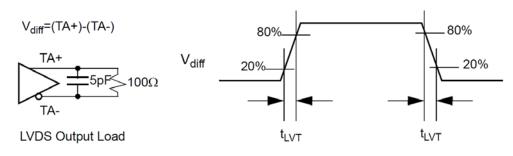
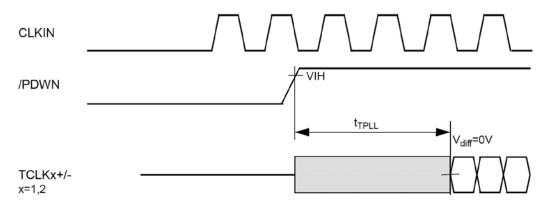
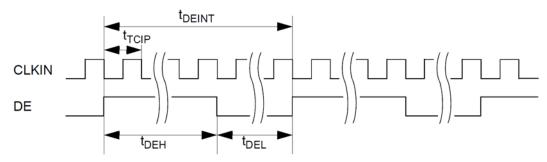
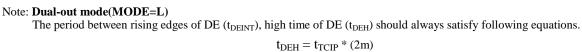


Figure 4. LVDS Output Load and Transition Time









 $t_{\text{DEINT}} = t_{\text{TCIP}} * (2n)$

m, n = integer

Figure 6. Dual-out mode DE input timing



AC Timing Diagrams(Continued)

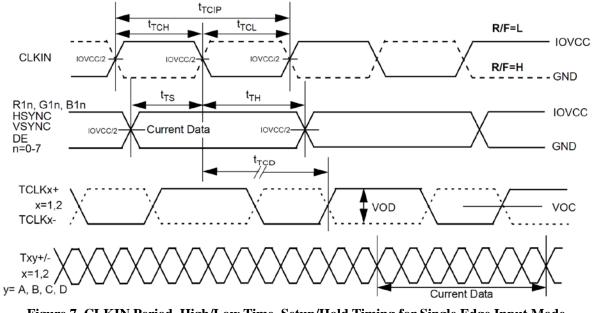


Figure 7. CLKIN Period, High/Low Time, Setup/Hold Timing for Single Edge Input Mode MODE = H or DDRN = H

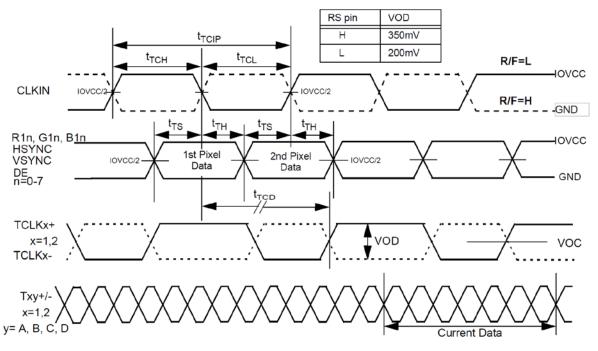


Figure 8. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode(DDR) MODE = L, DDRN = L



AC Timing Diagrams(Continued)

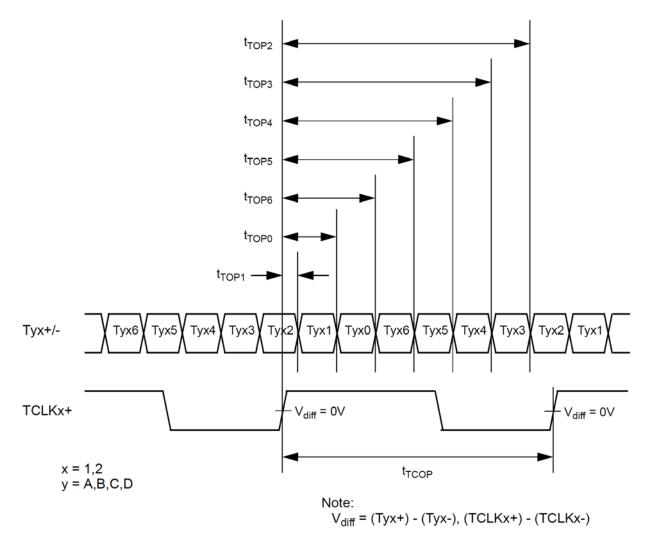


Figure 9. LVDS Output Data Position



$THC63LVD827\text{-}Q_Rev.1.20_E$

Single-In / Dual-Out Mode (MODE = L)

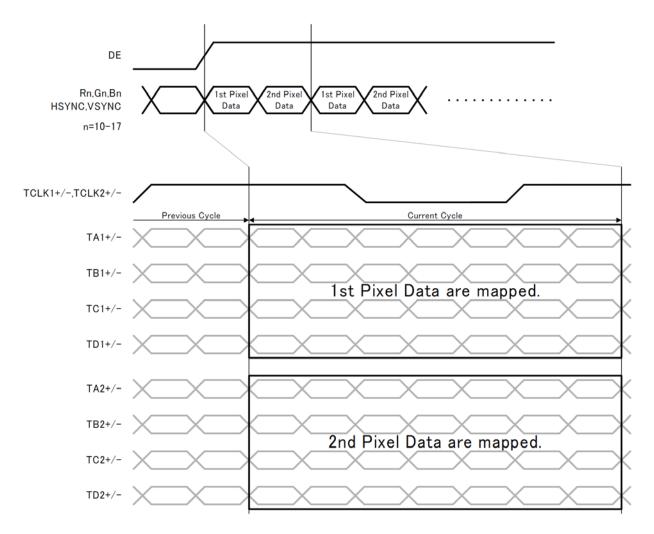


Figure 10. Single-In / Dual-Out Mode (MODE = L)



<u>Single-In / Single-Out Mode (MODE = H)</u>

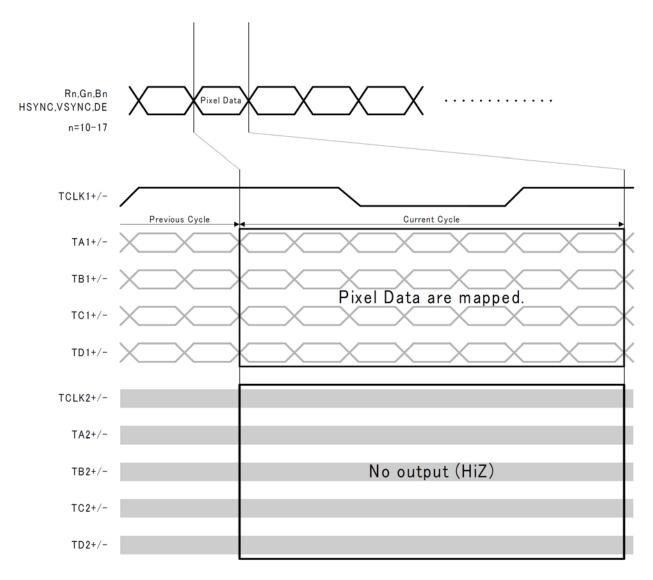


Figure 11. Single-In / Single-Out Mode (MODE = H)

$THC63LVD827\hbox{-}Q_Rev.1.20_E$



LVDS Data Mapping for 8 bit Mode (6B/8B = L)

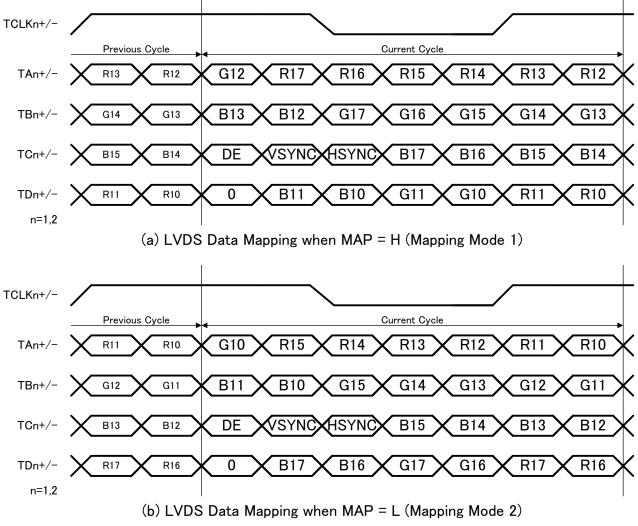
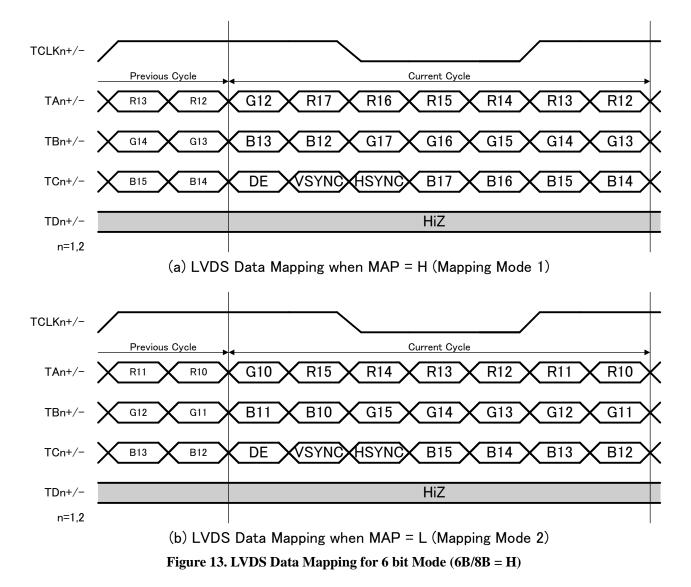


Figure 12. LVDS Data Mapping for 8 bit Mode (6B/8B = L)

$THC63LVD827\hbox{-}Q_Rev.1.20_E$



LVDS Data Mapping for 6 bit Mode (6B/8B = H)



Note: Input pins which are not used in 6 bit Mode (R10-11,G10-11,B10-11 on Mapping Mode 1, R16-17,G16-17,B16-17 on Mapping Mode 2) can be H, L, or Open.



Note

1) Cable Connection and Disconnection

Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect the each GND of the PCB which THC63LVD827-Q and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

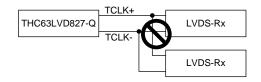
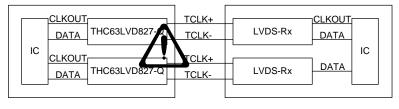


Figure 14. Multi Drop Connection

4) Asynchronous Use

Asynchronous use such as following systems are not recommended.



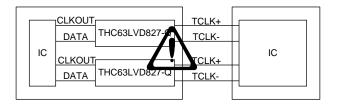


Figure 15. Asynchronous Use



Package

TFBGA

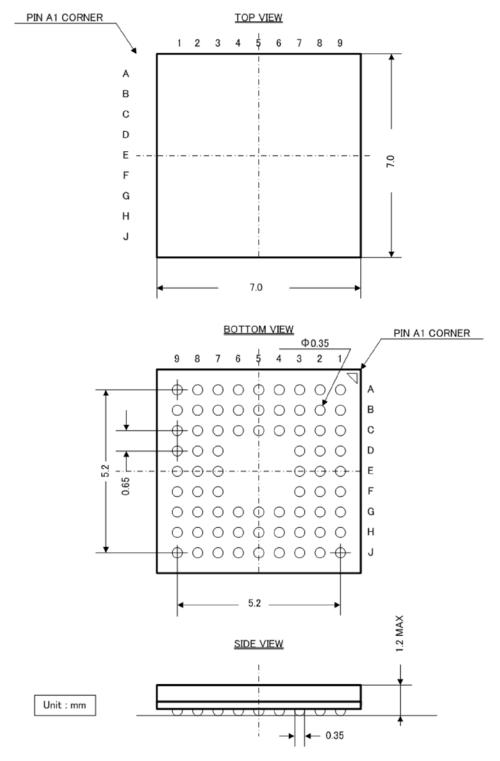


Figure 16. Package Diagram



Identification code

If a product has "-" in its product name, the product may have multiple product names and the figure/character after "-" is called "identification code". The identification code is B/D/F/G/H/L/Q or other figure/character(s) and it is used for THine internal product identification.

For example, the product "THC63LVD827-Q" may have other product name, like "THC63LVD827-B".



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- 5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
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THine Electronics, Inc.

sales@thine.co.jp