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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ517

Silicon P Channel MOS FET

REJ03G0874-0400
(Previous: ADE-208-575B)
Rev.4.00
Sep 07, 2005

Description

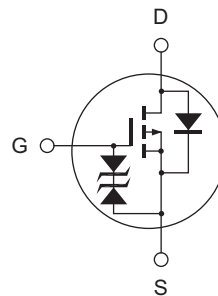
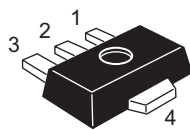
High speed power switching

Features

- Low on-resistance
 $R_{DS(on)} = 0.18 \Omega$ typ. (at $V_{GS} = -4 \text{ V}$, $I_D = -1 \text{ A}$)
- Low drive current
- High speed switching
- 2.5 V gate drive devices.

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK®)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "YY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	-20	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D	-2	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-4	A
Body to drain diode reverse drain current	I_{DR}	-2	A
Channel dissipation	P_{ch} ^{Note 2}	1	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 100 \mu s$, duty cycle $\leq 10\%$

2. When using the aluminium ceramic board (12.5 × 20 × 0.7 mm)

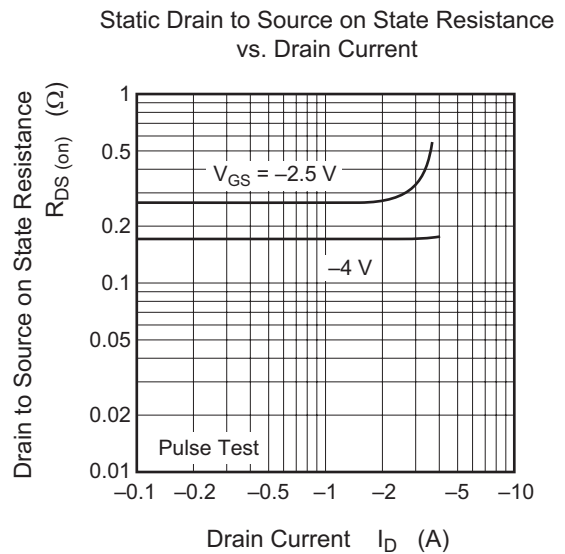
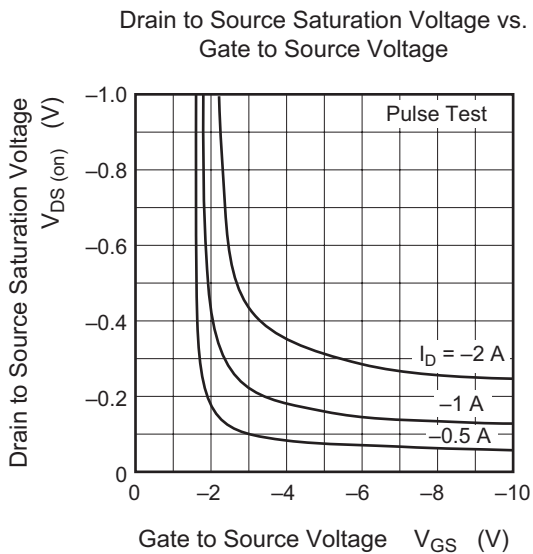
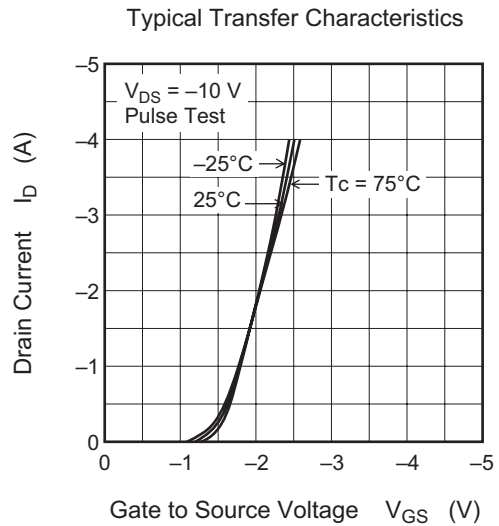
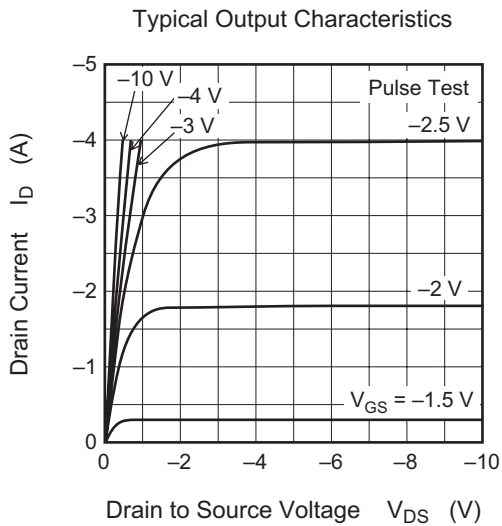
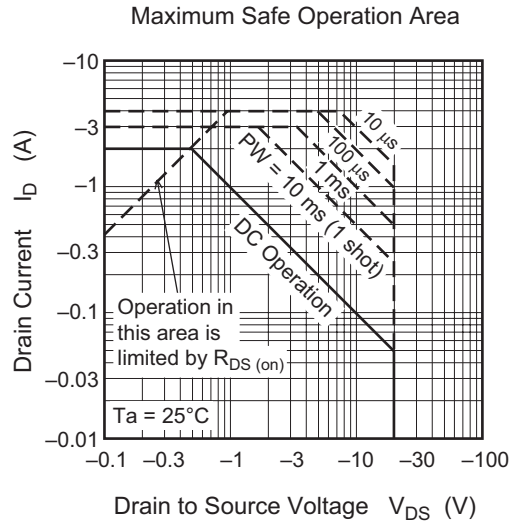
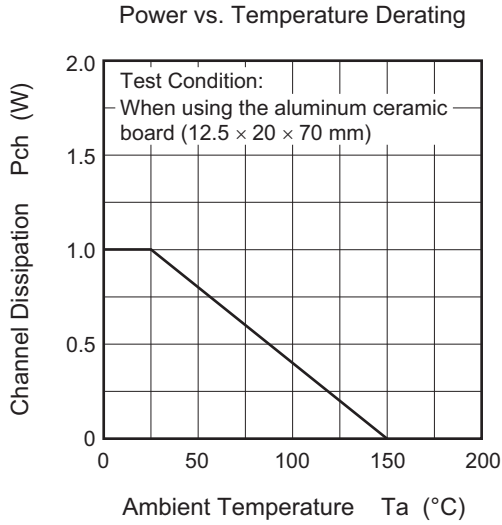
Electrical Characteristics

(Ta = 25°C)

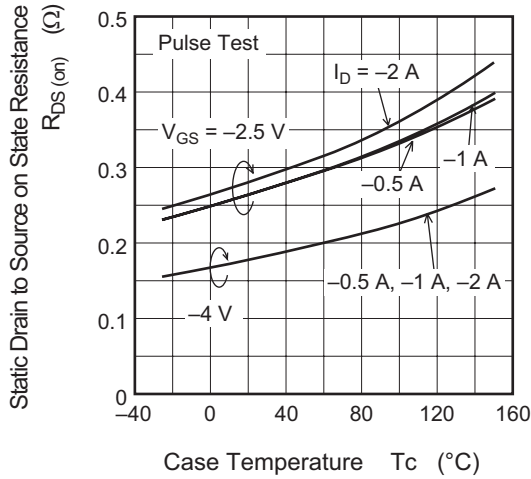
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 10	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.18	0.24	Ω	$I_D = -1 \text{ A}$, $V_{GS} = -4 \text{ V}$ ^{Note 3}
	$R_{DS(on)}$	—	0.27	0.43	Ω	$I_D = -1 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	1.8	3.0	—	S	$I_D = -1 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note 3}
Input capacitance	C_{iss}	—	320	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	90	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$V_{GS} = -4 \text{ V}$
Rise time	t_r	—	75	—	ns	$I_D = -1 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	$R_L = 10 \Omega$
Fall time	t_f	—	90	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-0.95	—	V	$I_F = -2 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -2 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

Note: 3. Pulse test

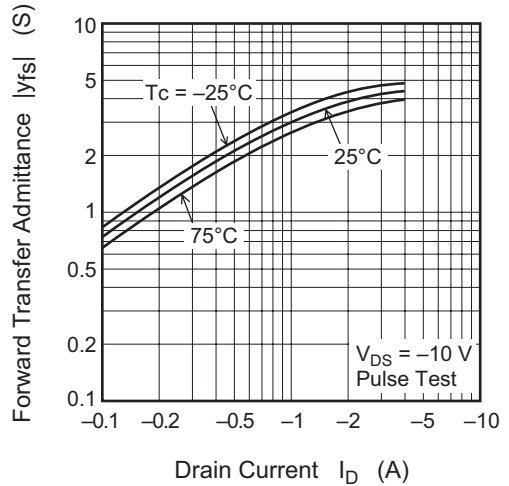
Main Characteristics



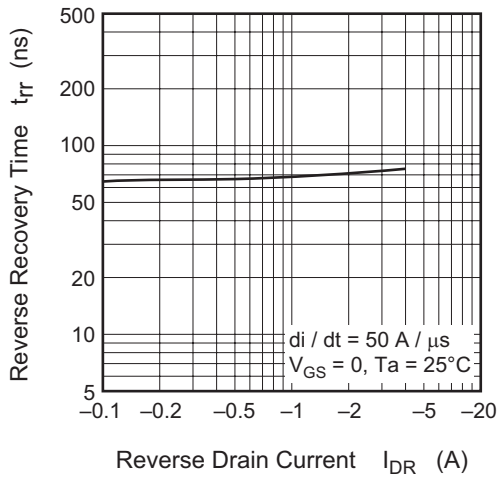
Static Drain to Source on State Resistance vs. Temperature



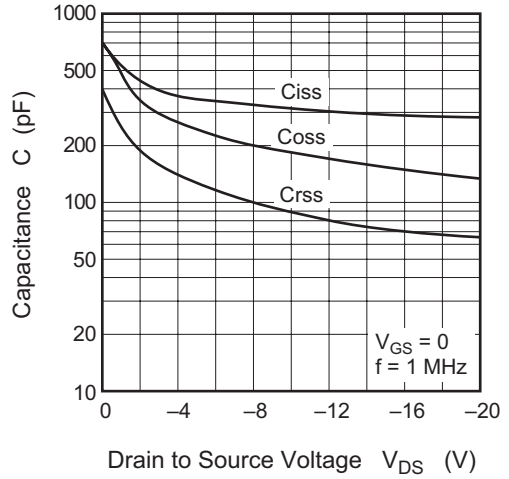
Forward Transfer Admittance vs. Drain Current



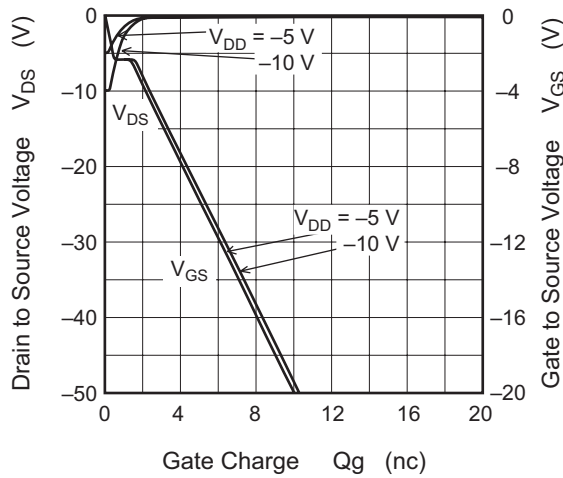
Body-Drain Diode Reverse Recovery Time



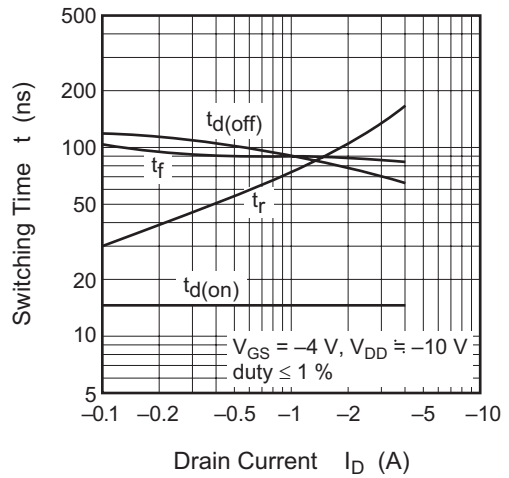
Typical Capacitance vs. Drain to Source Voltage



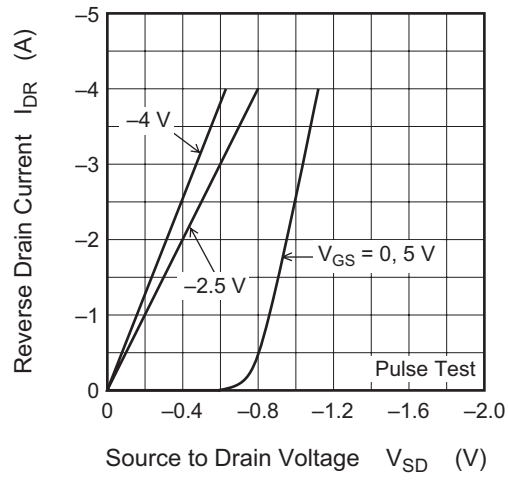
Dynamic Input Characteristics



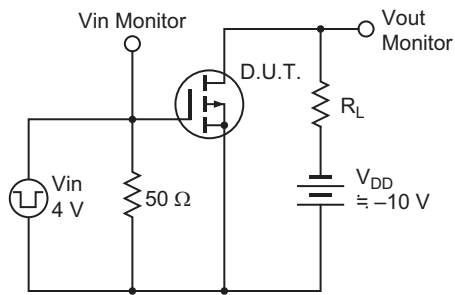
Switching Characteristics



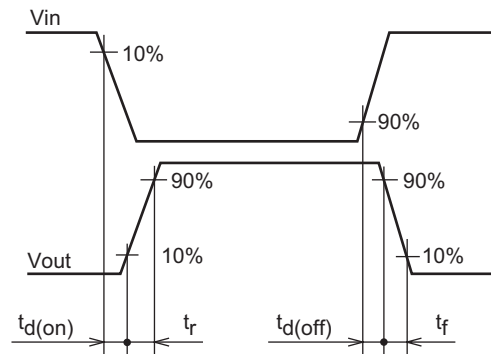
Reverse Drain Current vs. Source to Drain Voltage



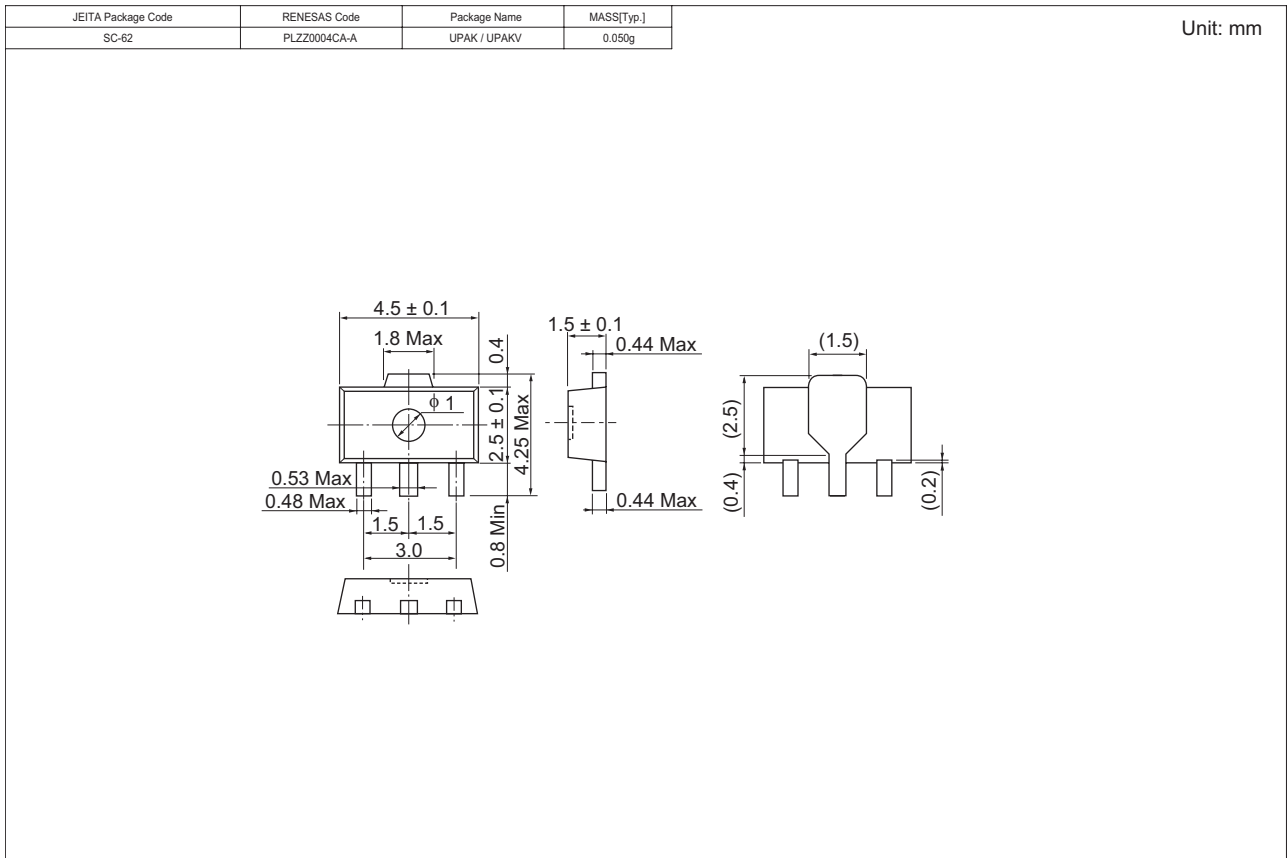
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ517YYTL-E	1000 pcs	Taping
2SJ517YYTR-E	1000 pcs	Taping

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