

## N-channel 600 V, 0.340 $\Omega$ typ., 11 A MDmesh™ M2 EP Power MOSFET in a DPAK package

Datasheet - production data

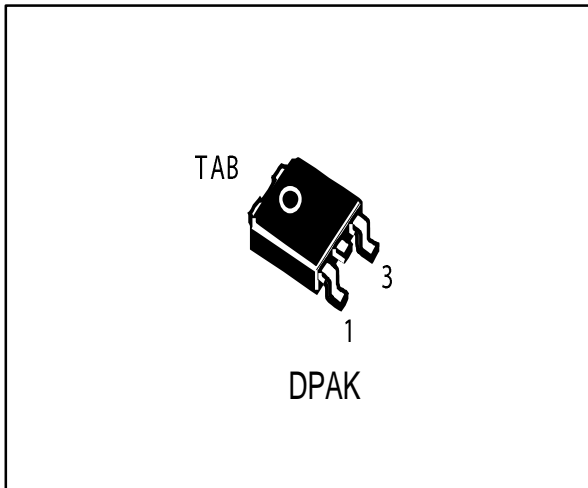
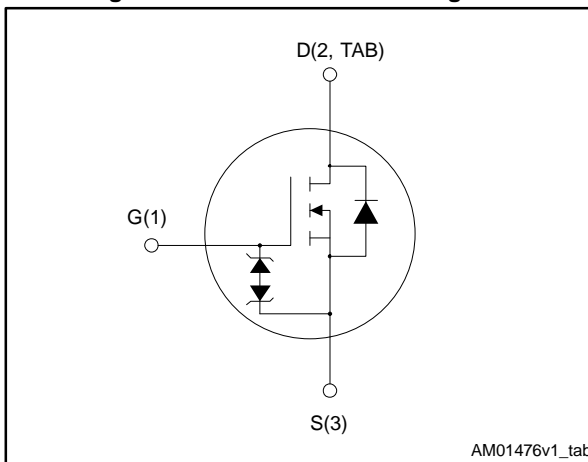


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD15N60M2-EP	650 V	0.378 $\Omega$	11 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD15N60M2-EP	15N60M2EP	DPAK	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	11	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature		

**Notes:**

(1)Pulse width limited by safe operating area.

(2) $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

(3) $V_{DS} \leq 480\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb max	50	°C/W

**Notes:**

(1)When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetetive or not repetetive (pulse width limited by $T_{jmax}$ )	2.8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	125	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$		0.340	0.378	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	590	-	pF
$C_{oss}$	Output capacitance		-	30	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	148	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 11\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	17	-	nC
$Q_{gs}$	Gate-source charge		-	3.1	-	nC
$Q_{gd}$	Gate-drain charge		-	7.3	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% $V_{GS}$ to 0% $I_D$ )	$V_{DD} = 400\text{ V}$ , $I_D = 1.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	4.7	-	$\mu\text{J}$
		$V_{DD} = 400\text{ V}$ , $I_D = 3.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	5.2	-	$\mu\text{J}$

Table 8: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 5.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	11	-	ns
$t_r$	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
$t_f$	Fall time		-	15	-	ns

Table 9: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 11\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	280		ns
$Q_{rr}$	Reverse recovery charge		-	2.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	400		ns
$Q_{rr}$	Reverse recovery charge		-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19		A

**Notes:**

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

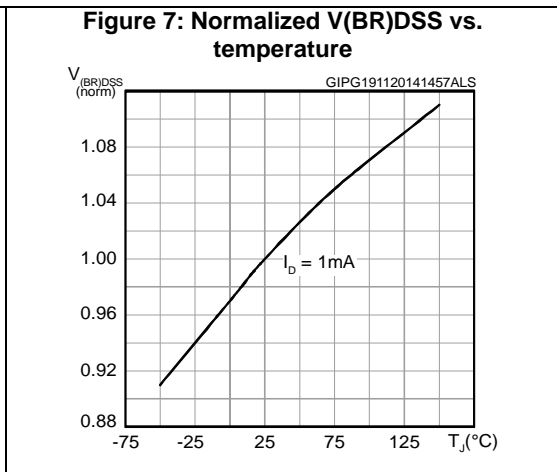
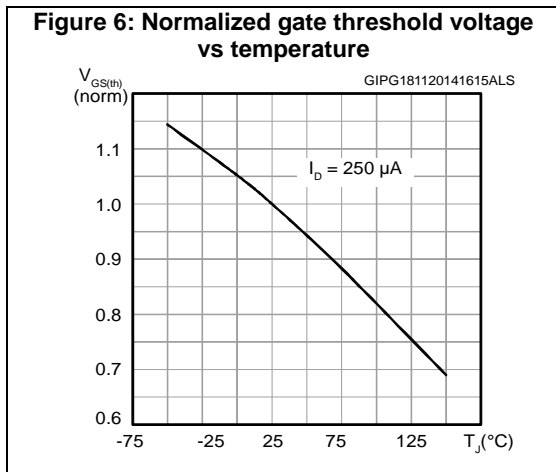
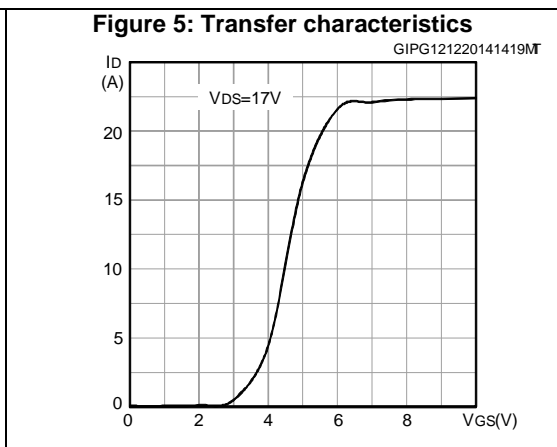
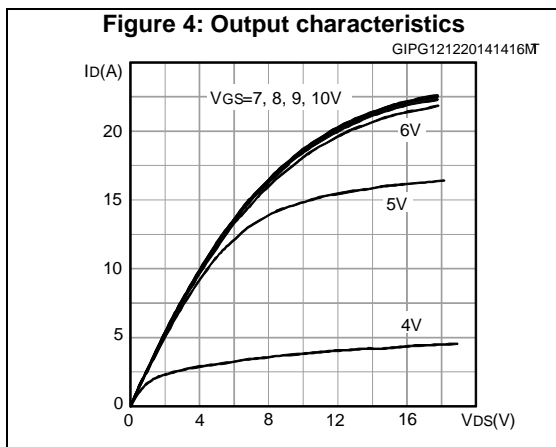
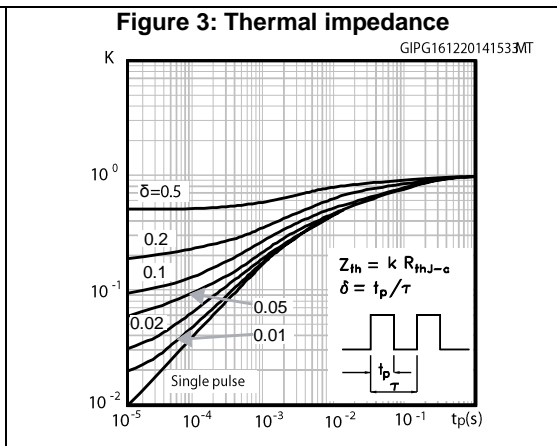
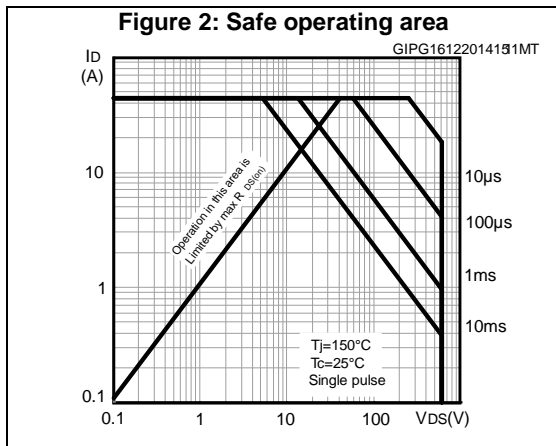


Figure 8: Static drain-source on-resistance

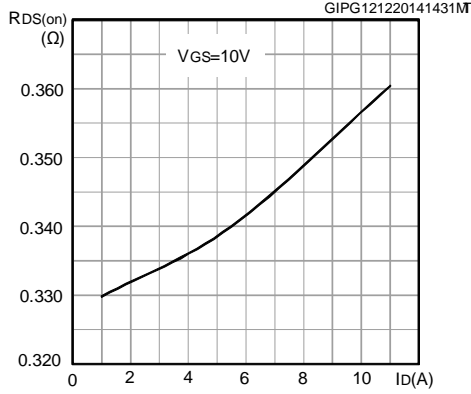


Figure 9: Normalized on-resistance vs temperature

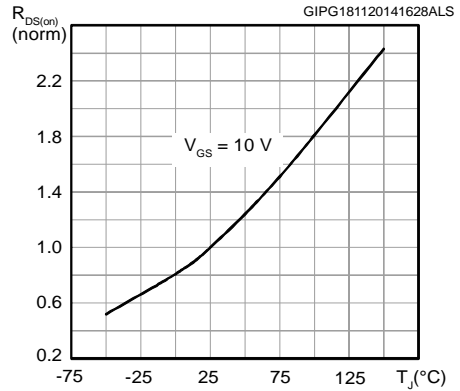


Figure 10: Gate charge vs. gate-source voltage

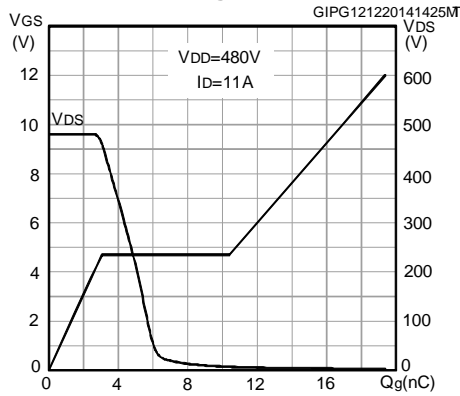


Figure 11: Capacitance variations

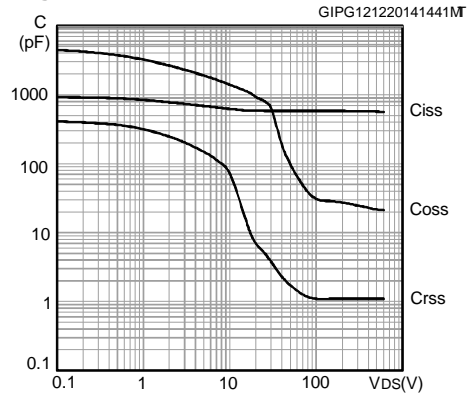


Figure 12: Turn-off switching loss vs drain current

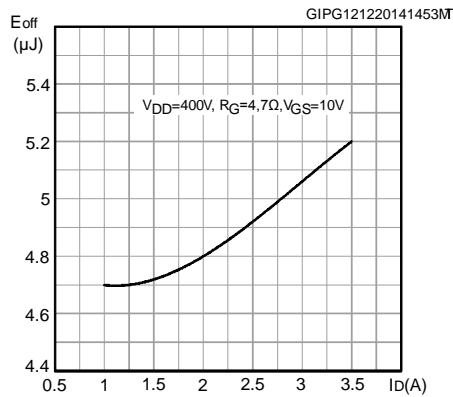
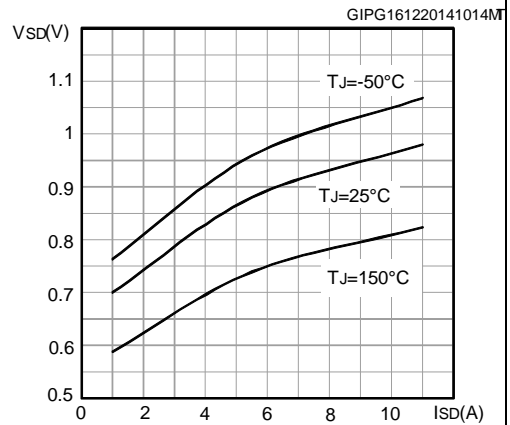
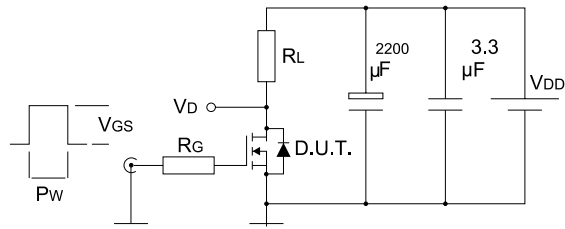


Figure 13: Source-drain diode forward characteristic



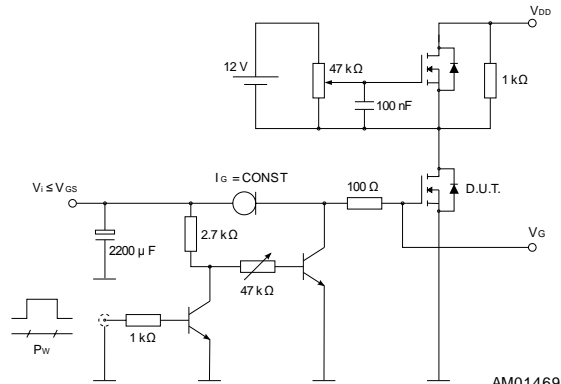
### 3 Test circuits

**Figure 14: Switching times test circuit for resistive load**



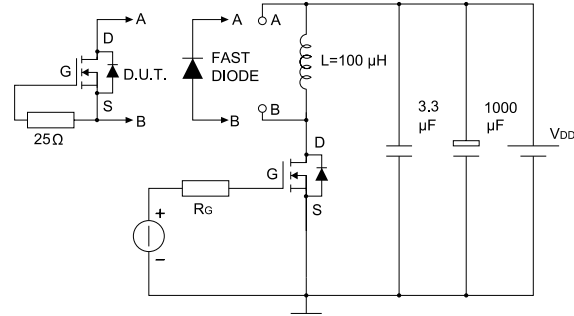
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**Figure 15: Gate charge test circuit**



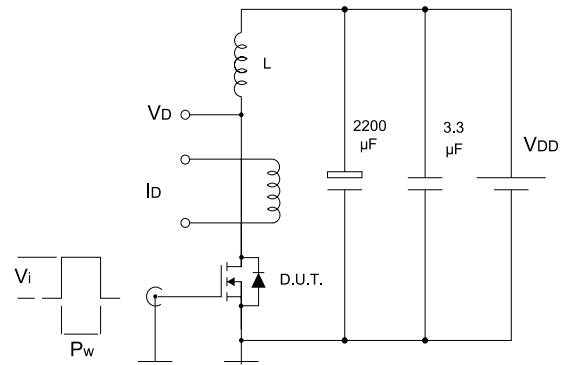
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



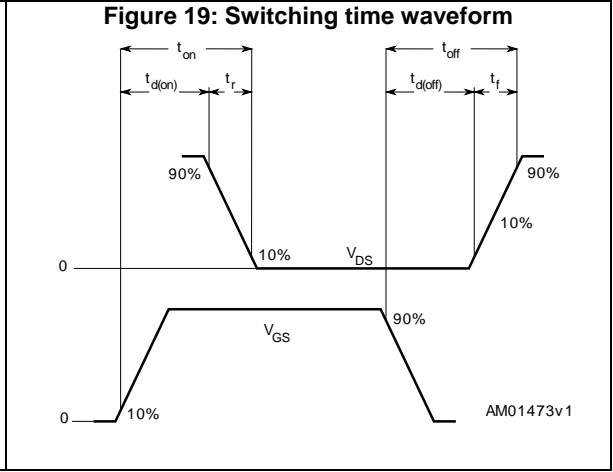
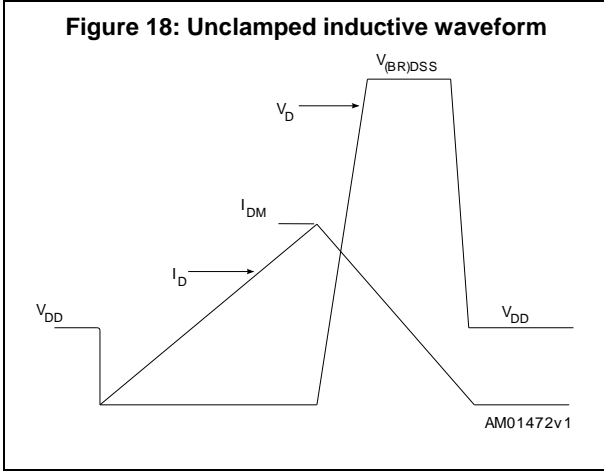
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**Figure 17: Unclamped inductive load test circuit**



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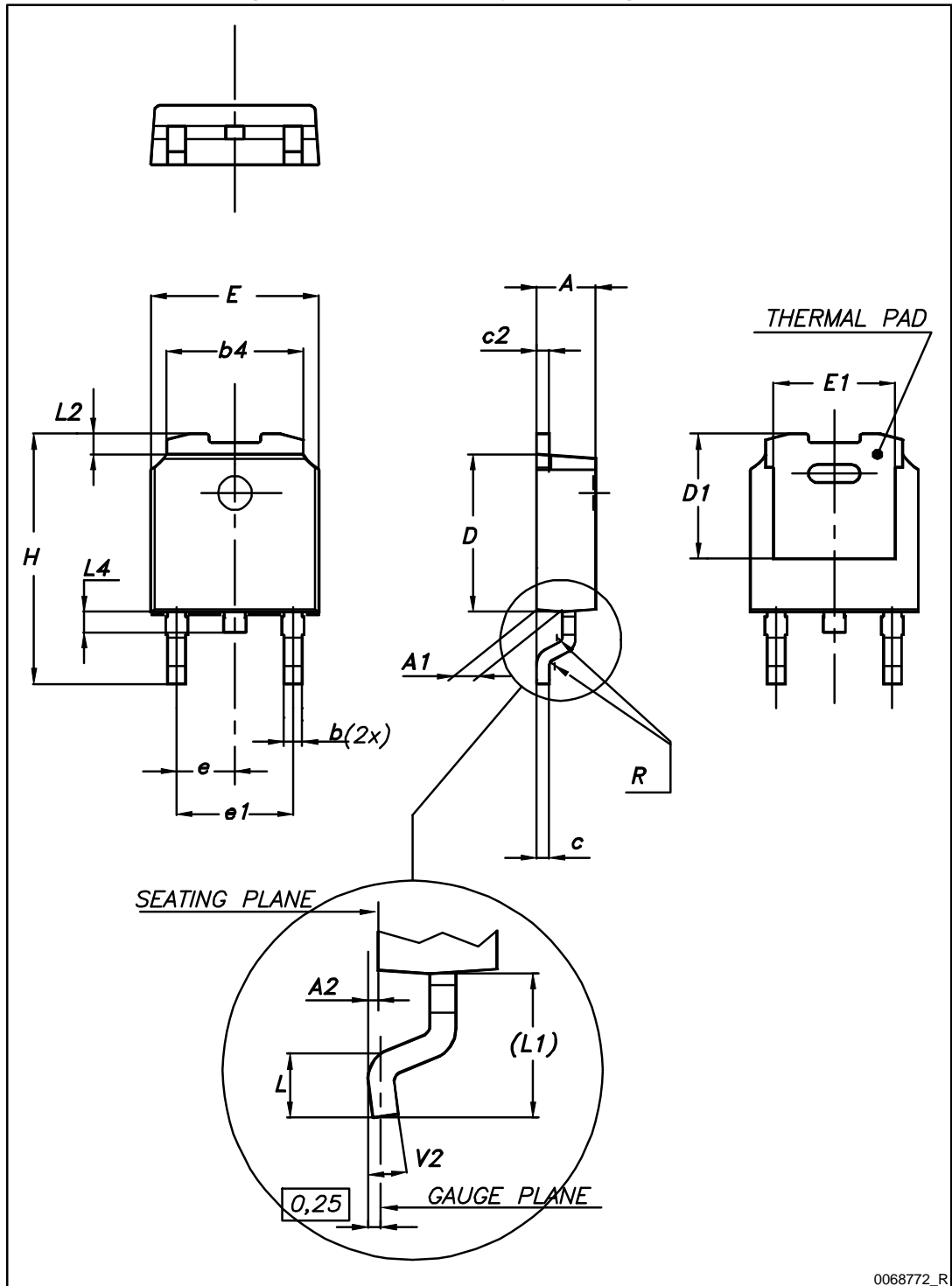


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK (TO-252) type A

Figure 20: DPAK (TO-252) type A package outline

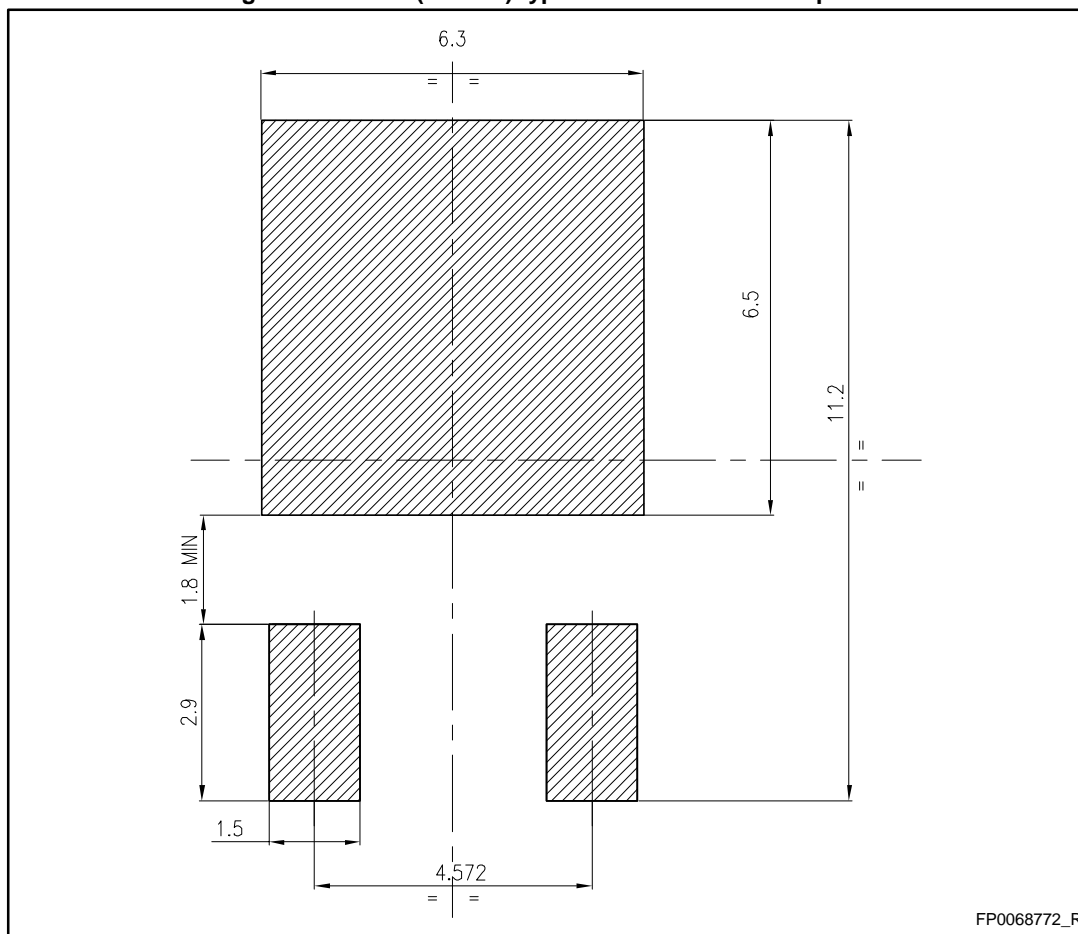


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Table 10: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) type A recommended footprint



All dimensions are in mm

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
16-Dec-2014	1	First release.

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