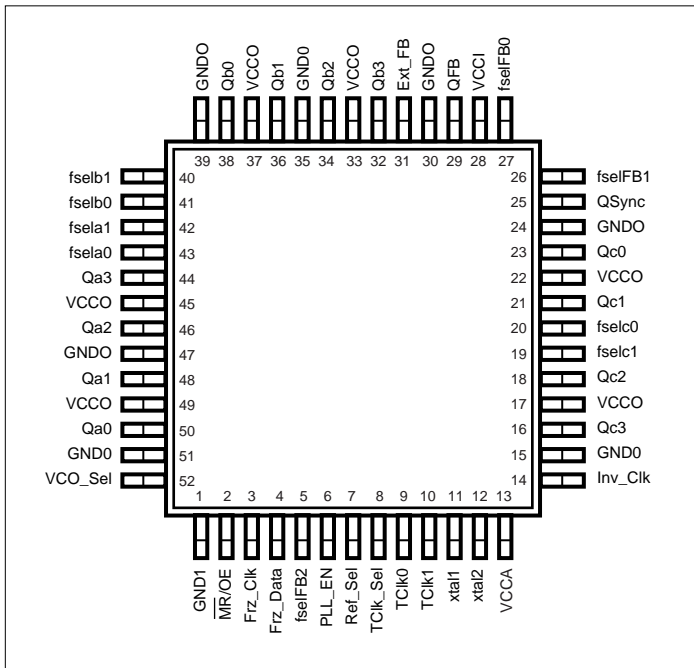


Low Voltage PLL Clock Driver

Features

- Fully Integrated PLL
- Output Frequency up to 125 MHz
- Compatible with PowerPC and Pentium Microprocessors
- 3.3V_{VCC}
- +100ps Typical Cycle-to-Cycle Jitter
- Packaging (Pb-free & Green available):
-52-pin LQFP (FC)

Pin Configuration



Description

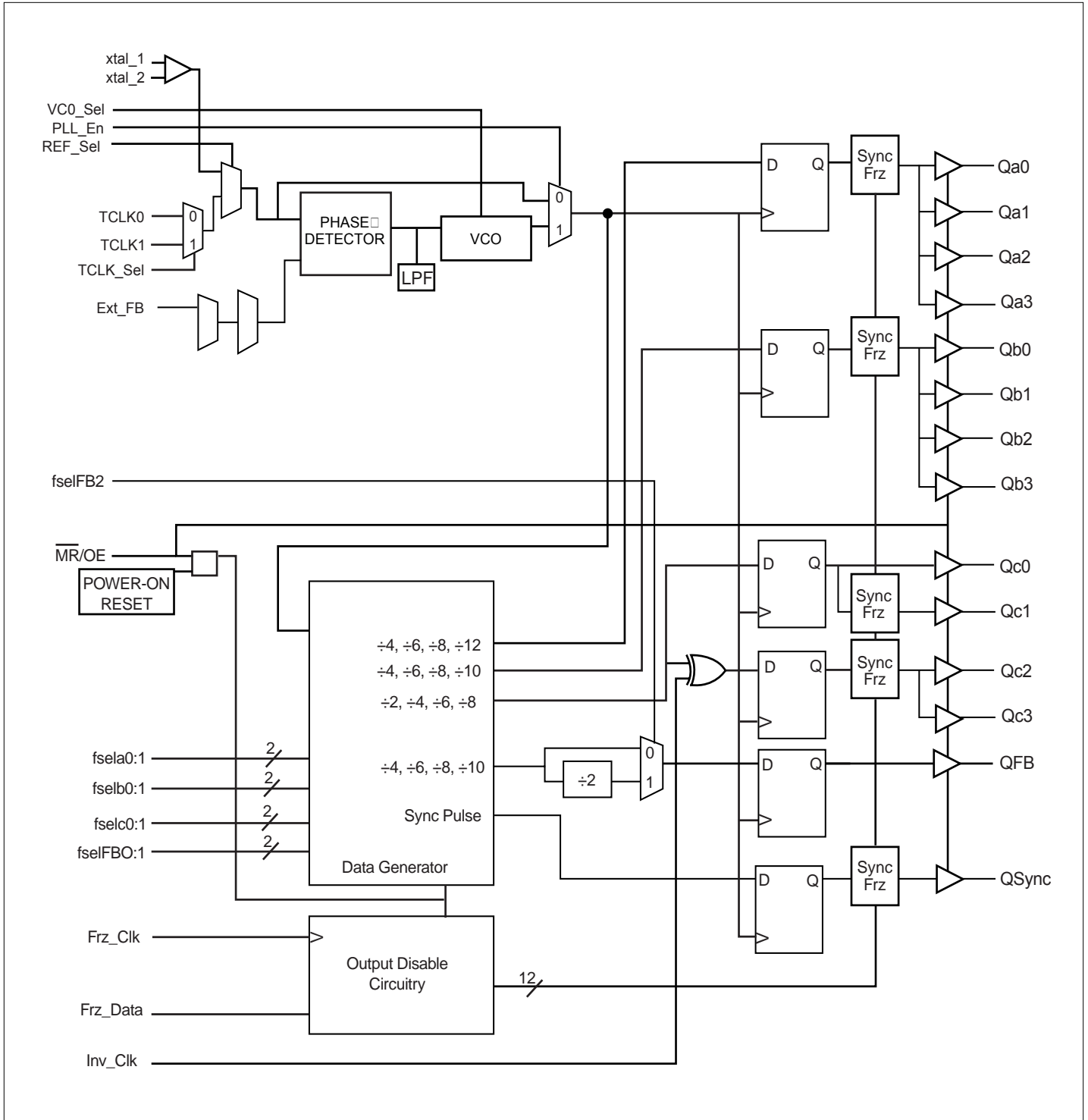
The PI6C2972 are 3.3V compatible, PLL based clock driver devices targeted for high-performance CISC or RISC processor based systems. With output frequencies of up to 125 MHz and skews of 550ps the PI6C2972 are ideally suited for most synchronous systems. The devices offer twelve low skew outputs plus a feedback and sync output for added flexibility and ease of system implementation.

The PI6C2972 features an extensive level of frequency programmability between the 12 outputs as well as the input vs output relationships. Using the select lines output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1 and 6:5 between outputs can be realized by pulsing low one clock edge prior to the coincident edges of the Qa and Qc outputs. The Sync output will indicate when the coincident rising edges of the above relationships will occur. The Power-On Reset ensures proper programming if the frequency select pins are set at power up. If the fselFB2 pin is held high, it may be necessary to apply a reset after power-up to ensure synchronization between the QFB output and the other outputs. The internal power-on reset is designed to provide this function, but with power-up conditions being dependent, it is difficult to guarantee. All other conditions of the fsel pins will automatically synchronize during PLL lock acquisition.

The PI6C2972 offers a very flexible output enable/disable scheme. Note that all of the control inputs on the PI6C2972 have internal pull-up resistors.

The PI6C2972 is fully 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50-ohm transmission lines. For series terminated lines each PI6C2972 output can drive two 50-ohm lines in parallel thus effectively doubling the fanout of the device.

Block Diagram



Function Table 1

| fsla1 | fsla0 | Qa | fselb1 | fselb0 | Qb | fselc1 | fselc0 | Qc |
|-------|-------|-----|--------|--------|-----|--------|--------|----|
| 0 | 0 | ÷4 | 0 | 0 | ÷4 | 0 | 0 | ÷2 |
| 0 | 1 | ÷6 | 0 | 1 | ÷6 | 0 | 1 | ÷4 |
| 1 | 0 | ÷8 | 1 | 0 | ÷8 | 1 | 0 | ÷6 |
| 1 | 1 | ÷12 | 1 | 1 | ÷10 | 1 | 1 | ÷8 |

Function Table 2

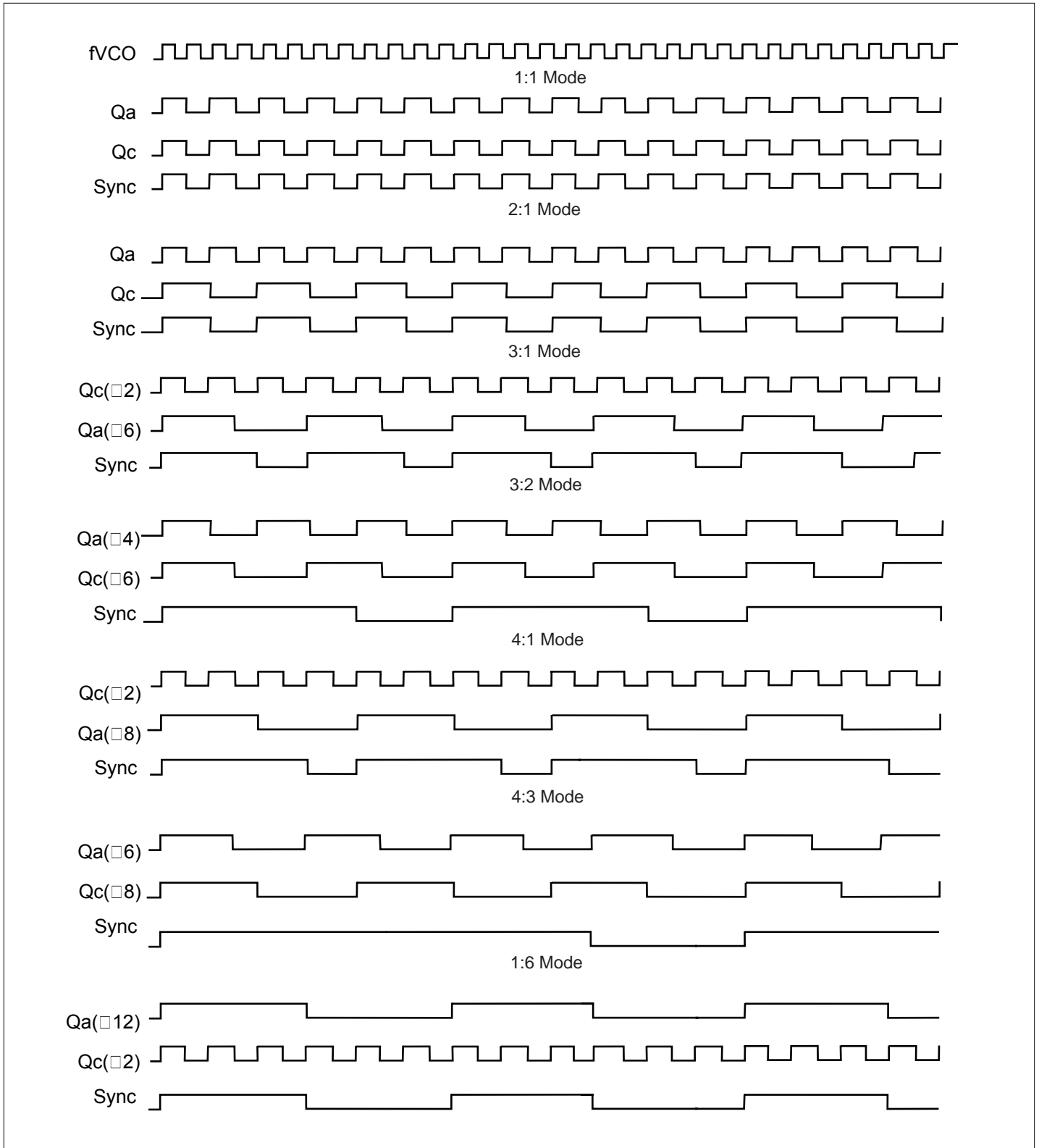
| fselFB2 | fselFB1 | fselFB0 | QFB |
|---------|---------|---------|-----|
| 0 | 0 | 0 | ÷4 |
| 0 | 0 | 1 | ÷6 |
| 0 | 1 | 0 | ÷8 |
| 0 | 1 | 1 | ÷10 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷12 |
| 1 | 1 | 0 | ÷16 |
| 1 | 1 | 1 | ÷20 |

Function Table 3

| Control Pin | Logic '0' | Logic '1' |
|-------------|--------------------------|-------------------|
| VCO_Sel | VCO/2 | VCO |
| Ref_Sel | TCLK | Xtal |
| TCLK_Sel | TCLK0 | TCLK1 |
| PLL_En | Bypass PLL | Enable PLL |
| MR/OE | Master Reset/Output Hi-Z | Enable Outputs |
| Inv_CLK | Non-Inverted Qc2, Qc3 | Inverted Qc2, Qc3 |

Crystal Recommendations

| Parameters | Value |
|-----------------------|-----------------------------|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Parallel Resonance |
| Freq. Tolernace | ±100ppm @ 25°C |
| Freq. Temp. Stability | ±175ppm (0° to 70°C) |
| Operating Range | 0° to 70°C |
| Shunt Capacitance | < 7pF |
| ESR | < 40-Ohm |
| Drive Level | 5mW |
| Aging | 5ppm / Year (First 3 years) |

Timing Diagrams


Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Units |
|-------------------|---------------------|------|-----------------------|-------|
| V _{CC} | Supply Voltage | -0.3 | 4.6 | V |
| V _I | Input Voltage | -0.3 | V _{DD} + 0.3 | V |
| I _{IN} | Input Current | | ±20 | mA |
| T _{STOR} | Storage Temperature | -40 | 125 | °C |

*Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 3.3V ± 5%)(4)

| Symbol | Conditions | Characteristic | Min. | Typ. | Max. | Units |
|------------------|---------------------------------------|----------------------------------|------|------|------|-------|
| V _{IH} | | Input HIGH Voltage | 2.0 | | 3.6 | V |
| V _{IL} | | Input LOW Voltage | | | 0.8 | |
| V _{OH} | I _{OH} = 20mA ⁽²⁾ | Output HIGH Voltage | 2.4 | | | |
| V _{OL} | I _{OL} = 20mA ⁽²⁾ | Output LOW Voltage | | | 0.5 | |
| I _{IN} | Note 3 | Input Current | | | ±120 | μA |
| I _{CC} | | Maximum Quiescent Supply Current | | 190 | 215 | mA |
| I _{CCA} | | Analog V _{CC} Current | | 15 | 20 | |
| C _{IN} | | Input Capacitance | | | 4 | pF |
| C _{pd} | Per Output | Power Dissipation Capacitance | | 25 | | |

Notes:

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
2. The PI6C2972 outputs can drive series or parallel terminated 50 Ohm (or 50 Ohm to V_{CC}/2) transmission lines on the incident edge.
3. Inputs have pull-up/pull-down resistors which affect input current.
4. Special thermal handling may be required in some configurations.

PLL Input Reference Characteristic ($T_A = 0^\circ\text{C}$ to 70°C)

| Symbol | Conditions | Characteristics | Min. | Max. | Units |
|-------------|------------|------------------------------|--------|-------------|-------|
| t_r, t_f | | TCLK Input Rise/Falls | | 3.0 | ns |
| f_{ref} | Note 5 | Reference Input Frequency | Note 5 | 100, Note 5 | MHz |
| f_{refDC} | | Reference Input Duty Cycle | 25 | 75 | % |
| t_{xtal} | | Crystal Oscillator Frequency | 10 | 25 | MHz |

Notes:

5. Maximum input reference frequency is limited by the VCO lock range and the feedback divider or 100 MHz, minimum input reference frequency is limited by the VCO lock range and the feedback divider.

AC Characteristics ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 5\%$)

| Symbol | Characteristics | Conditions | Min. | Typ. | Max. | Units | |
|--------------------|---|----------------|-----------------------|----------------------------|------------------------|-------|----|
| t_r, t_f | Output Rise/Fall Time (Note7) | 0.8 to 2.0V | 0.15 | | 1.2 | ns | |
| t_{pw} | Output Duty Cycle (Note7) | | $t_{CYCLE}/2$ -750 | $t_{CYCLE}/2$ ± 500 | $t_{CYCLE}/2$ +750 | ps | |
| t_{pd} | Propagation Delay Notes 7, 8, QFB = $\div 8$ | TCLK0 TCLK1 | -270 -330 | 130 70 | 530 470 | | |
| t_{os} | Output-to-Output Skew | Note 7 | | | 550 | | |
| f_{VCO} | VCO Lock Range | | 200 | | 480 | MHz | |
| f_{max} | Maximum Output Frequency Q ($\div 2$) Q ($\div 4$) Q ($\div 6$) Q ($\div 8$) | Note 7 | | | 125 120 80 60 | | |
| t_{jitter} | Cycle-to-Cycle Jitter (Peak-to-Peak) | | | ± 100 | | | ps |
| t_{PLZ}, t_{PHZ} | Output Disable Time | | 2 | | 8 | | ns |
| t_{PZL}, t_{PZH} | Output ENable Time | | 2 | | 10 | | |
| t_{lock} | Maximum PLL Lock Time | | | | 10 | ms | |
| f_{MAX} | Maximum Frz_Clk Frequency | | | | 20 | MHz | |

Notes:

7. 50 Ohm transmission line terminated into $V_{CC}/2$

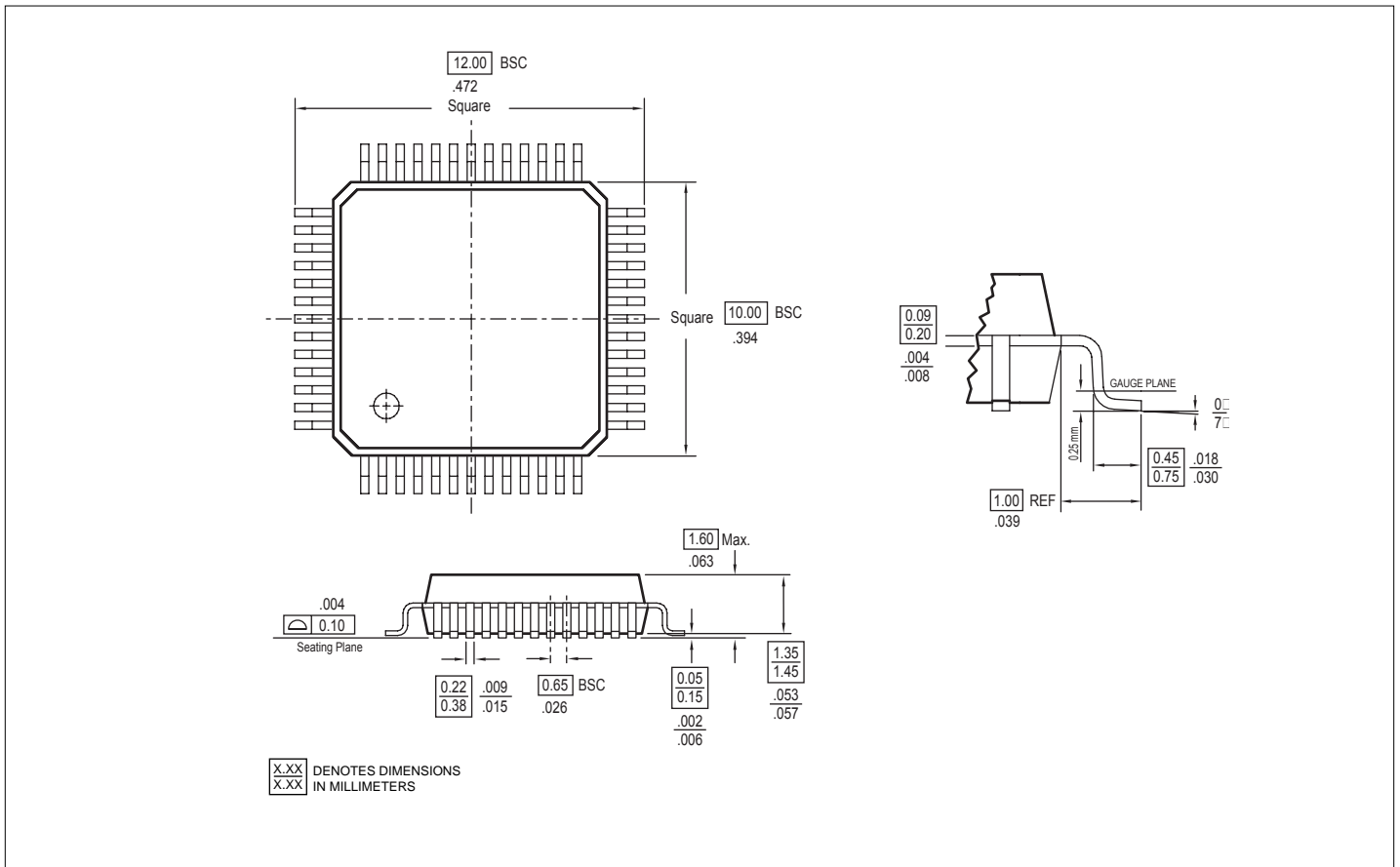
8. t_{pd} is specified for a 50 MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

| | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|-----|-----|
| Start Bit | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 |
|-----------|----|----|----|----|----|----|----|----|----|----|-----|-----|

D0–D3 are the control bits for Qa0–Qa3, respectively
D4–D7 are the control bits for Qb0–Qb3, respectively
D8–D10 are the control bits for Qc1–Qc3, respectively
D11 is the control bit for QSync

Freeze Data Input Protocol

Packaging Mechanical: 52-Pin LQFP (FC)



Ordering Information

| Ordering Code | Package Code | Package Type |
|---------------|--------------|------------------------------|
| PI6C2972FC | FC | 52-pin LQFP |
| PI6C2972FCE | FC | Pb-free & Green, 52-pin LQFP |

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/