MN103SK0/K1 Series

32-bit Single-chip Microcontroller

■ Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors, arithmetic unit for speed-up of inverter control and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on chip for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN103SFK0K	256 KB	8 KB	Flash EEPROM version	QFP100-P-1818B
MN103SFK1K				LQFP080-P-1414A TQFP080-P-1212D

■ Features

- CPU core

  MN103S core
  4 GB of linear address space (for instructions / data)
  LOAD/STORE architecture with 5-stage pipeline
  46 basic instructions + 23 extension instructions
  6 addressing modes
  Instruction set of 1 byte in word length
  Extension arithmetic unit incorporated (high-speed multiply, multiply and accumulate and saturation operation instructions)
  Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)
  Operation mode: NORMAL mode, SLEEP mode, HALT mode, STOP mode

- Oscillation circuit

  External oscillation (crystal/ ceramic), Internal oscillation (10 MHz)

- ROM correction

  Maximum 4 parts in a program

- Internal memory

  ROM 256 Kbytes
  RAM 8 Kbytes

- Interrupts

  Internal interrupts: MN103SFK0K: 54 interrupts / MN103SFK1K: 54 interrupts
  Watchdog timer overflow interrupts
  System error interrupts
  Fail safe function interrupts
  <Timer Interrupts>
  Timer 0 underflow interrupts
  Timer 1 underflow interrupts
  Timer 2 underflow interrupts
  Timer 3 underflow interrupts
  Timer 4 underflow interrupts
  Timer 5 underflow interrupts
  Timer 6 underflow interrupts
  Timer 7 underflow interrupts
  Timer 8 underflow interrupts
  Timer 9 underflow interrupts
  Timer 10 underflow interrupts
  Timer 11 underflow interrupts
  Timer 16 overflow/underflow interrupt
  Timer 16 compare/capture A interrupt
  Timer 16 compare/capture B interrupt
  Timer 17 overflow/underflow interrupt
  Timer 17 compare/capture A interrupt
  Timer 17 compare/capture B interrupt
  Timer 18 overflow/underflow interrupt
  Timer 18 compare/capture A interrupt
  Timer 18 compare/capture B interrupt
  Timer 19 overflow/underflow interrupt
  Timer 19 compare/capture A interrupt
  Timer 19 compare/capture B interrupt
  Timer 20 overflow/underflow interrupt
  Timer 20 compare/capture A interrupt
  Timer 20 compare/capture B interrupt

■ Features (continued)

• Interrupts (continued)

<Timer Interrupts> (continued)

Timer 21 overflow/underflow interrupt
Timer 21 compare/capture A interrupt
Timer 21 compare/capture B interrupt
Timer 23 overflow/underflow interrupt
Timer 23 compare/capture A interrupt
Timer 23 compare/capture B interrupt

<Serial Interface>

Serial 0 reception end interrupts
Serial 0 transmission end interrupts
Serial 1 reception end interrupts
Serial 1 transmission end interrupts
Serial 2 reception end interrupts
Serial 2 transmission end interrupts
Serial 3 reception end interrupts
Serial 3 transmission end interrupts

<PWM>

PWM0 overflow interrupts of PWM cycle
PWM0 underflow interrupts
PWM1 overflow interrupts of PWM cycle
PWM1 underflow interrupts

<A/D interrupt>

A /D 0 conversion end interrupt
A /D 0 conversion end B interrupt
A /D 1 conversion end interrupt
A /D 1 conversion end B interrupt
A /D 2 conversion end interrupt
A /D 2 conversion end B interrupt

External interrupts: MN103SFK0K: 16 interrupts / MN103SFK1K: 12 interrupts

IRQ0: Edge, both edges, level interrupts, noise filter connectable
IRQ1: Edge, both edges, level interrupts, noise filter connectable
IRQ2: Edge, both edges, level interrupts, noise filter connectable
IRQ3: Edge, both edges, level interrupts, noise filter connectable
IRQ4: Edge, both edges, level interrupts, noise filter connectable
IRQ5: Edge, both edges, level interrupts, noise filter connectable
IRQ6: Edge, both edges, level interrupts, noise filter connectable
IRQ7: Edge, both edges, level interrupts, noise filter connectable
IRQ8: Edge, both edges, level interrupts, noise filter connectable
IRQ9: Edge, both edges, level interrupts, noise filter connectable
IRQ10: Edge, both edges, level interrupts, noise filter connectable
IRQ11: Edge, both edges, level interrupts, noise filter connectable
IRQ12: Edge, both edges, level interrupts, noise filter connectable (only MN103SFK0K)
IRQ13: Edge, both edges, level interrupts, noise filter connectable (only MN103SFK0K)
IRQ14: Edge, both edges, level interrupts, noise filter connectable (only MN103SFK0K)
IRQ15: Edge, both edges, level interrupts, noise filter connectable (only MN103SFK0K)

■ Features (continued)

- Timer counter

8-bit timer for general use 16 sets
16-bit timer for general use 7 sets

Timer 0 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Baud rate timer
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 1 underflow, Timer 2 underflow, TM0IO pin input

Timer 1 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection (connected to Timer 0)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 2 underflow, TM1IO pin input

Timer 2 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection (connected to Timer 1)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow, TM2IO pin input

Timer 3 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection (connected to Timer 2)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow, Timer 2 underflow, TM3IO pin input

Timer 4 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 5 underflow, Timer 6 underflow, TM4IO pin input

Timer 5 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 4)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 4 underflow, Timer 6 underflow, TM5IO pin input

Timer 6 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 5)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 4 underflow, Timer 5 underflow, TM6IO pin input

Timer 7 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (connected to Timer 6)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 4 underflow, Timer 5 underflow, Timer 6 underflow, TM7IO pin input

Timer 8 (8-bit Timer for general use)
Interval timer, Timer pulse output, Event count
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM8IO pin input Timer 9 underflow, Timer 10 underflow

Timer 9 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 8)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM9IO pin input Timer 8 underflow, Timer 10 underflow

■ Features (continued)

- Timer counter (continued)

Timer 10 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 9)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM10IO pin input
Timer 8 underflow, Timer 9 underflow

Timer 11 (8-bit timer for general use)
Interval timer, Timer pulse output, Event count, Cascade connection (Connected to Timer 10)
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM11IO pin input
Timer 8 underflow, Timer 9 underflow, Timer 10 underflow

Timer 16 (16-bit timer for general use)
Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, IOCLK/64, Timer 7 underflow, TM16BIO pin input

Timer 17 (16-bit timer for general use)
Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, IOCLK/64, Timer 11 underflow, TM17BIO pin input

Timer 18 (16-bit timer for general use)
Interval timer, Event count, Up/down count, Timer output, PWM output (output to 6 ports all at once is possible),
Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, Timer 6 underflow, Timer 7 underflow, TM18BIO pin input

Timer 19 (16-bit timer for general use)
Interval timer, Event count, Up/down count, Timer output, PWM output, Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, Timer 10 underflow, Timer 11 underflow, TM19BIO pin input

Timer 20 (16-bit timer for general use)
Interval timer, Event count *, Up/down count, Timer output *, PWM output *, Input capture *, one-shot output *,
External trigger start *, Start by PWM0 overflow/underflow interrupt, A/D conversion start trigger generation
Count clock source: MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 6 underflow,
Timer 7 underflow, TM20BIO pin input * *: only MN103SFK0K

Timer 21 (16-bit timer for general use)
Interval timer, Event count *, Up/down count, Timer output *, PWM output *, Input capture *, one-shot output *,
External trigger start *, PWM1 overflow/underflow interrupt, A/D conversion start trigger generation
Count clock source: MCLK, MCLK/8, IOCLK, IOCLK/8, Timer 10 underflow,
Timer 11 underflow, TM21BIO pin input * *: only MN103SFK0K

Timer 23 (16-bit timer for general use)
Interval timer, Event count, Up/down count, Timer output, PWM output (output to 6 ports all at once is possible),
Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, Timer 10 underflow, Timer 11 underflow, TM23BIO pin input

- Watchdog Timer

Detection time 6.55 ms to 1677.72 ms (oscillation frequency 10 MHz)
Generates non-maskable interrupt at detection
Generates hard-reset at second consective overflow

■ Features (continued)

- A /D Converter

  Minimum conversion time 1.0 µs

  MN103SFK0K: 20 channels, 3 converters

  MN103SFK1K: 16 channels, 3 converters

  Use of 3 converters allows simultaneous sampling of 3 phases

  A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer

- Complementary 3-phase PWM output

  Min. resolution: 16.7 ns

  Triangular and saw-tooth waves output

  Incorporates a dead time insertion circuit

  Can overwrite registers by double buffer during PWM operation

  PWM output protection circuit supporting external interrupts and non-maskable interrupt

  Output timing varying function

- Serial Interface 4 channels

  Serial 0 (Multi-master IIC / Synchronous serial interface)

  Synchronous serial interface

  Overrun error detection

  Transfer clock source: 1/2, 1/4, 1/16 and 1/32 of timer 0 underflow,
  1/2, 1/4, 1/16 and 1/32 of timer 1 underflow,
  1/2, 1/4, 1/16 and 1/32 of timer 2 underflow,
  1/2, 1/4, 1/16 and 1/32 of timer 3 underflow, IOCLK/2, IOCLK/4, SBT0 pin

  Can be selected as the first bit to be transferred, Any transfer size from 1 to 8 bits can be selected.

  Can be continuously transmitted, received or transmitted and received.

  Maximum transfer rate: 5.0 Mbps

  Multi-master IIC

  7-bit or 10-bit slave address can be set.

  Supports General call communication mode.

■Features (continued)

- Serial Interface (continued)

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Overrun error detection

Transfer clock source: 1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow, IOCLK/2, IOCLK/4, SBT1 pin

Can be selected as the first bit to be transferred, Any transfer size from 1 to 8 bits can be selected.

Continuous transmission, reception, and transmission/reception

Maximum transfer rate: 5.0 Mbps

Full duplex UART

Parity check, Overrun and flaming error detection

Transfer clock source: 1/32, 1/64, 1/256, and 1/1024 of timer 0 underflow,
1/32, 1/64, 1/256, and 1/1024 of timer 1 underflow,
1/32, 1/64, 1/256, and 1/1024 of timer 2 underflow,
1/32, 1/64, 1/256, and 1/1024 of timer 3 underflow, IOCLK/32, IOCLK/64

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Continuous transmission, reception, and transmission/reception

Maximum transfer rate: 300 kbps

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Parity check, Overrun error detection

Transfer clock source: 1/2 and 1/16 of timer 0 underflow,
1/2 and 1/16 of timer 1 underflow,
1/2 and 1/16 of timer 2 underflow,
1/2 and 1/16 of timer 3 underflow, SBT2 pin

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Maximum transfer rate: 3.0 Mbps

Full duplex UART

Parity check, Overrun and flaming error detection

Transfer clock source: 1/16 of timer 0 underflow, 1/16 of timer 1 underflow,
1/16 of timer 2 underflow, 1/16 of timer 3 underflow

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Maximum transfer rate: 375 kbps

Serial 3 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Parity check, Overrun error detection

Transfer clock source: 1/2 and 1/16 of timer 0 underflow,
1/2 and 1/16 of timer 1 underflow,
1/2 and 1/16 of timer 2 underflow,
1/2 and 1/16 of timer 3 underflow, SBT3 pin

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Maximum transfer rate: 3.0 Mbps

Full duplex UART

Parity check, Overrun and flaming error detection

Transfer clock source: 1/16 of timer 0 underflow, 1/16 of timer 1 underflow,
1/16 of timer 2 underflow, 1/16 of timer 3 underflow

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Maximum transfer rate: 375 kbps

■ Features (continued)

- Regulator

  Incorporates regulator, and use of 5 V power supply is possible

- Power Supply Detection

  Detection level 3.7 V to 4.4 V

  When power supply voltage is under detection level, reset is generated.

- Port / pins

  (MN103SFK0K)

I/O ports	84 pins
Motor control output	12 pins
External interrupt	16 pins
A/D input	20 pins
Special pins	16 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Test pin	3 pins
Power pin	10 pins

  (MN103SFK1K)

I/O ports	64 pins
Motor control output	12 pins
External interrupt	12 pins
A/D input	16 pins
Special pins	16 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Test pin	3 pins
Power pin	10 pins

- Package

  (MN103SFK0K)

  QFP100-P-1818B (18 mm square, 0.65 mm pitch)

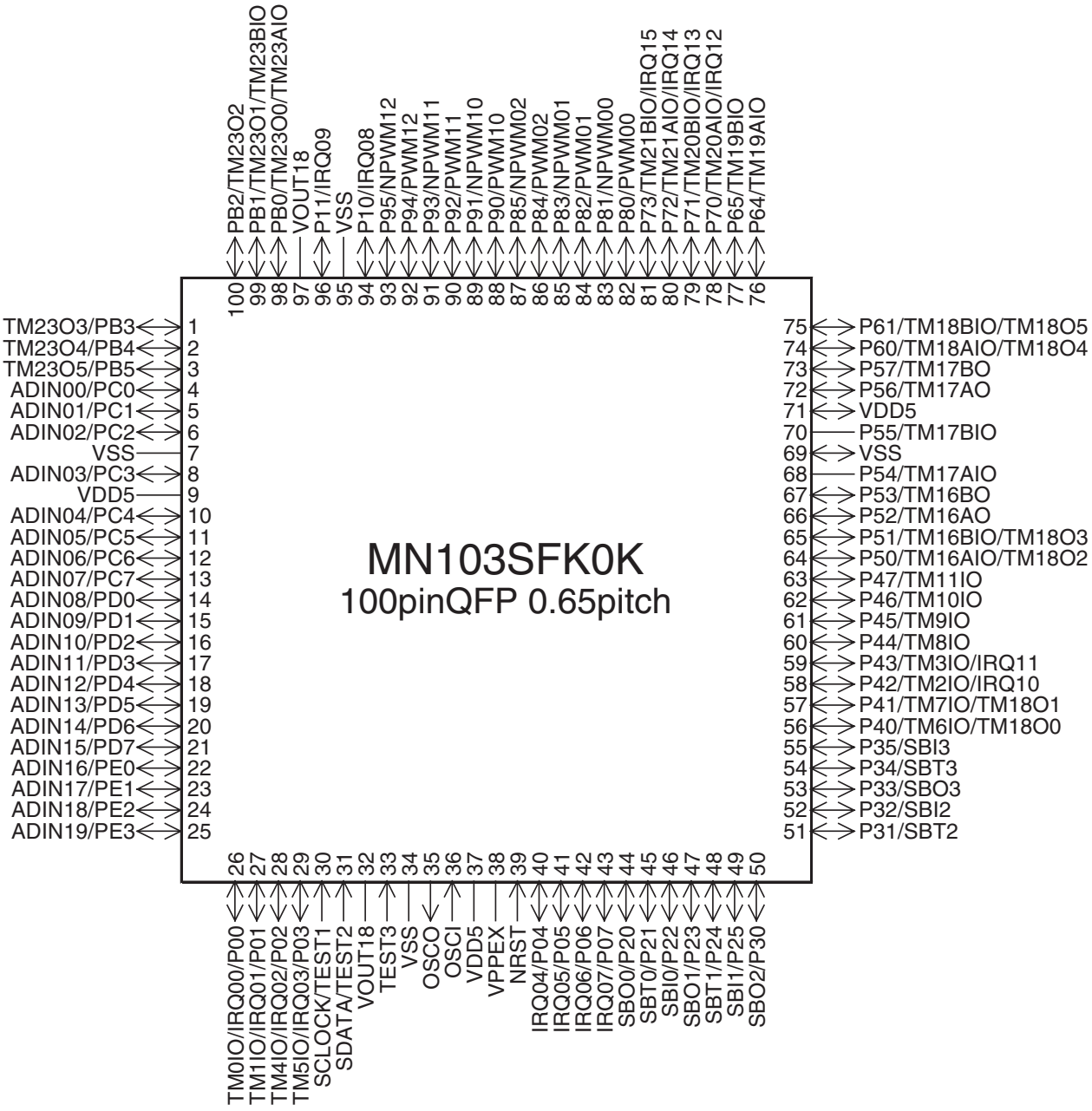
  (MN103SFK1K)

  LQFP080-P-1414A (14 mm square, 0.65 mm pitch)

  TQFP080-P-1212D (12 mm square, 0.50 mm pitch)

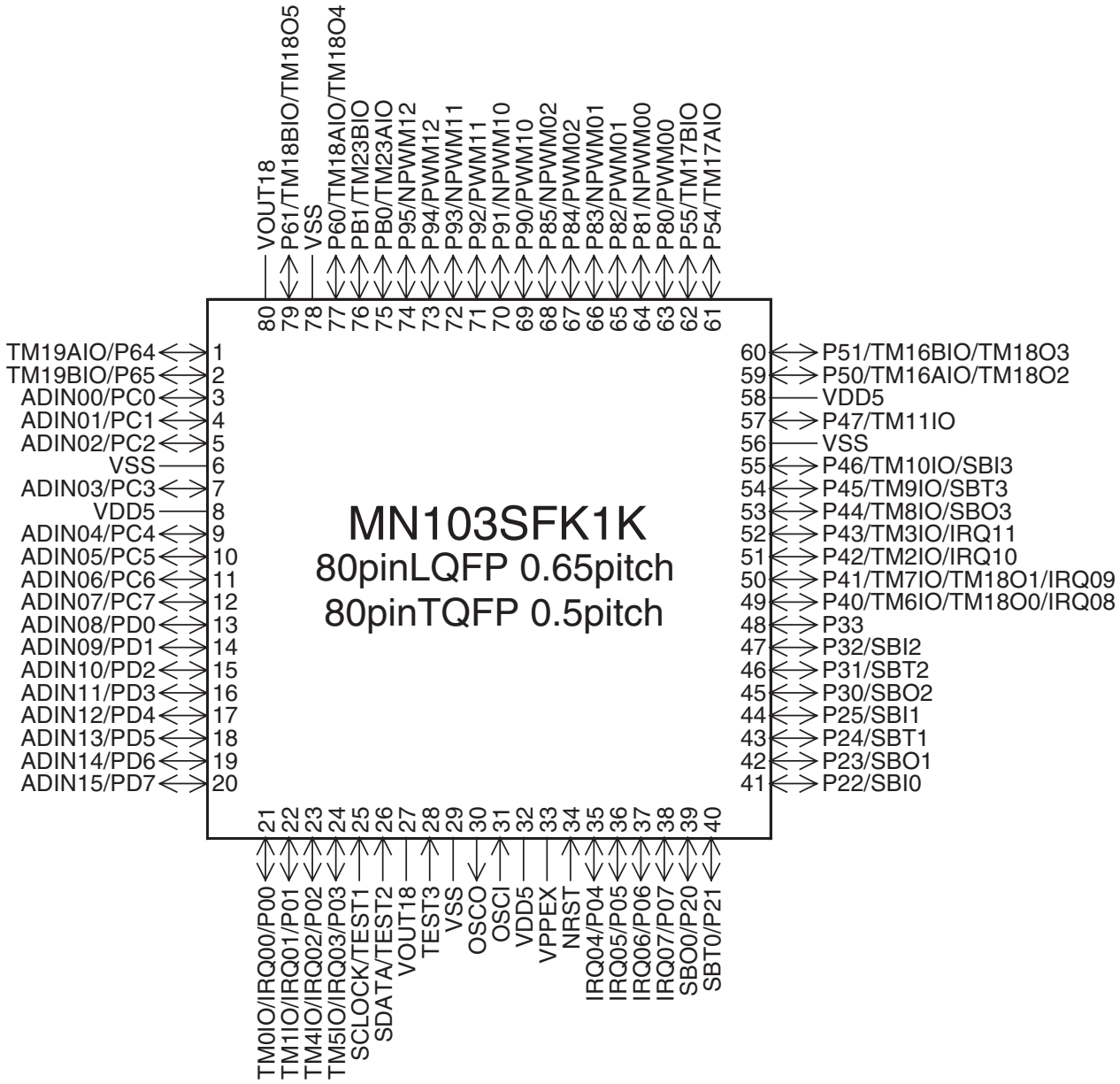
■ Pin Description (continued)

• MN103SFK0K (QFP100-P-1818B)



■ Pin Description (continued)

• MN103SFK1K (LQFP080-P-1414A, TQFP080-P-1212D)



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