



A 22 V, 50 mΩ, 3 A Reverse Blocking Integrated Power Switch with VIN Lockout Select and MOSFET Current Monitor Output

General Description

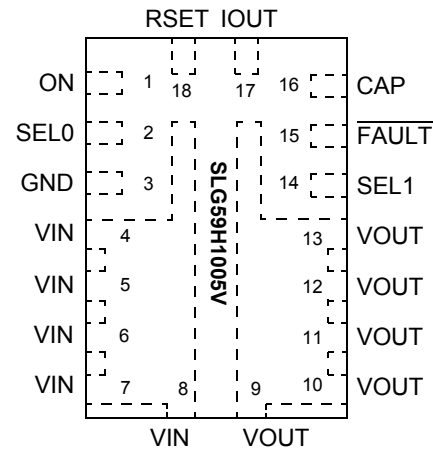
The SLG59H1005V is a high-performance, self-powered 50 mΩ NMOS power switch with back-to-back reverse-current blocking designed for all 4.5 to 22 V power rails up to 3A. Using a proprietary MOSFET design, the SLG59H1005V achieves a stable 50 mΩ $R_{DS(ON)}$ across a wide input/supply voltage range. Using Silego's proprietary CuFET™ technology, the SLG59H1005V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40°C to 85°C range, the SLG59H1005V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

Features

- Wide Operating Supply Voltage: 4.5 V to 22 V
- Maximum Continuous Switch Current: 3 A
- Back-to-Back FET Reverse Current Blocking, when OFF
- Internal nFET Power Limiting
- High-performance MOSFET Switch
 - Low $R_{DS(ON)}$: 50 mΩ at $V_{IN} = 22 V$
 - Low $\Delta R_{DS(ON)}/\Delta V_{IN}$: <0.05 mΩ/V
 - Low $\Delta R_{DS(ON)}/\Delta T$: <0.06 mΩ/°C
- 4-Level, Pin-programmable V_{IN} Overvoltage Lockout
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
 - Resistor-adjustable Active Current Limit
 - Internal Short-circuit Current limit
- Open Drain \overline{FAULT} Signaling
- MOSFET Current Analog Output Monitor: 10 $\mu A/A$
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

Pin Configuration

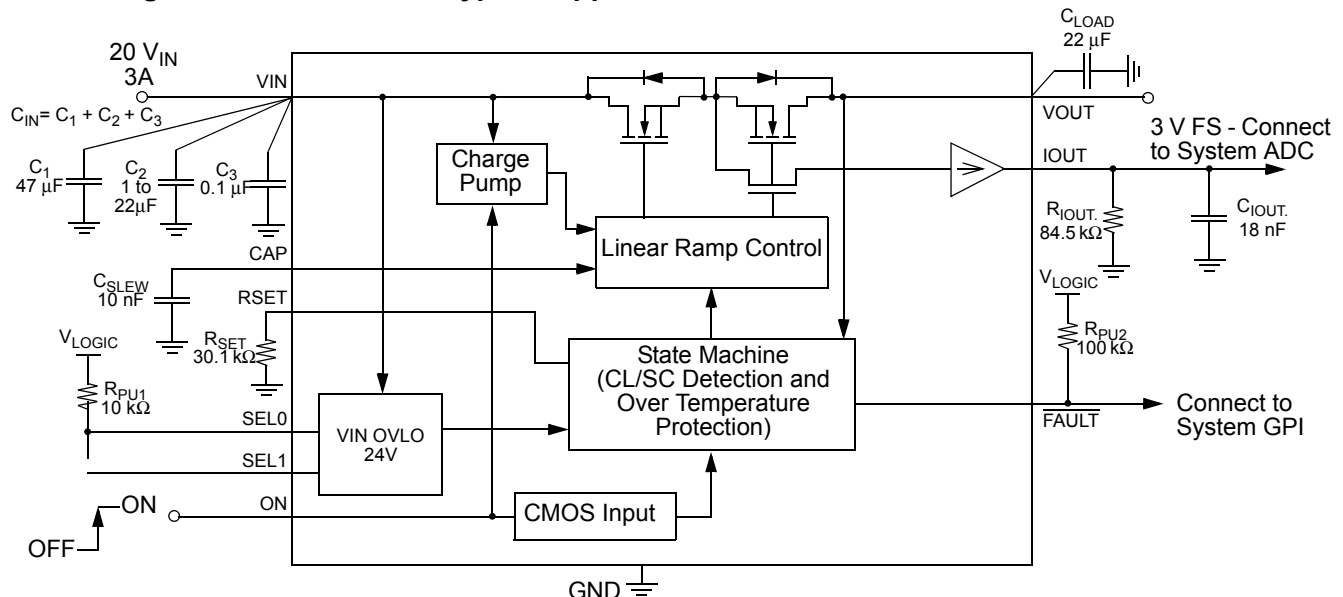


18-pin STQFN
1.6 x 3.0 mm, 0.40mm pitch
(Top View)

Applications

- Power-Rail Switching
- Multifunction Printers
- Large-format Copiers
- Telecommunications Equipment
- High-performance Computing
 - 4.5 V and 22 V Point-of-Load Power Distribution
- Motor Drives

Block Diagram and a 20 V / 3 A Typical Application Circuit





Pin Description

| Pin # | Pin Name | Type | Pin Description |
|-------|---------------------------|--------|---|
| 1 | ON | Input | A low-to-high transition on this pin initiates the operation of the SLG59H1005V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $V_{IL} < 0.3\text{ V}$ and $V_{IH} > 0.85\text{ V}$. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited. |
| 2 | SEL0 | Input | As level-sensitive, CMOS inputs with $V_{IL} < 0.3\text{ V}$ and $V_{IH} > 1.65\text{ V}$, the SEL0 (LSB) and the SEL1 (MSB) pins select one of four V_{IN} overvoltage lockout thresholds. Please see the Applications Section for additional information and the Electrical Characteristics table for the V_{IN} overvoltage thresholds. A logic LOW on either pin is achieved by connecting the pin of interest to GND; a logic HIGH on either pin is achieved by connecting a 10 k Ω external resistor from the pin in question to the system's local logic supply. |
| 3 | GND | GND | Pin 3 is the main ground connection for the SLG59H1005V's internal charge pump, its gate drive and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane. |
| 4-8 | VIN | MOSFET | VIN supplies the power for the operation of the SLG59H1005V, its internal control circuitry, and the drain terminal of the back-to-back, reverse-blocking nFET power switch. With 5 pins fused together at VIN, connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher. |
| 9-13 | VOUT | MOSFET | Drain terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 22 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher. |
| 14 | SEL1 | Input | Please see SEL0 Pin Description above |
| 15 | $\overline{\text{FAULT}}$ | Output | An open drain output, $\overline{\text{FAULT}}$ is asserted within $T_{\text{FAULT_LOW}}$ when a V_{IN} overvoltage, a current-limit, or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within $T_{\text{FAULT_HIGH}}$ when the fault condition is removed. Connect an 100 k Ω external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply. |
| 16 | CAP | Output | A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1005V. For best performance, the range for C_{SLEW} values are $10\text{ nF} \leq C_{\text{SLEW}} \leq 20\text{ nF}$ – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select C_{SLEW} based on V_{OUT} slew rate and loading conditions. |
| 17 | IOUT | Output | IOUT is the SLG59H1005V's power MOSFET load current monitor output. As an analog output current, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I_{OUT} transfer characteristic is typically 10 $\mu\text{A/A}$ with a voltage compliance range of $0.5\text{ V} \leq V_{\text{IOUT}} \leq 4\text{ V}$. Optimal I_{OUT} linearity is exhibited for $0.5\text{ A} \leq I_{\text{DS}} \leq 3\text{ A}$. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor. |
| 18 | RSET | Input | A 1%-tolerance, metal-film resistor between 30 k Ω and 95 k Ω sets the SLG59H1005V's active current limit. A 95 k Ω resistor sets the SLG59H1005V's active current limit to 1 A and a 30 k Ω resistor sets the active current limit to 3 A. |

Ordering Information

| Part Number | Type | Production Flow |
|---------------|------------------------------|-----------------------------|
| SLG59H1005V | STQFN 18L FC | Industrial, -40 °C to 85 °C |
| SLG59H1005VTR | STQFN 18L FC (Tape and Reel) | Industrial, -40 °C to 85 °C |



Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|--|---|------|------|-----------------|------|
| V _{IN} to GND | Power Switch Input Voltage to GND | Continuous | -0.3 | -- | 30 | V |
| | | Maximum pulsed V _{IN} , pulse width <0.1s | -- | -- | 32 | V |
| V _{OUT} to GND | Power Switch Output Voltage to GND | | -0.3 | -- | V _{IN} | V |
| ON, SEL[1,0], CAP, RSET, IOU \bar{T} , and FAULT to GND | ON, SEL[1,0], CAP, RSET, IOU \bar{T} , and FAULT Pin Voltages to GND | | -0.3 | -- | 7 | V |
| T _S | Storage Temperature | | -65 | -- | 150 | °C |
| ESD _{HBM} | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| ESD _{CDM} | ESD Protection | Charged Device Model | 500 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| θ_{JA} | Thermal Resistance | 1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in ² , 1 oz. copper pad of FR-4 material | -- | 40 | -- | °C/W |
| T _{J,MAX} | Maximum Junction Temperature | | -- | 150 | -- | °C |
| MOSFET IDS _{CONT} | Continuous Current from VIN to VOUT | T _J < 150°C | -- | -- | 4 | A |
| MOSFET IDS _{PEAK} | Peak Current from VIN to VOUT | Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle | -- | -- | 5 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

4.5 V ≤ V_{IN} ≤ 22 V; C_{IN} = 47 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------|--|---|------|------|------|------|
| V _{IN} | Operating Input Voltage | | 4.5 | -- | 22 | V |
| V _{IN(OVLO)} | V _{IN} Overvoltage Lockout Threshold | V _{IN} ↑; SEL[1,0] = [0,0] | 5.6 | 6 | 6.3 | V |
| | | V _{IN} ↑; SEL[1,0] = [0,1] | 10.2 | 10.8 | 11.4 | V |
| | | V _{IN} ↑; SEL[1,0] = [1,0] | 13.5 | 14.4 | 15.2 | V |
| | | V _{IN} ↑; SEL[1,0] = [1,1] | 22.6 | 24 | 25.2 | V |
| V _{IN(OVLOHYST)} | V _{IN} Overvoltage Lockout Hysteresis | | -- | 2 | -- | % |
| V _{IN(UVLO)} | V _{IN} Undervoltage Lockout Threshold | V _{IN} ↓ | 3 | 3.2 | 3.4 | V |
| I _Q | Quiescent Supply Current | ON = HIGH; I _{DS} = 0 A | -- | 0.5 | 0.6 | mA |
| I _{SHDN} | OFF Mode Supply Current | ON = LOW; I _{DS} = 0 A | -- | 1 | 3 | μA |
| RDS _{ON} | ON Resistance | T _A = 25°C; I _{DS} = 0.1 A | -- | 50 | 52 | mΩ |
| | | T _A = 85°C; I _{DS} = 0.1 A | -- | 65 | 68 | mΩ |



Electrical Characteristics (continued)

4.5 V ≤ V_{IN} ≤ 22 V; C_{IN} = 47 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------------|---|--|-----------------------------------|------|------|------|
| MOSFET I _{DS} | Current from VIN to VOUT | Continuous | -- | -- | 3 | A |
| I _{REVERSE} | MOSFET Reverse-Leakage Current | V _{IN} = 0 V; V _{OUT} = 22 V; ON = 0 V | -- | -- | 3 | μA |
| I _{LIMIT} | Active Current Limit, I _{ACL} | V _{OUT} > 0.5 V; R _{SET} = 30.1 kΩ | 3 | 3.2 | 3.4 | A |
| | Short-circuit Current Limit, I _{SCL} | V _{OUT} < 0.5 V | -- | 0.5 | -- | A |
| T _{ACL} | Active Current Limit Response Time | R _{SET} = 51.6 kΩ | -- | 120 | -- | μs |
| I _{OUT} | MOSFET Current Analog Monitor Output | I _{LOAD} = 1 A | 9.3 | 10 | 10.7 | μA |
| | | I _{LOAD} = 3 A | 28.5 | 30 | 31.5 | μA |
| T _{IOUT} | I _{OUT} Response Time to Change in Main MOSFET Current | C _{IOUT} = 180 pF; Step load 0 to 2.4 A; 0% to 90% I _{OUT} | -- | 45 | -- | μs |
| C _{LOAD} | Output Load Capacitance | C _{LOAD} connected from VOUT to GND | -- | 22 | -- | μF |
| T _{ON_Delay} | ON Delay Time | 50% ON to 10% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF | -- | 0.3 | 0.5 | ms |
| | | 50% ON to 10% V _{OUT} ↑; V _{IN} = 22 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF | -- | 0.7 | 1.2 | ms |
| T _{Total_ON} | Total Turn-on Time | 50% ON to 90% V _{OUT} ↑ | Set by External C _{SLEW} | | | ms |
| | | 50% ON to 90% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF | -- | 1.5 | 2.1 | ms |
| | | 50% ON to 90% V _{OUT} ↑; V _{IN} = 22 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF | -- | 6.5 | 8 | ms |
| V _{OUT(SR)} | V _{OUT} Slew rate | 50% ON to 90% V _{OUT} ↑ | Set by External C _{SLEW} | | | V/ms |
| | | 10% to 90% V _{OUT} ↑; V _{IN} = 4.5 to 22 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF | 2.7 | 3.2 | 3.9 | V/ms |
| T _{OFF_Delay} | OFF Delay Time | 50% ON to V _{OUT} ↓; R _{LOAD} = 100 Ω, No C _{LOAD} | -- | 15 | -- | μs |
| T _{FALL} | V _{OUT} Fall Time | 90% V _{OUT} to 10% V _{OUT} ↓; ON = HIGH-to-LOW; V _{IN} = 4.5 V to 22 V; R _{LOAD} = 100 Ω, No C _{LOAD} | 10.4 | 12.7 | 14.3 | μs |
| T _{FAULT_LOW} | FAULT Assertion Time | Abnormal Step Load Current event to FAULT ↓; I _{ACL} = 1 A; V _{IN} = 22 V; R _{SET} = 95 kΩ; switch in 20 Ω load | -- | 80 | -- | μs |
| T _{FAULT_HIGH} | FAULT De-assertion Time | Delay to FAULT ↑ after fault condition is removed; I _{ACL} = 1 A; V _{IN} = 22 V; R _{SET} = 95 kΩ; switch out 20 Ω load | -- | 180 | -- | μs |
| FAULT _{VOL} | FAULT Output Low Voltage | I _{FAULT} = 1 mA | -- | 0.2 | -- | V |
| ON_V _{IH} | ON Pin Input High Voltage | | 0.9 | -- | 5 | V |
| ON_V _{IL} | ON Pin Input Low Voltage | | -0.3 | 0 | 0.3 | V |
| SEL[1,0] _{V_{IH}} | SEL[1,0] pins Input High Voltage | | 1.65 | -- | 4.5 | V |



Electrical Characteristics (continued)

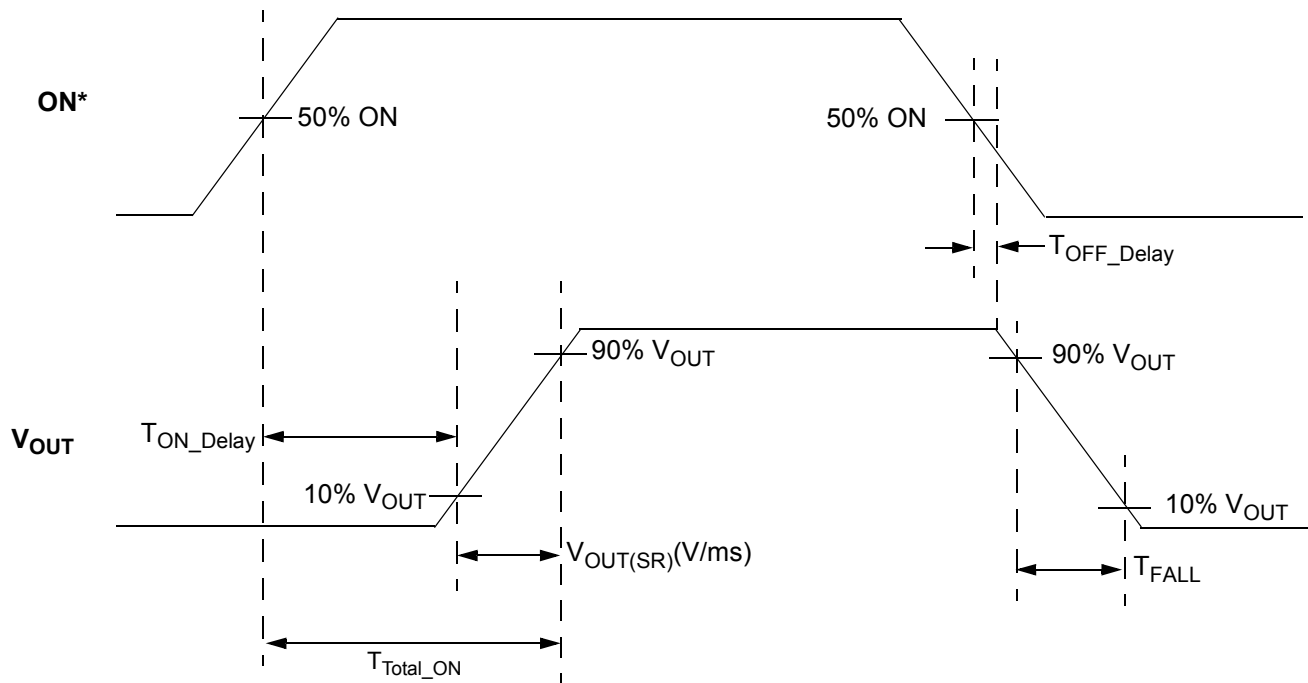
4.5 V ≤ V_{IN} ≤ 22 V; C_{IN} = 47 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|---------------------------------------|--------------------------|------|------|------|------|
| SEL[1,0]_V _{IL} | SEL[1,0] pins Input Low Voltage | | -0.3 | -- | 0.3 | V |
| I _{ON(Leakage)} | ON Pin Leakage Current | 1V ≤ ON ≤ 5V or ON = GND | -- | -- | 1 | μA |
| THERM _{ON} | Thermal Protection Shutdown Threshold | | -- | 125 | -- | °C |
| THERM _{OFF} | Thermal Protection Restart Threshold | | -- | 100 | -- | °C |

Notes:

1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement Timing Details

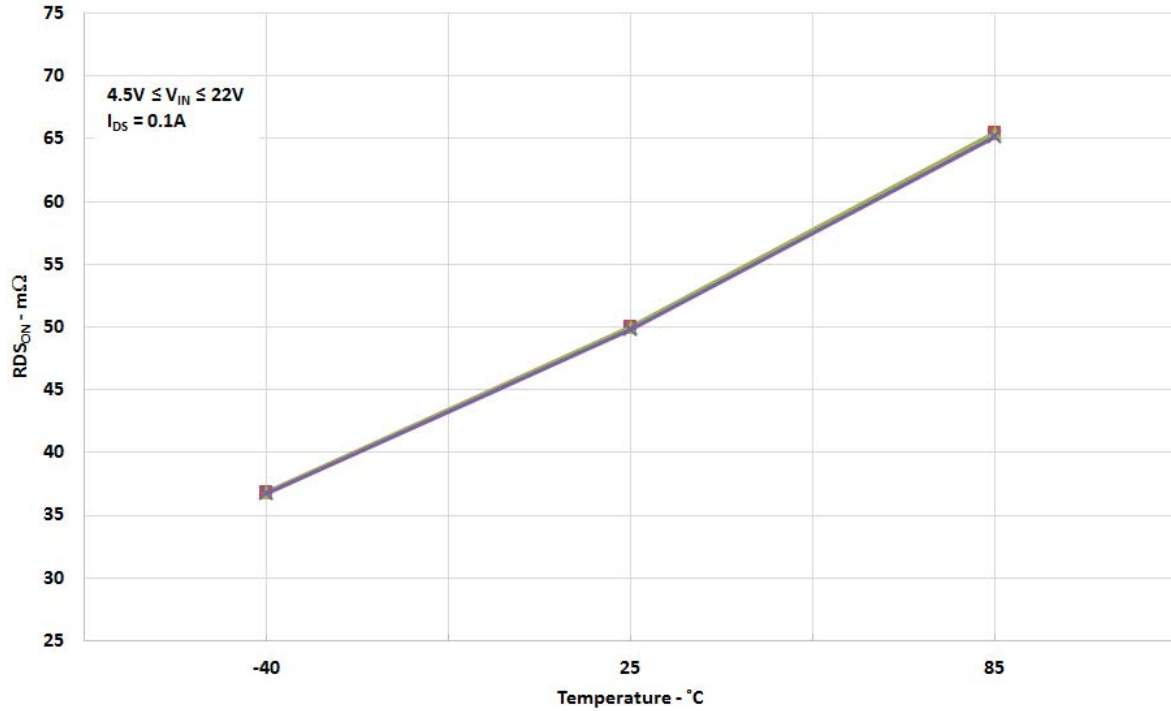


* Rise and Fall times of the ON signal are 100 ns

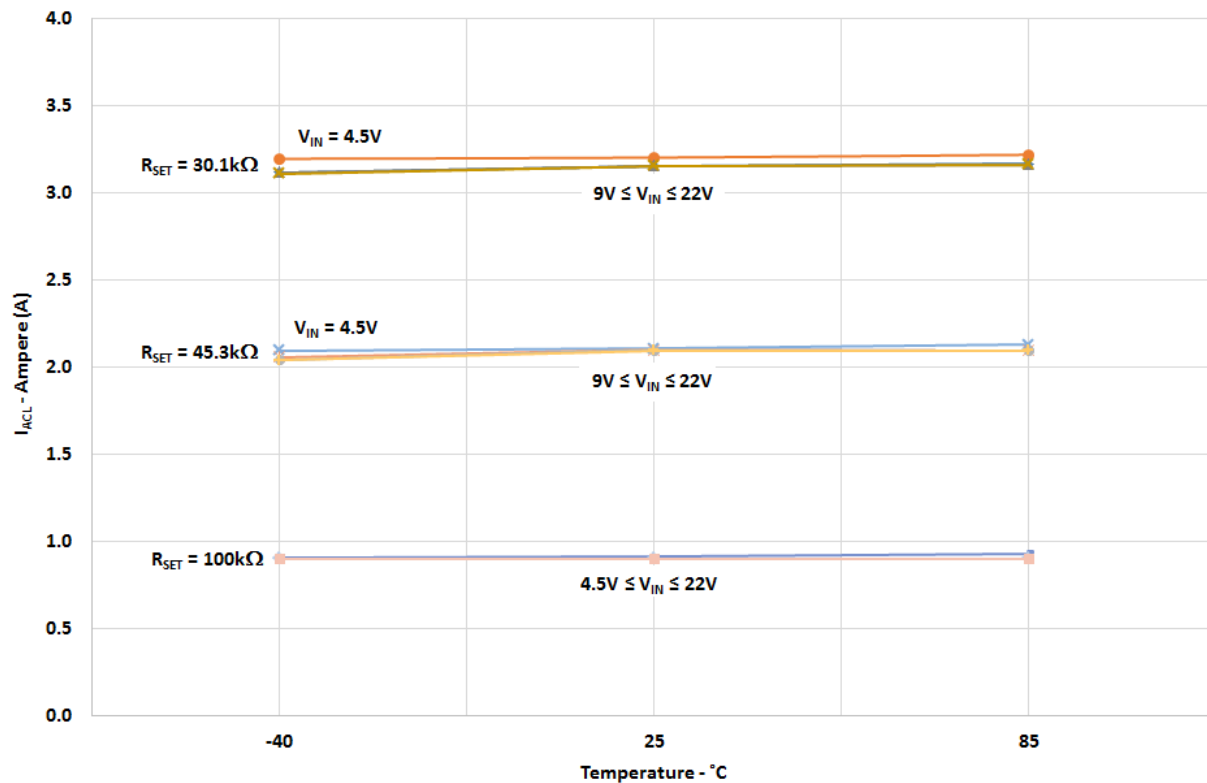


Typical Performance Characteristics

$R_{DS(ON)}$ vs. Temperature and V_{IN}

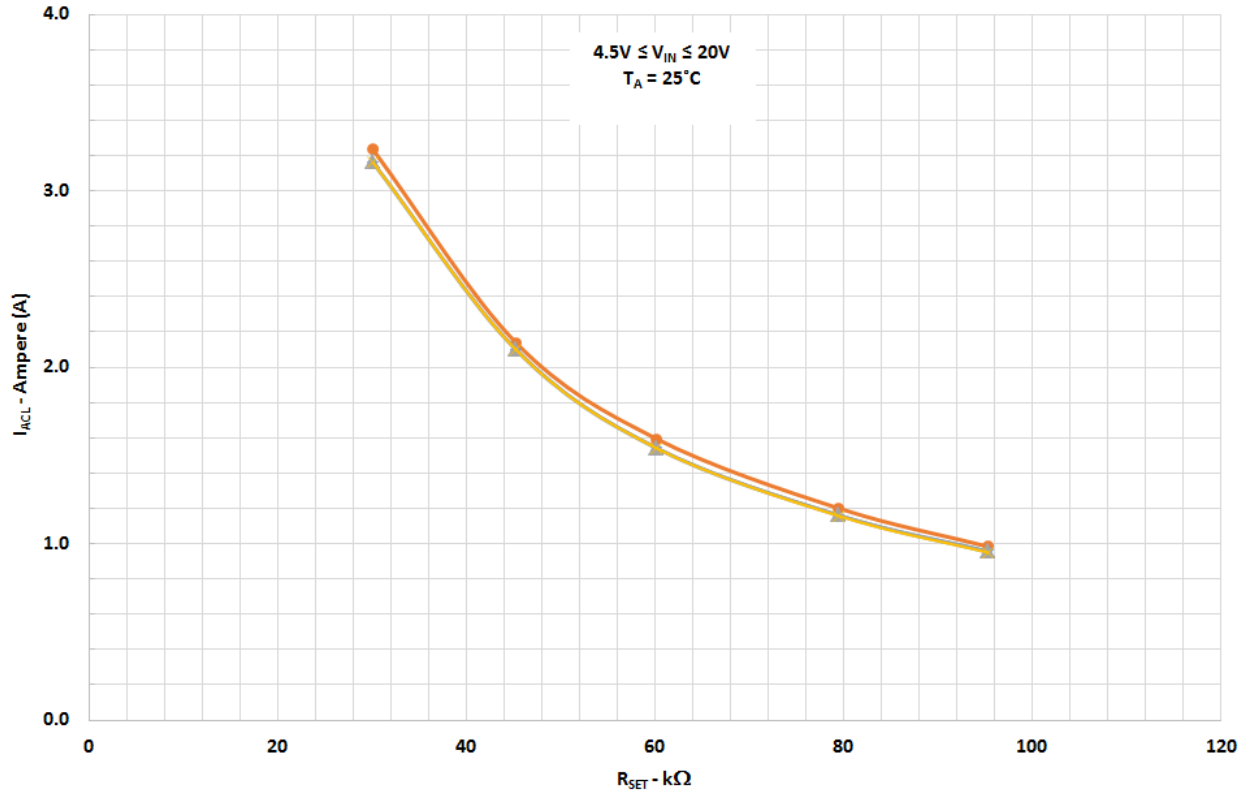


I_{ACL} vs. Temperature and R_{SET}

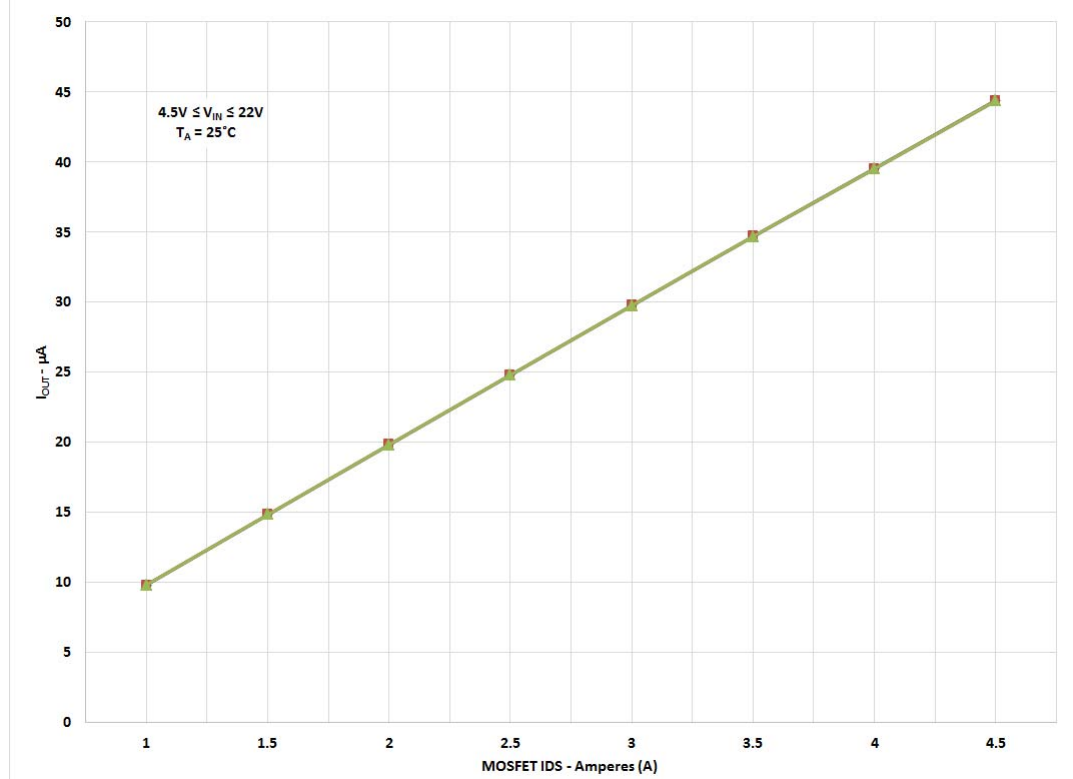




I_{ACL} vs. R_{SET}

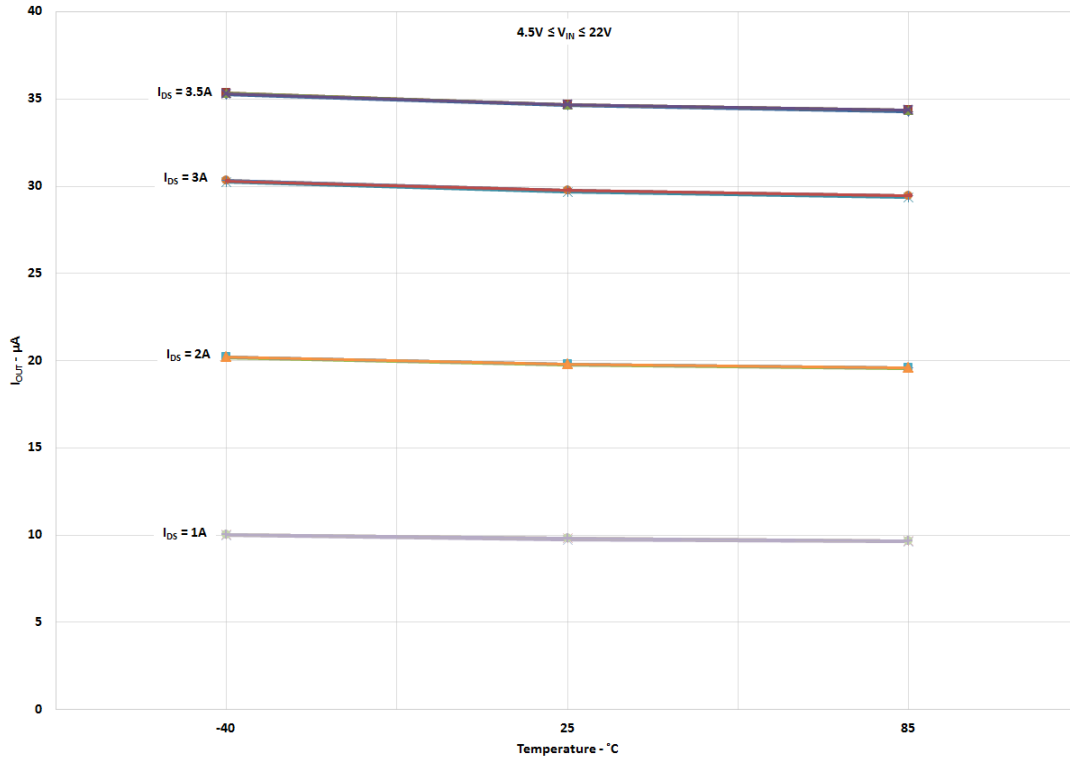


I_{OUT} vs. MOSFET I_{DS} and V_{IN}

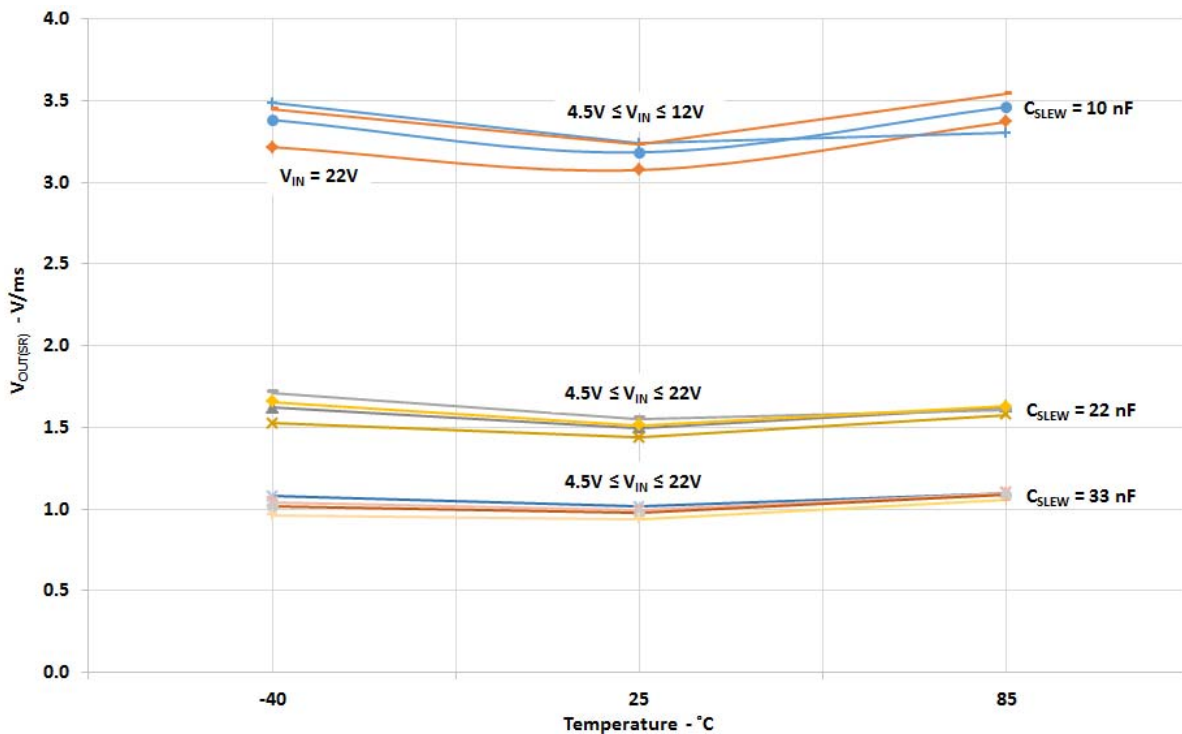




I_{OUT} vs. Temperature and MOSFET IDS

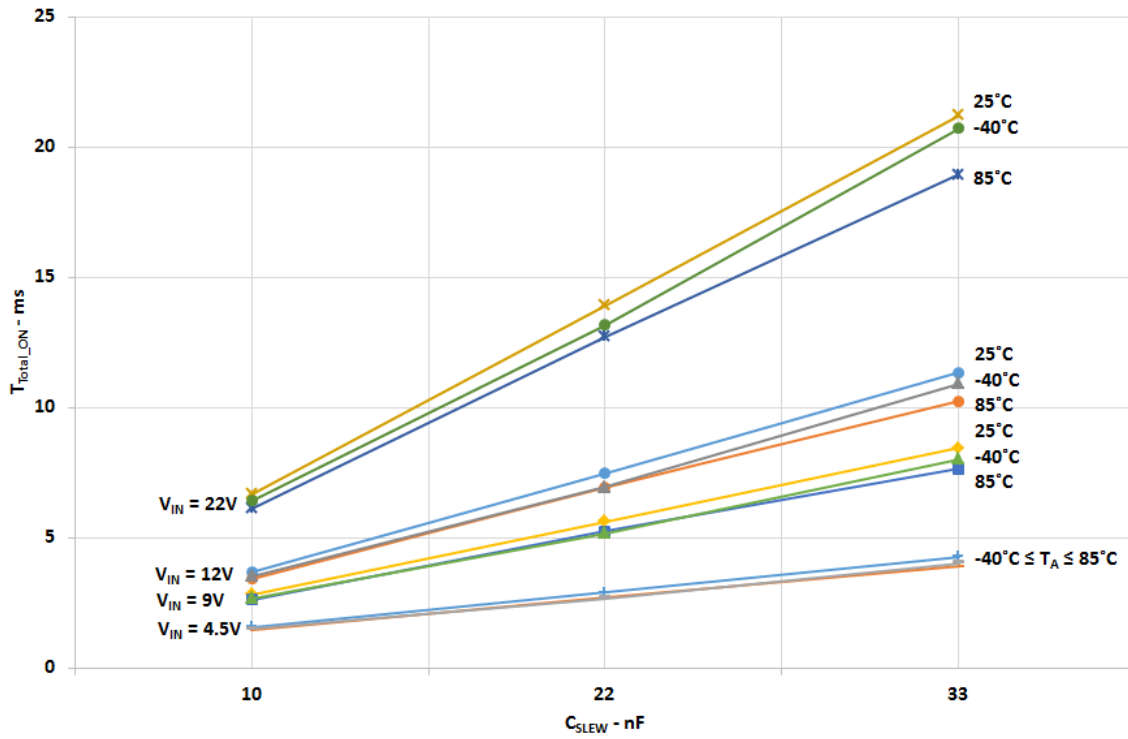


V_{OUT} Slew Rate vs. Temperature, V_{IN} , and C_{SLEW}



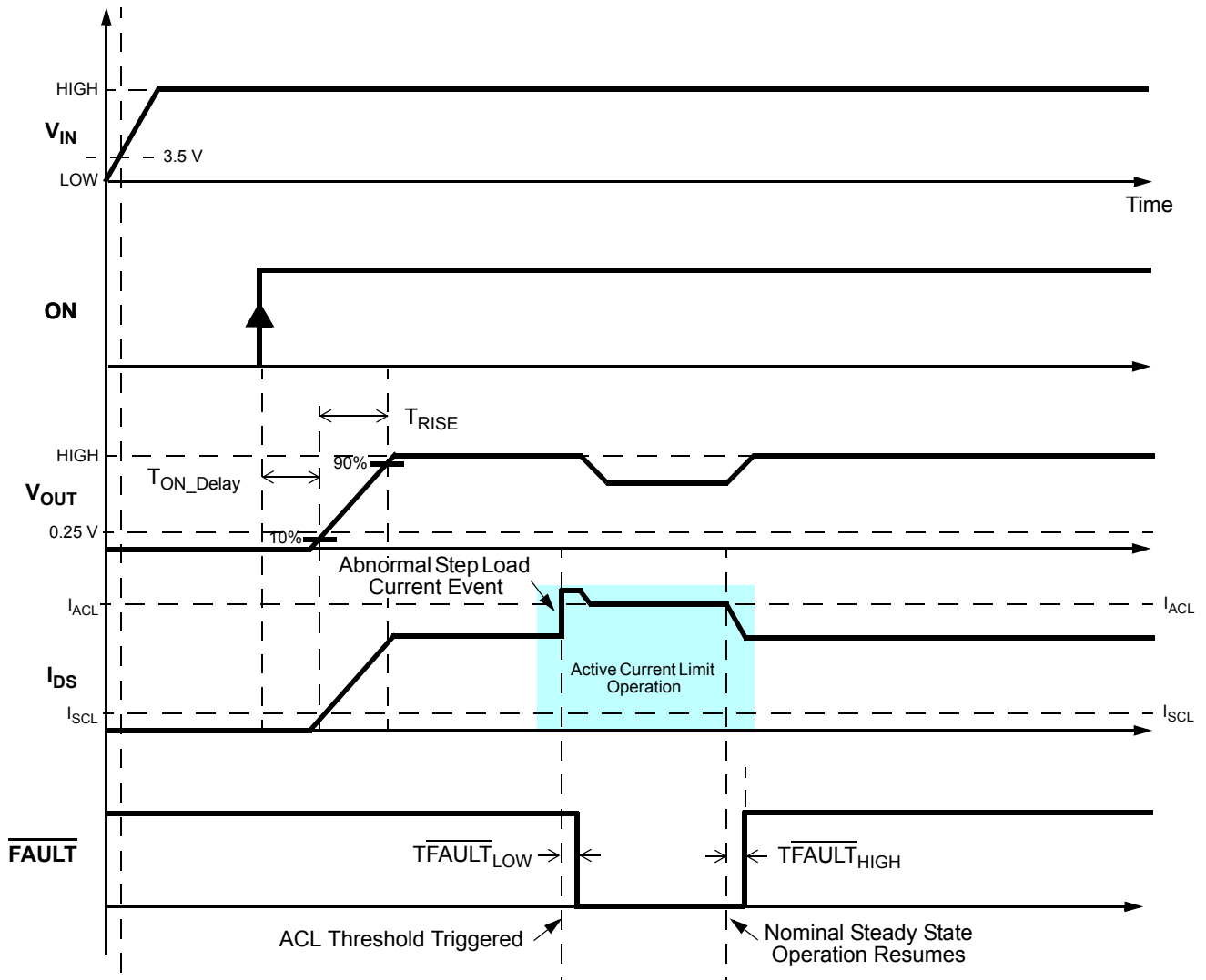


T_{Total_ON} vs. C_{SLEW} , V_{IN} , and Temperature



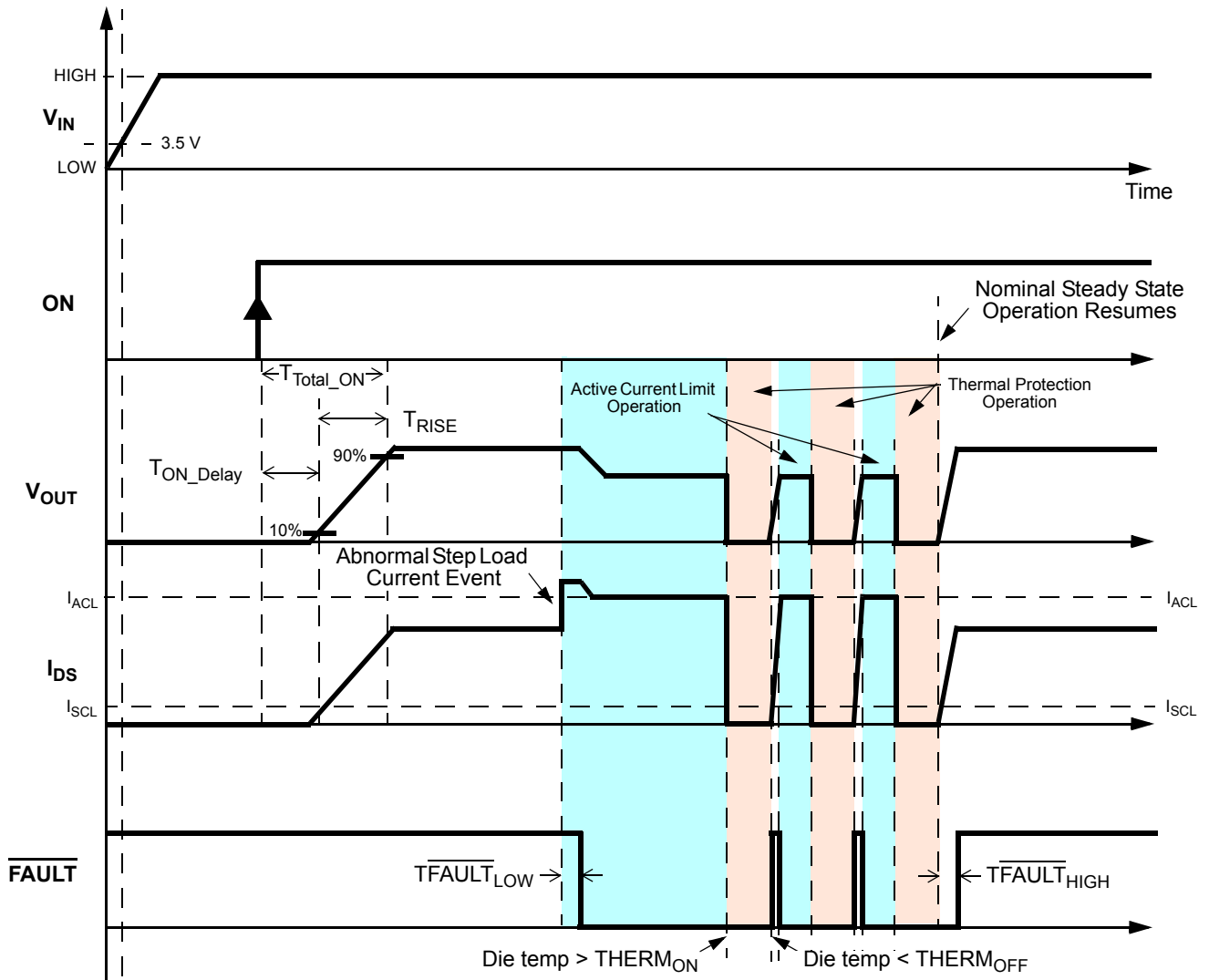


Timing Diagram - Basic Operation including Active Current Limit Protection



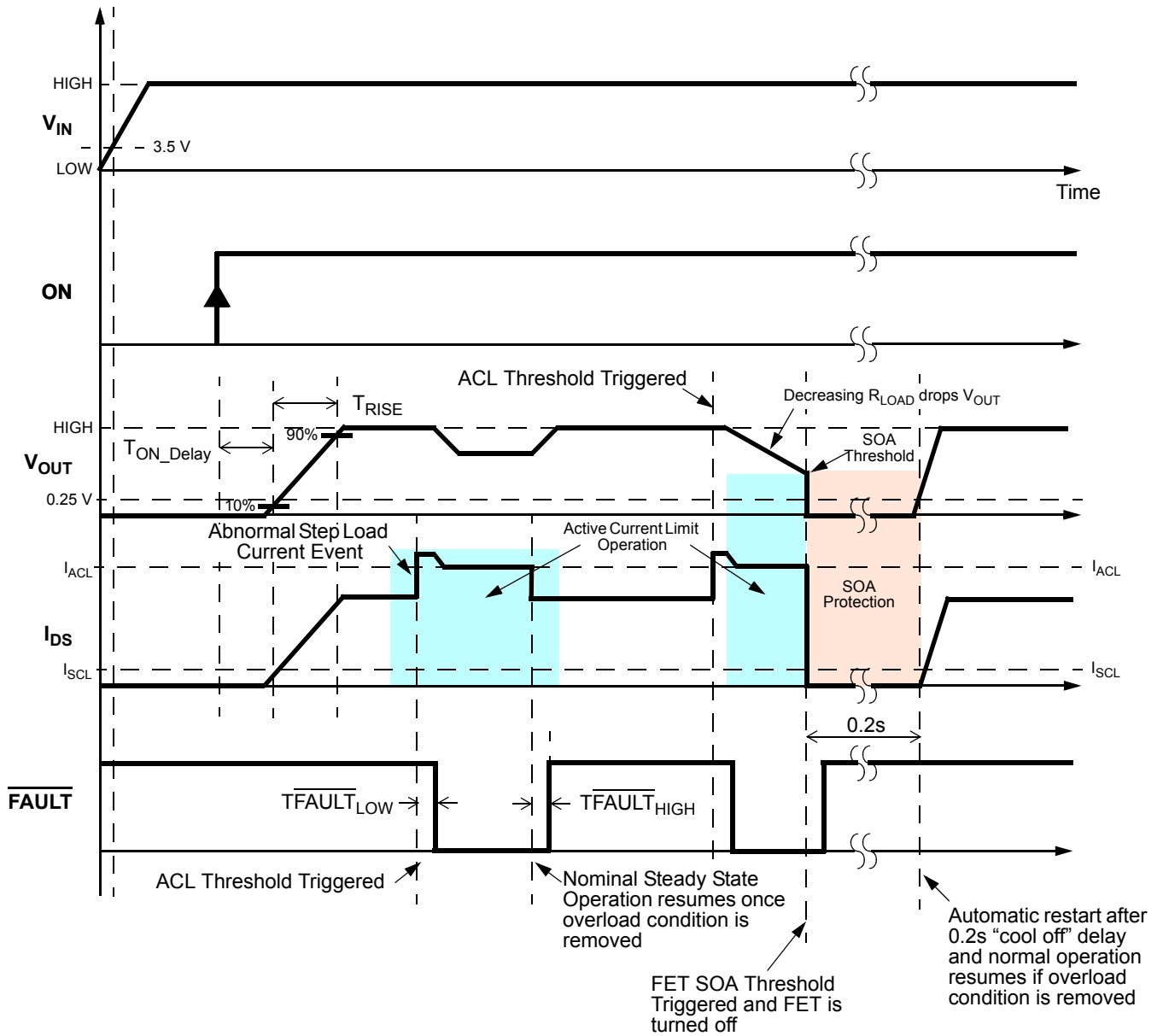


Timing Diagram - Active Current Limit & Thermal Protection Operation





Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection





Applications Information

HFET1 Safe Operating Area Explained

Silego's HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 5W threshold longer than 2.5 ms. HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One possible way to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external R_{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's $R_{DS_{ON}}$ increased as well. Since the FET's $R_{DS_{ON}}$ is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 5 W for longer than 2.5 ms, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms.

Safe Start-up Condition

SLG59H1005V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the V_{OUT} pin with a capacitor and a resistor may result in non-monotonic V_{OUT} ramping. In general, under light loading on V_{OUT} , V_{OUT} ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 5 \mu A \times \frac{20}{3}$$

where

T_{RISE} = Total rise time from 10% V_{OUT} to 90% V_{OUT}

V_{IN} = Input Voltage

C_{SLEW} = Capacitor value for CAP pin

When capacitor and resistor loading on V_{OUT} during start up, the following tables will ensure V_{OUT} ramping is monotonic without triggering internal protection:

| Safe Start-up Loading for $V_{IN} = 22 V$ (Monotonic Ramp) | | | |
|--|------------------------------|-----------------|----------------|
| Slew Rate (V/ms) | C_{SLEW} (nF) ³ | C_{LOAD} (μF) | R_{LOAD} (Ω) |
| 0.5 | 66.7 | 500 | 80 |
| 1.0 | 33.3 | 250 | 80 |
| 1.5 | 22.2 | 160 | 80 |
| 2.0 | 16.7 | 120 | 80 |
| 2.5 | 13.3 | 100 | 80 |



| Safe Start-up Loading for $V_{IN} = 12\text{ V}$ (Monotonic Ramp) | | | |
|---|------------------------------|-----------------------|-------------------------|
| Slew Rate (V/ms) | C_{SLEW} (nF) ³ | C_{LOAD} (μ F) | R_{LOAD} (Ω) |
| 1 | 33.3 | 500 | 20 |
| 2 | 16.7 | 250 | 20 |
| 3 | 11.1 | 160 | 20 |
| 4 | 8.3 | 120 | 20 |
| 5 | 6.7 | 100 | 20 |

Note 3: Select the closest-value tolerance capacitor.

Setting the SLG59H1005V's Active Current Limit

| R_{SET} (k Ω) | Active Current Limit (A) ⁴ |
|-------------------------|---------------------------------------|
| 95 | 1 |
| 45 | 2 |
| 30 | 3 |

Note 4: Active Current Limit accuracy is $\pm 15\%$ over voltage range and over temperature range.

Setting the SLG59H1005V's Input Overvoltage Lockout Threshold

As shown in the table below, SEL[1,0] selects the V_{IN} overvoltage threshold at which the SLG59H1005V's internal state machine will turn OFF (open circuit) the power MOSFET if V_{IN} exceeds the selected threshold.

| SEL1 | SEL0 | $V_{IN(OVLO)}$ (Typ) |
|------|------|----------------------|
| 0 | 0 | 6 |
| 0 | 1 | 10.8 |
| 1 | 0 | 14.4 |
| 1 | 1 | 24 |

For example, SEL[1,1] would be the most appropriate setting for applications where the steady-state V_{IN} can extend up to 20V without causing any damage to the SLG59H1005V since the IC is 29-V tolerant.

With an activated SLG59H1005V (ON=HIGH) and at any time V_{IN} crosses the programmed V_{IN} overvoltage threshold, the state machine opens the power switch and asserts the \overline{FAULT} pin within T_{FAULT_LOW} .

In applications with a deactivated or inactive SLG59H1005V ($V_{IN} > V_{IN(OVLO)}$ and ON=LOW) and if the applied V_{IN} is higher than the programmed $V_{IN(OVLO)}$ threshold, the SLG59H1005V's state machine will keep the power switch open circuited if the ON pin is toggled LOW-to-HIGH. In these cases, the \overline{FAULT} pin will also be asserted within T_{FAULT_LOW} and will remain asserted until V_{IN} resumes nominal, steady-state operation.

In all cases, the SLG59H1005V's V_{IN} undervoltage lockout threshold is fixed at $V_{IN(UVLO)}$.



Power Dissipation

The junction temperature of the SLG59H1005V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1005V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees ($^{\circ}C$)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt ($^{\circ}C/W$)

T_A = Ambient temperature, in Celsius degrees ($^{\circ}C$)

In current-limit mode, the SLG59H1005V's power dissipation can be calculated by taking into account the voltage drop across the power switch ($V_{IN}-V_{OUT}$) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN}-V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

V_{IN} = Input Voltage, in Volts (V)

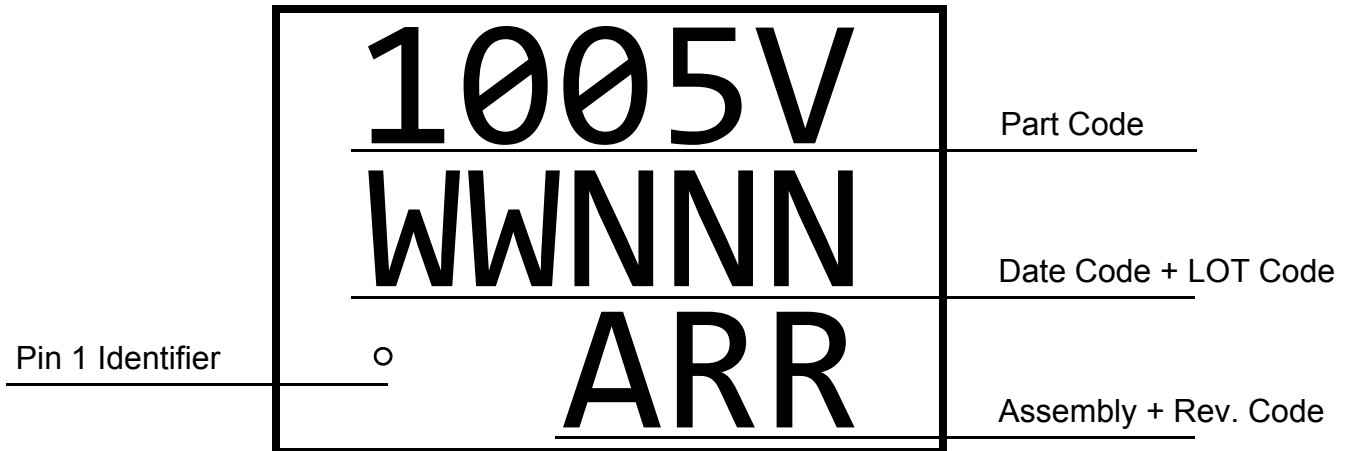
R_{LOAD} = Load Resistance, in Ohms (Ω)

I_{ACL} = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$



Package Top Marking System Definition



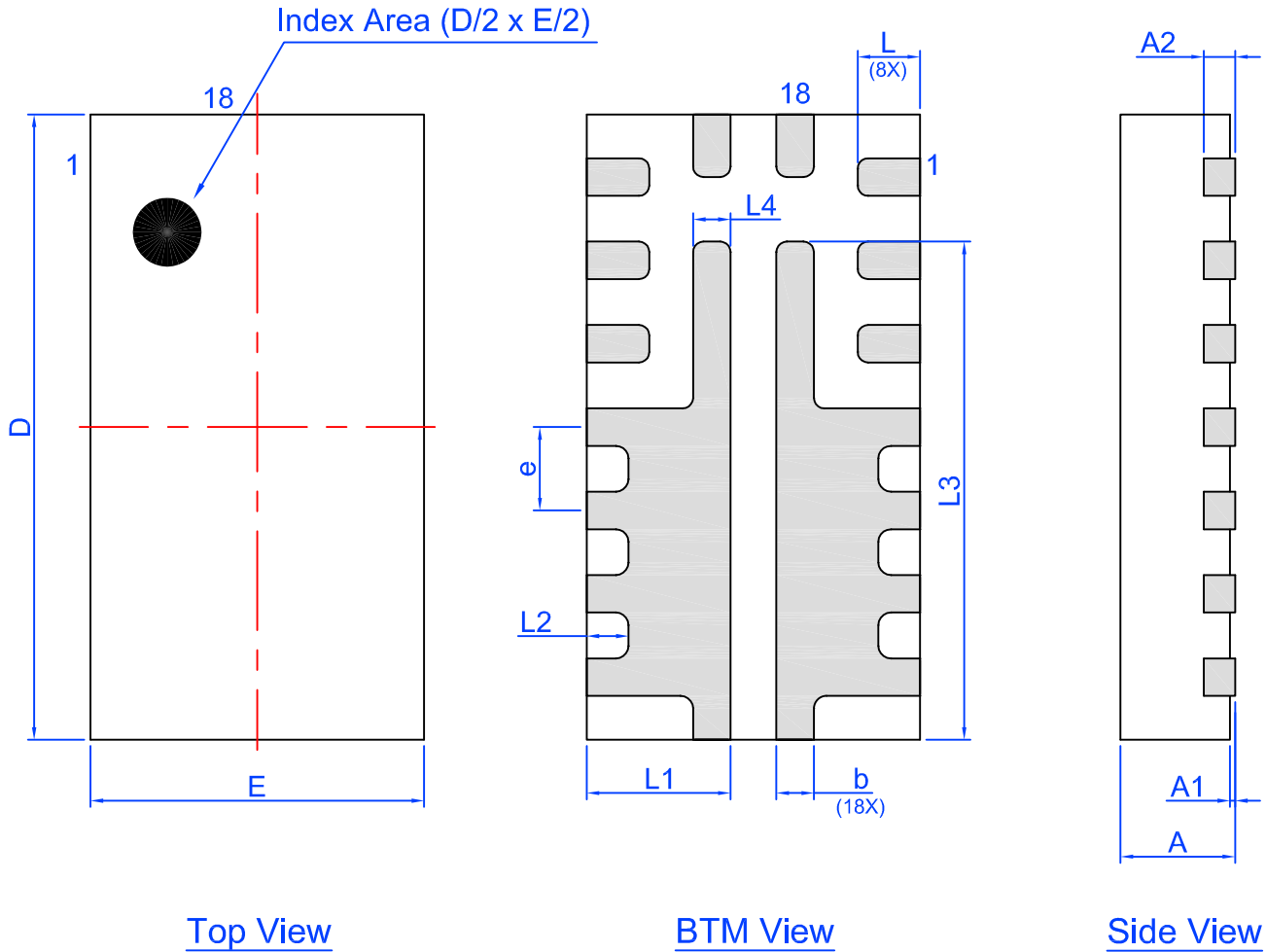
- 1005V - Part ID Field
- WW - Date Code Field¹
- NNN - Lot Traceability Code Field¹
- A - Assembly Site Code Field²
- RR - Part Revision Code Field²

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z



Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE



Unit: mm

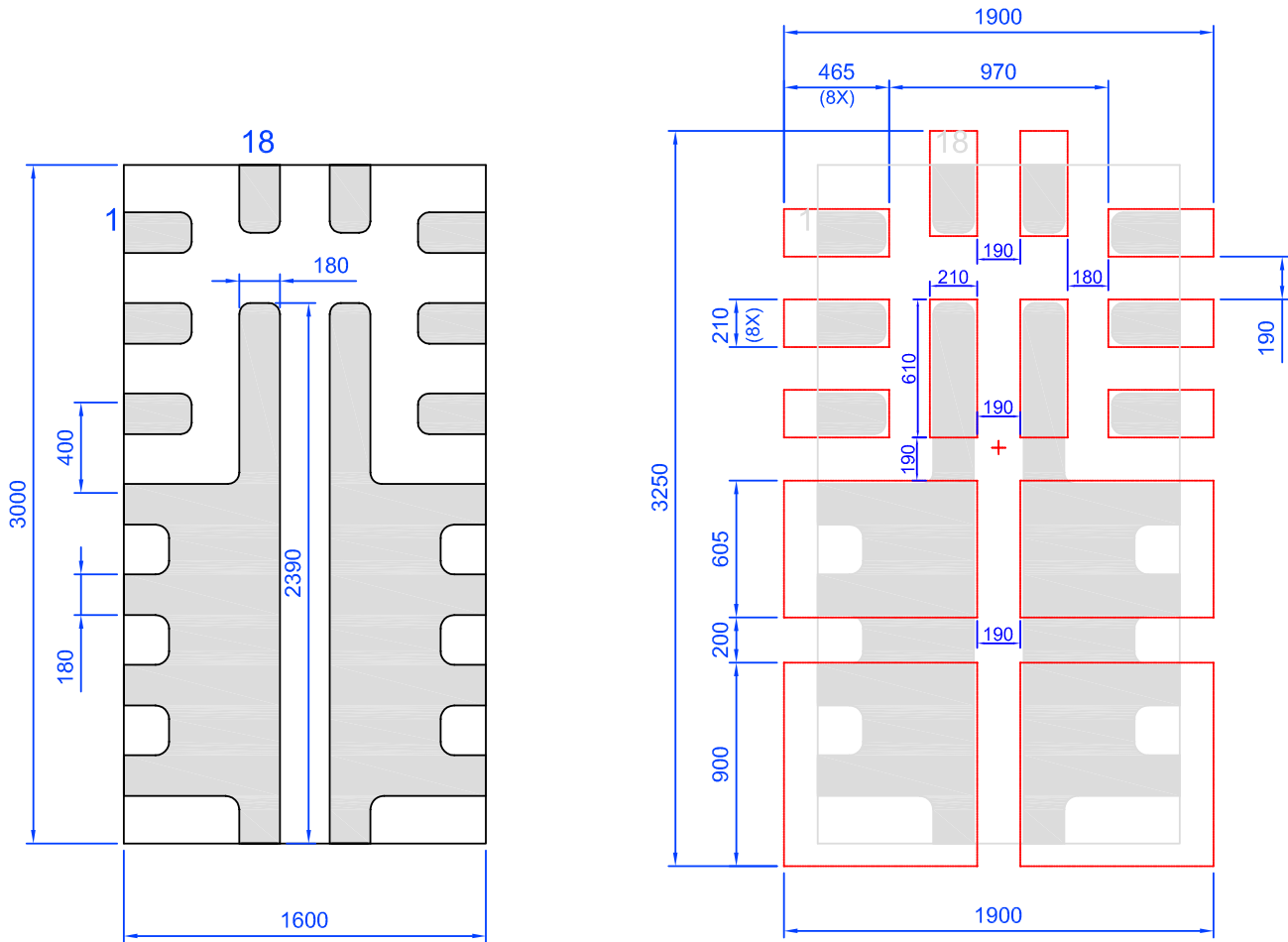
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|------|--------|------|------|------|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.05 | E | 1.55 | 1.60 | 1.65 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.25 | 0.30 | 0.35 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.64 | 0.69 | 0.74 |
| e | 0.40 BSC | | | L2 | 0.15 | 0.20 | 0.25 |
| L3 | 2.34 | 2.39 | 2.44 | L4 | 0.13 | 0.18 | 0.23 |



SLG59H1005V 18-pin STQFN PCB Landing Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



Note: All dimensions shown in micrometers (μm)

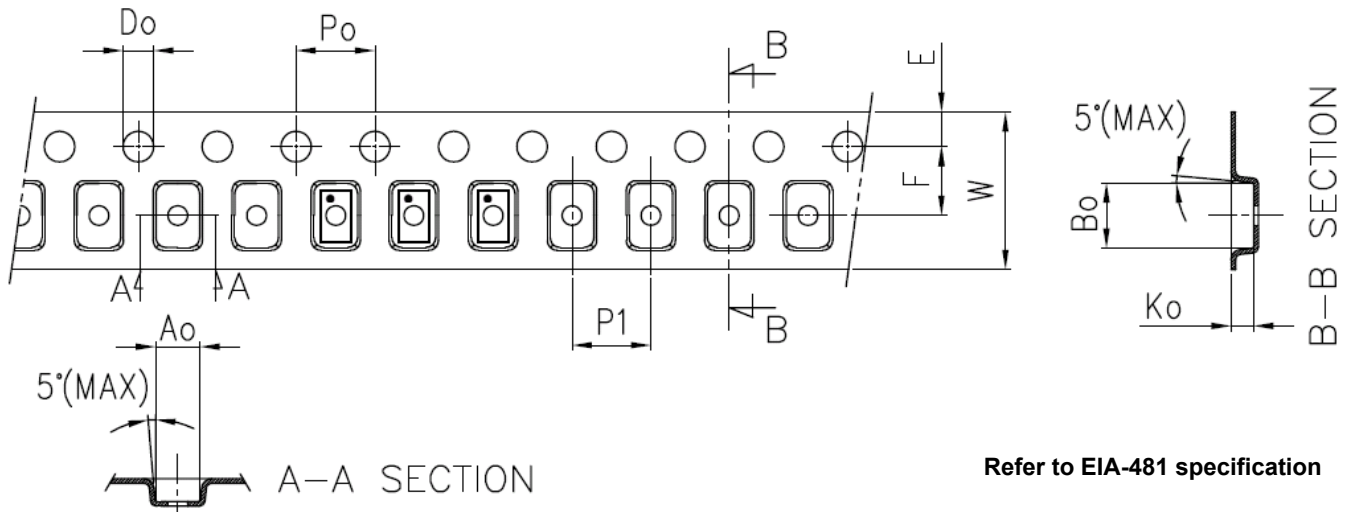


Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|-------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 18L 0.4P FC Green | 18 | 1.6 x 3 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|-------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 18L 0.4P FC Green | 1.78 | 3.18 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal). More information can be found at www.jedec.org.



Revision History

| Date | Version | Change |
|-----------|---------|--|
| 4/4/2017 | 1.02 | Updated Block Diagram Updated Charts Updated SOA operation Timing Diagrams |
| 3/21/2017 | 1.01 | Updated Features |
| 2/24/2017 | 1.00 | Production Release |