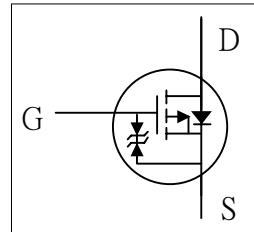




- ▼ 100% R<sub>g</sub> & UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

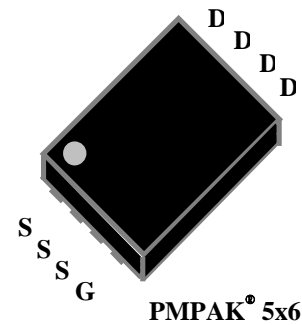


BV <sub>DSS</sub>	-30V
R <sub>DS(ON)</sub>	7mΩ
I <sub>D</sub>	-75A
HBM ESD	2KV

**Description**

AP3P7R0E series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK<sup>®</sup> 5x6 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



**Absolute Maximum Ratings @T<sub>j</sub>=25°C (unless otherwise specified)**

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V	-75	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	-47.8	A
I <sub>D</sub> @T <sub>A</sub> =25°C	Drain Current <sup>3</sup> , V <sub>GS</sub> @ 10V	-22	A
I <sub>D</sub> @T <sub>A</sub> =70°C	Drain Current <sup>3</sup> , V <sub>GS</sub> @ 10V	-17.5	A
I <sub>DM</sub>	Pulsed Drain Current <sup>1</sup>	-200	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	59.5	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation	5	W
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>4</sup>	135	mJ
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Value	Unit
R <sub>thj-c</sub>	Maximum Thermal Resistance, Junction-case	2.1	°C/W
R <sub>thj-a</sub>	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	25	°C/W



# AP3P7R0EMT

## Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	-	7	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	-	-	15	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-	-3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A	-	47	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-10	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±30	uA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =-20A	-	34	54.4	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V	-	12	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =-4.5V	-	11	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =-15V	-	42	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =-20A	-	120	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω	-	460	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =-10V	-	280	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	4300	6880	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =-15V	-	590	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	330	-	pF

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V	-	-	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V,	-	21	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=-100A/μs	-	8	-	nC

### Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤10sec
- 4.Starting T<sub>j</sub>=25°C , V<sub>DD</sub>=-30V , L=0.3mH , R<sub>G</sub>=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

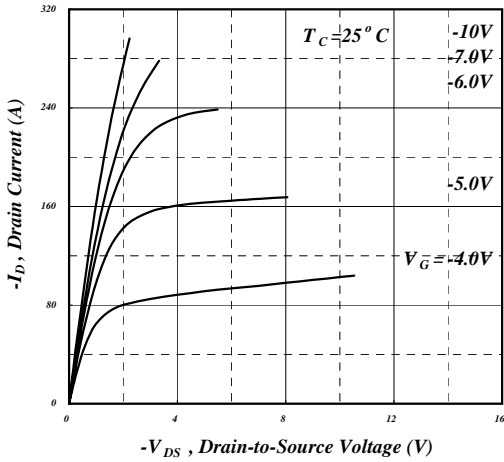


Fig 1. Typical Output Characteristics

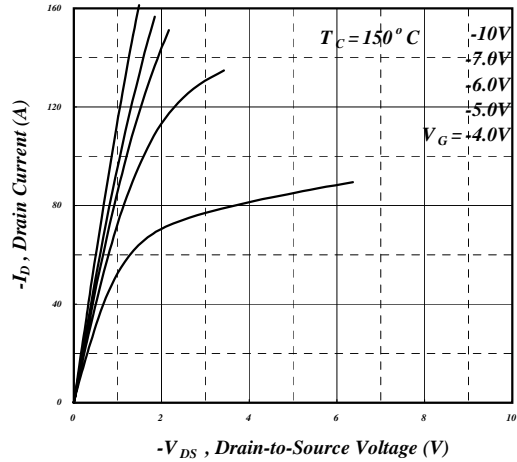


Fig 2. Typical Output Characteristics

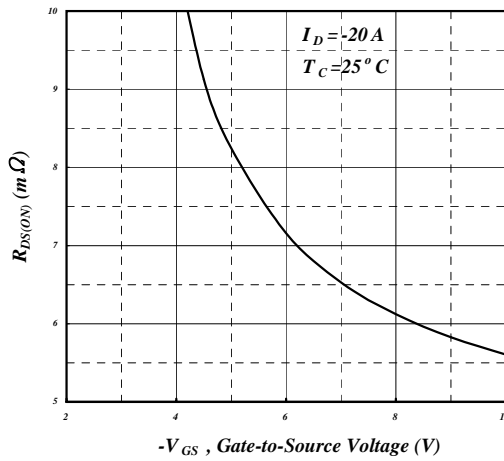


Fig 3. On-Resistance v.s. Gate Voltage

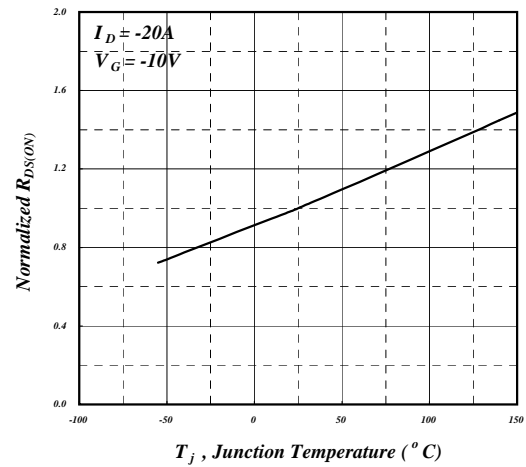


Fig 4. Normalized On-Resistance v.s. Junction Temperature

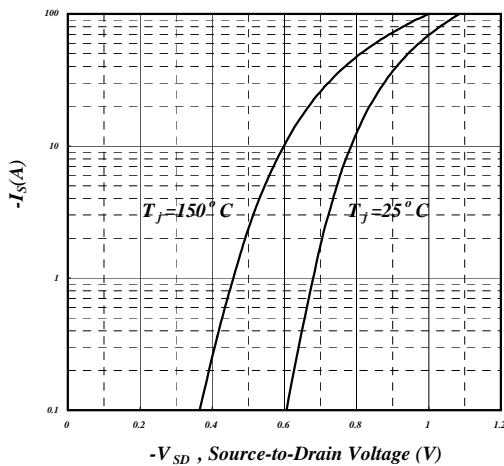


Fig 5. Forward Characteristic of Reverse Diode

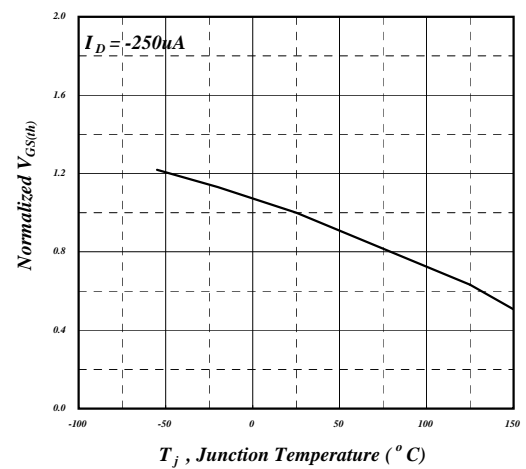
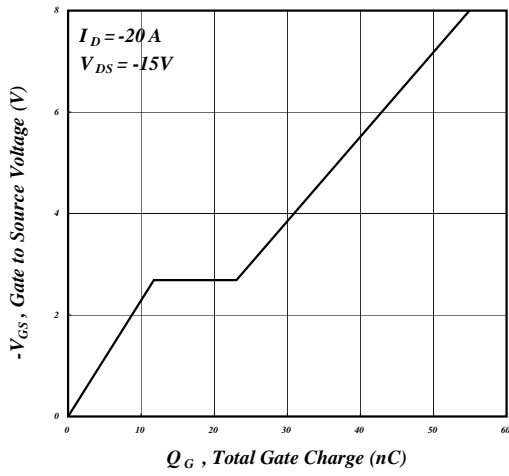
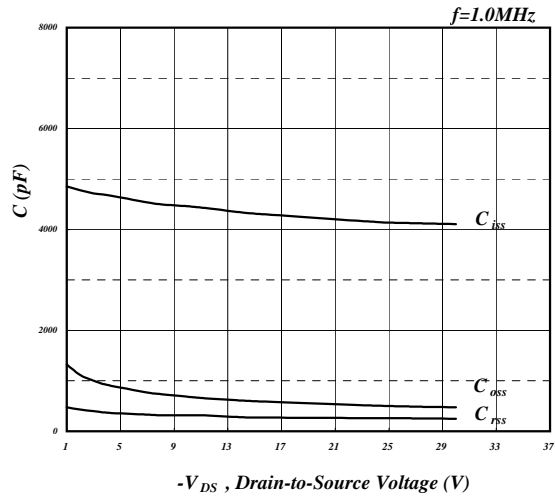


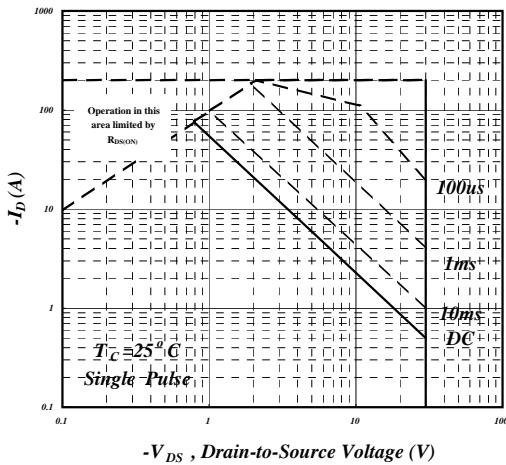
Fig 6. Gate Threshold Voltage v.s. Junction Temperature



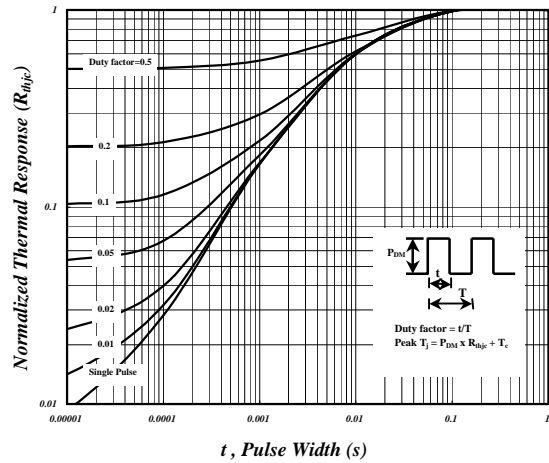
**Fig 7. Gate Charge Characteristics**



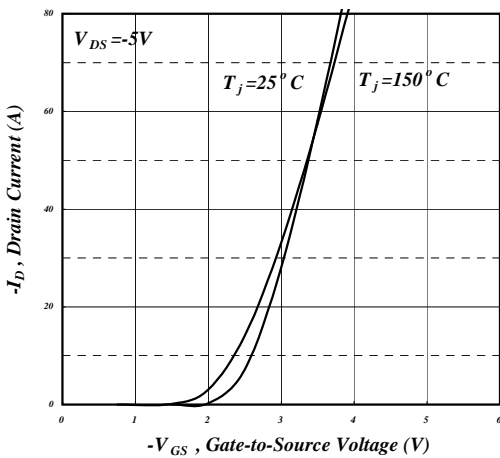
**Fig 8. Typical Capacitance Characteristics**



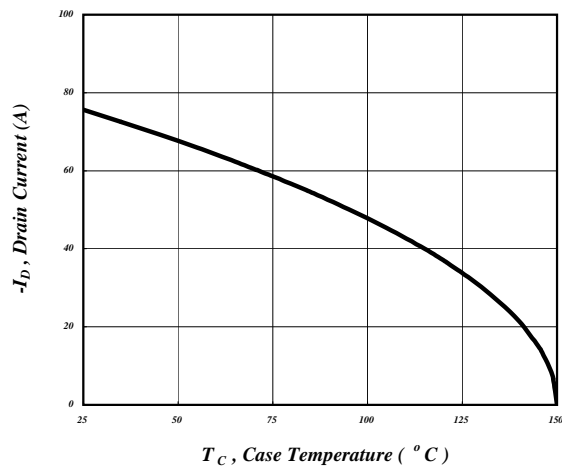
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Transfer Characteristics**



**Fig 12. Drain Current v.s. Case Temperature**

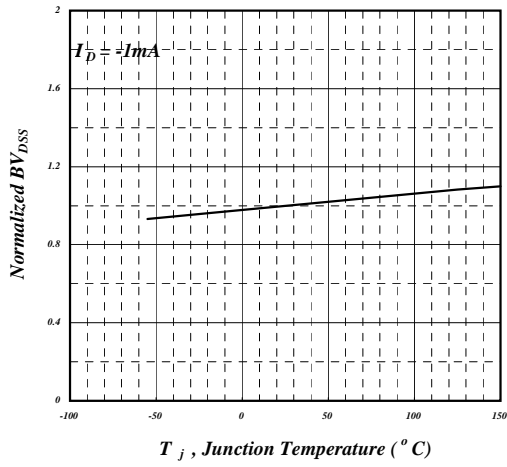


Fig 13. Normalized  $BV_{DSS}$  v.s. Junction Temperature

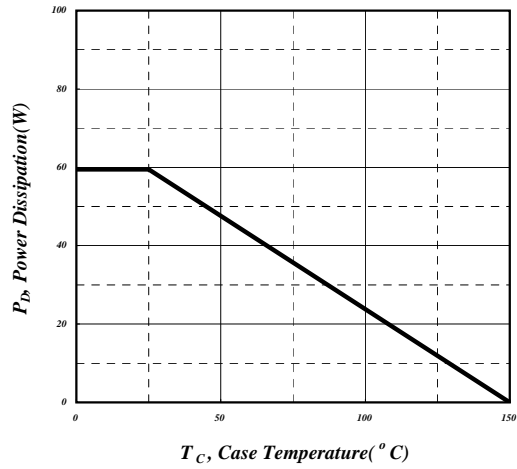


Fig 14. Total Power Dissipation

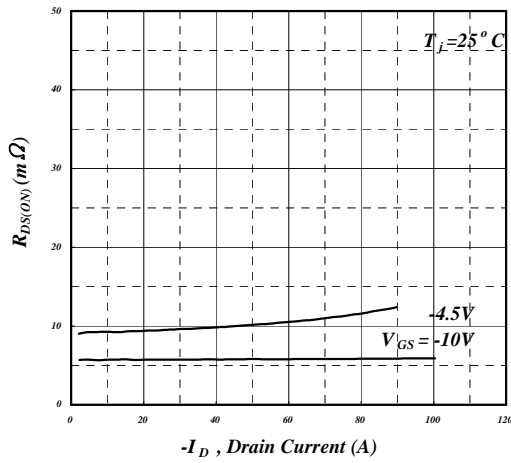


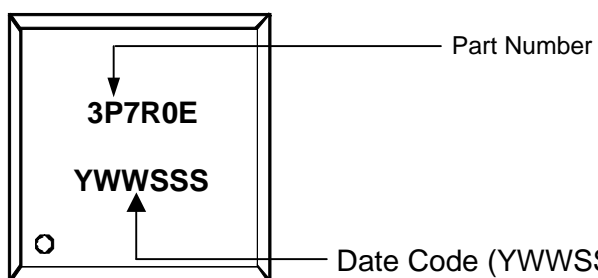
Fig 15. Typ. Drain-Source on State Resistance



# AP3P7R0EMT

## MARKING INFORMATION

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Y : Last Digit Of The Year

WW : Week

SSS : Sequence