3A ULTRA LOW DROPOUT LINEAR REGULATOR

FEATURES

- **Ultra Low Dropout - 0.23V(typical) at 3A Output Current**
- **Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable**
- **0.8V Reference Voltage**
- **Fast Transient Response**
- **Adjustable Output Voltage by External Resistors**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Under-Voltage Protection**
- **Current-Limit and Thermal Shutdown Protection**
- **Power-OK Output with a Delay Time**
- **ESOP-8 & TDFN 3x3-10L Pb-Free & Halogen-Free Package.**

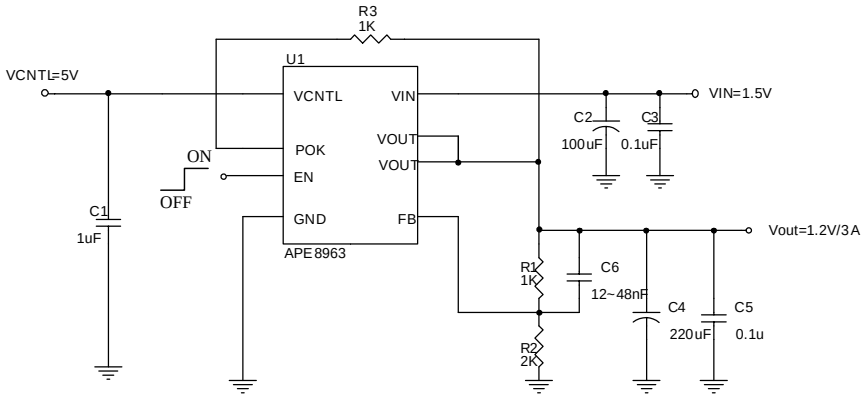
DESCRIPTION

The APE8963 is a 3A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8963 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The APE8963 can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

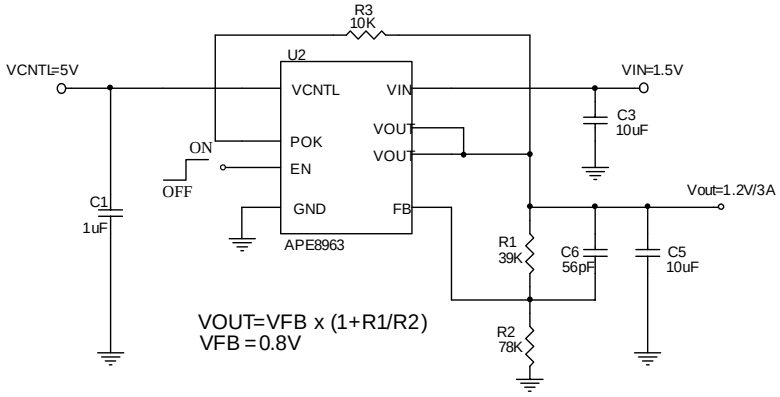
The APE8963 is available in ESOP-8 and TDFN 3x3-10L packages which features small size as an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

TYPICAL APPLICATION

1.Using an Output Capacitor with ESR ≥ 20mΩ

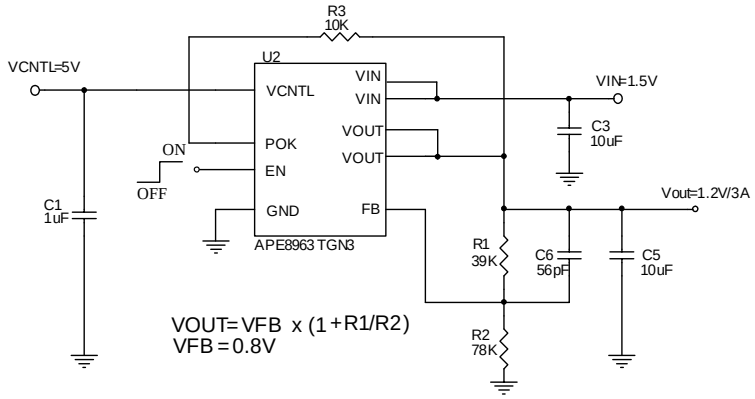


2.Using an MLCC as the Output Capacitor (ESOP-8)



TYPICAL APPLICATION

3.Using an MLCC as the Output Capacitor (TDFN 3x3-10L)



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VCNTL Supply Voltage(V_{CNTL})	-0.3V to 7V
VIN Supply Voltage(V_{IN})	-0.3V to 6V
EN and FB Pin Voltage($V_{I/O}$)	-0.3V to V_{CNTL}+0.3V
Power Good Voltage(V_{POK})	-0.3V to 7V
Power Dissipation(P_D)	
ESOP-8	2.5W
TDFN 3x3-10L	2.2W
Storage Temperature Range(T_{ST})	-65°C to +150°C
Junction Temperature Range(T_J)	-40°C To 125°C
Operating Temperature Range (T_{OP})	-40°C to +85°C
Thermal Resistance from Junction to Case(Rth_{JC})	
ESOP-8	15°C/W
TDFN 3x3-10L	15°C/W
Thermal Resistance from Junction to Ambient(Rth_{JA})	
ESOP-8	40°C/W
TDFN 3x3-10L	45°C/W

Note: Rth_{ja} is measured with the PCB copper area (need connect to Expose-Pad) of approximately 1.5 in^2 (Multi-layer)

RECOMMENDED OPERATING CONDITIONS

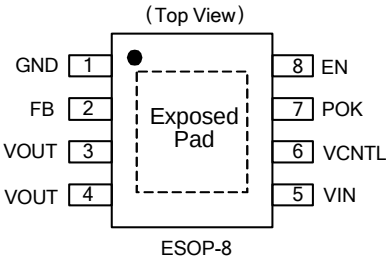
VCNTL Supply Voltage(V_{CNTL})	3V to 5.5V
VIN Supply Voltage(V_{IN})	1.2V to 3.65V
Output Voltage(V_{OUT})	0.8V to V_{IN}-V_{DROP} (V_{CNTL} - V_{OUT} > 1.9V)
Output Current(I_{OUT})	0 to 3A

ORDERING/PACKAGE INFORMATION

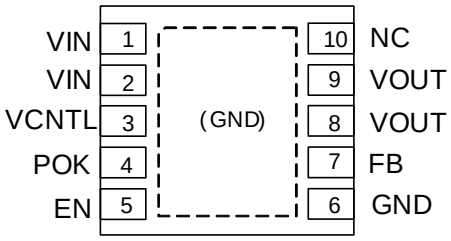
APE8963X

Package Type

MP : ESOP-8
TGN3 : DFN 3x3-10L



ESOP-8



TDFN 3x3-10L

ELECTRICAL SPECIFICATIONS

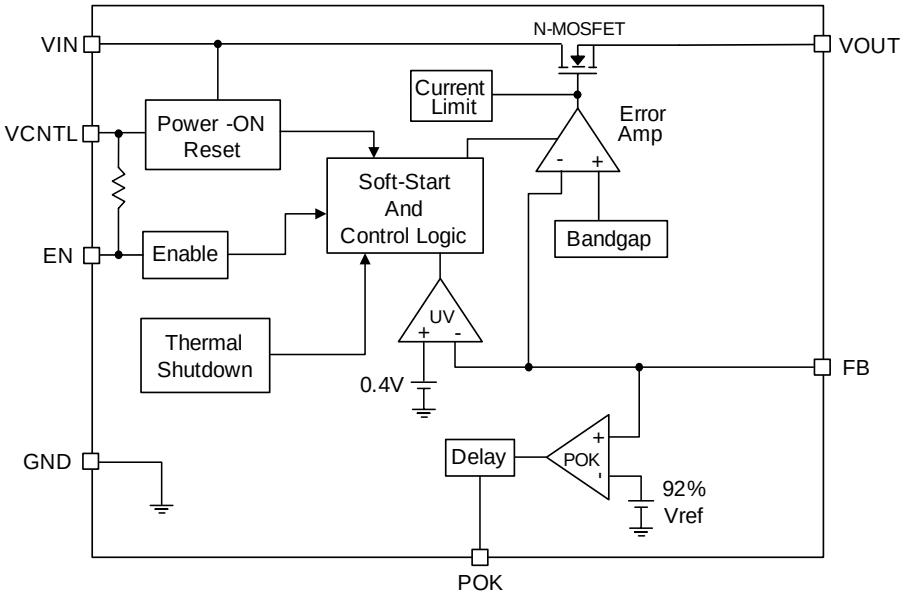
(V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, T_A=25°C unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VCNTL POR Threshold	V_{CNTL}		2.5	2.7	2.9	V
VCNTL POR Hysteresis	$V_{CNTL(hys)}$		-	0.4	-	V
VIN POR Threshold	V_{IN}		0.8	0.9	1	V
VIN POR Hysteresis	$V_{IN(hys)}$		-	0.5	-	V
VCNTL Nominal Supply Current	I_{CNTL}	EN= V_{CNTL}	-	1	1.8	mA
VCNTL Shuntdown Current	I_{SD}	EN= 0V	-	15	30	uA
Feedback Voltage	V_{FB}	V_{CNTL}=5V, I_{OUT} =10mA	0.788	0.8	0.812	V
Load Regulation		I_{OUT}=0A ~ 3A	-	0.06	0.25	%
Line Regulation		V_{CNTL}= V_{EN} =5V V_{IN} = V_{OUT} + 0.5V~5V I_{OUT} =10mA	-	0.01	0.1	%/V
Dropout Voltage	V_{DROP}	I_{OUT} = 3A, V_{CNTL}=5V, V_{OUT}=1.2V	-	0.23	0.28	V
VOUT Pull Low Resistance		EN=0V	-	85	-	Ω
Soft Start Time	T_{SS}		-	2	4	ms
EN Pin Logic High Threshold Voltage	V_{ENH}	Enable	1.2	-	-	V
	V_{ENL}	Disable	-	-	0.4	
EN Hysteresis			-	50	-	mV
EN Pin Pull-Up Current	I_{EN}	EN=GND	-	10	-	uA
Current Limit	I_{LIM}	V_{CNTL}=3~5.5V, T_J= -40 ~ 125°C	3.3	-	-	A
Ripple Rejection VIN	PSRR	F=120Hz, I_{OUT}=100mA	-	65	-	dB
Ripple Rejection VCNTL			-	65	-	
Under-Voltage Threshold		VFB Falling	-	0.4	-	V
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising	89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling	78%	81%	84%	VFB
POK Low Voltage		POK sinks 5mA	-	0.25	0.4	V
POK Delay Time	T_{DELAY}		0.8	2	4	ms
Thermal Shutdown Temp	TSD		-	160	-	°C
Thermal Shutdown Hysteresis			-	50	-	

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
GND	GND Pin
FB	Feedback Pin
EN	Internal Pull High. EN=High or Floating à Enable EN=Low à Shutdown mode
VOUT	Output Voltage pin
POK	Power OK Output Pin
VCNTL	CNTL Pin Input Voltage
VIN	Input Voltage
EP	Connect to VIN or GND

BLOCK DIAGRAM



FUNCTION PIN DESCRIPTION

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad (V)$$

Where R1 is connected from V_{OUT} to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100KΩ.

FUNCTION PIN DESCRIPTION

VIN

Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

EN

Enable control pin. Pulling and holding this pin below 0.3V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, this pin is internal pulled up to VCNTL voltage, enabling the regulator.

VOUT

Output of the regulator. Please connect Pin 3 and Pin 4 using wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

FUNCTION DESCRIPTION

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at V_{CNTL} and V_{IN} pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the V_{CNTL} voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2ms.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from V_{IN} to V_{OUT}.

FUNCTION DESCRIPTION(Cont.)

Current Limit

The APE8963 monitors the current via the output NMOS and limits the maximum current to prevent load and APE8963 from damages during overload or short circuit conditions.

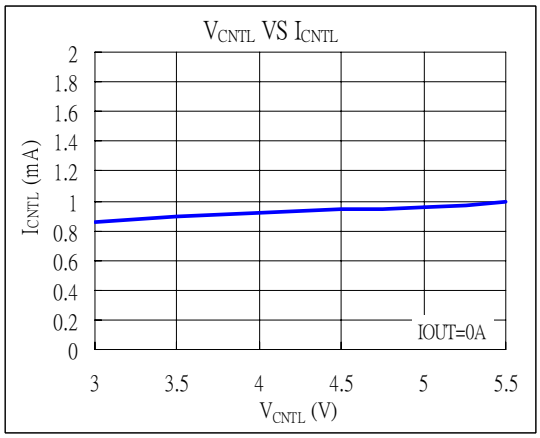
Under-Voltage Protection (UVP)

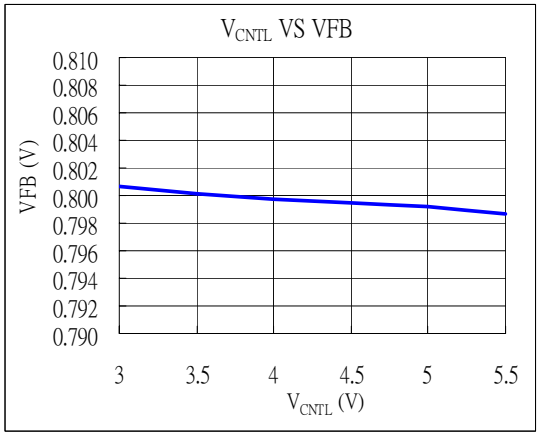
The APE8963 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APE8963 starts a new soft-start to regulate output.

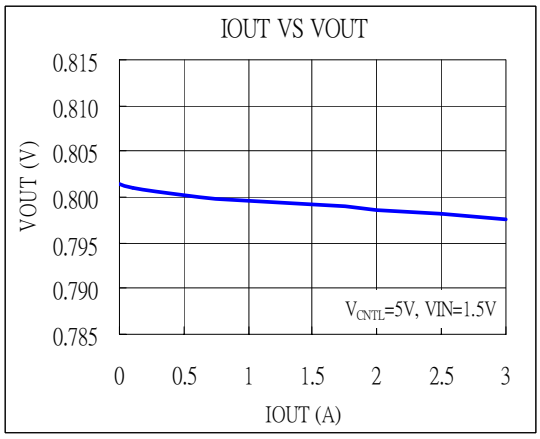
Thermal Shutdown

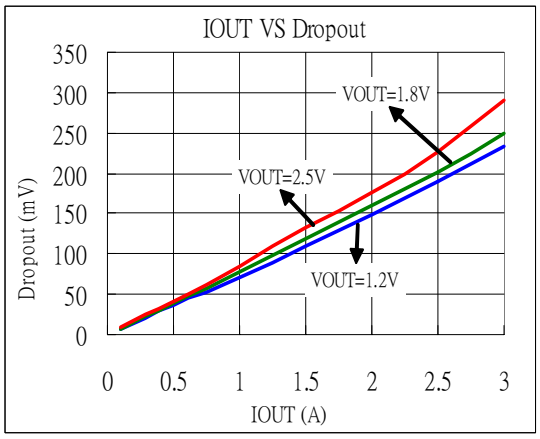
A thermal shutdown circuit limits the junction temperature of APE8963. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed.

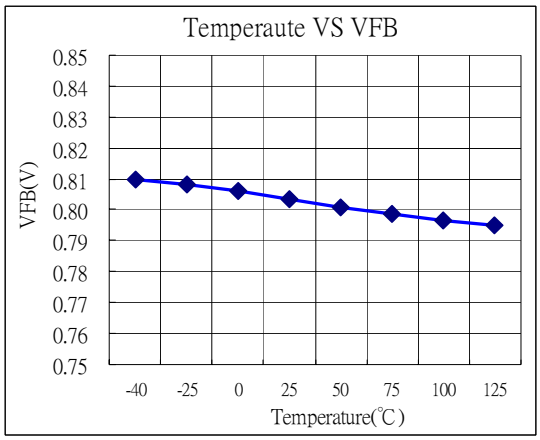
TYPICAL PERFORMANCE CHARACTERISTICS

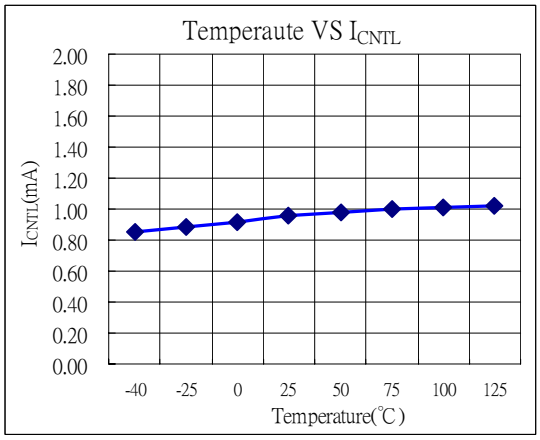






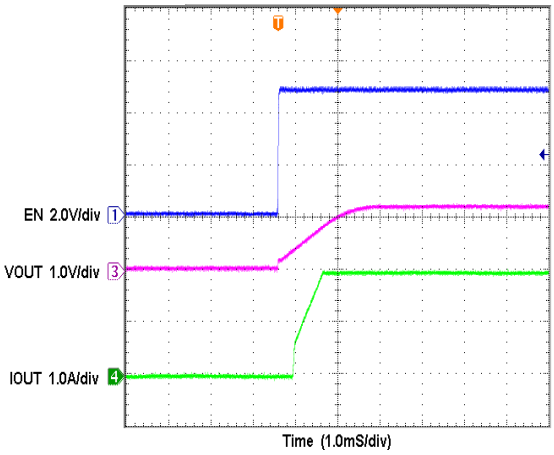




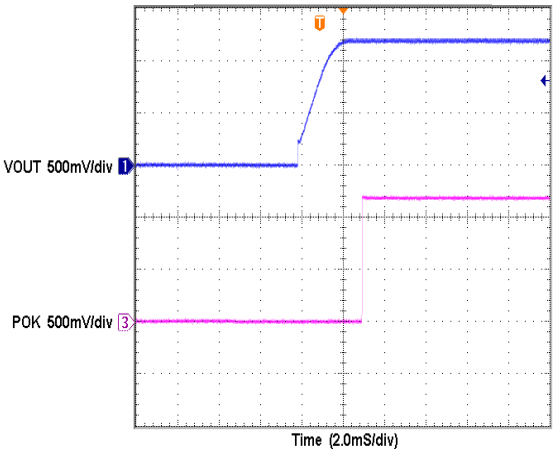


TYPICAL PERFORMANCE CHARACTERISTICS

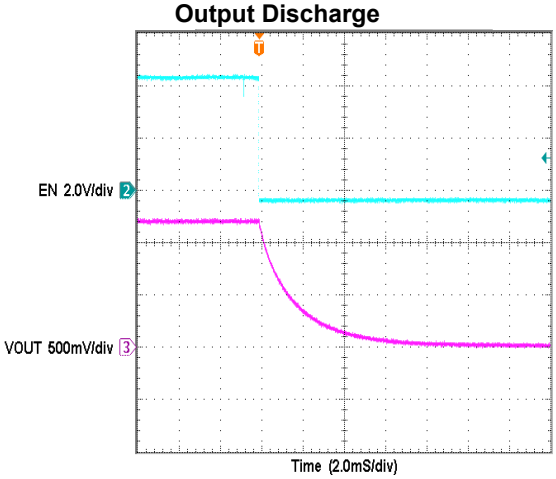
Enable-ON



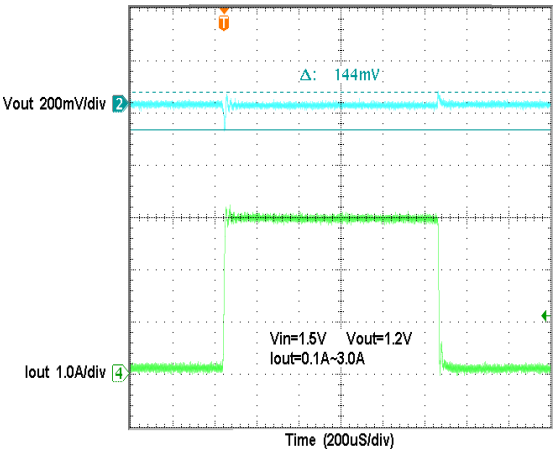
Power OK Wave



Output Discharge

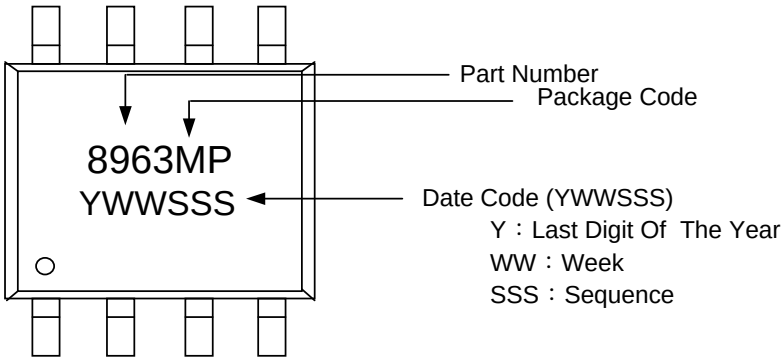


Load Transient



MARKING INFORMATION

ESOP-8



TDFN 3x3-10L