



U74ACT32

CMOS IC

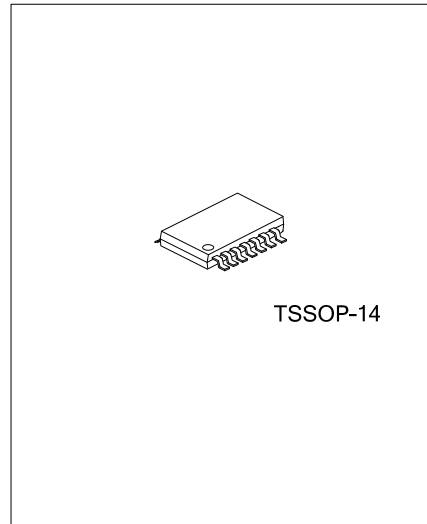
QUADRUPLE 2-INPUT POSITIVE-OR GATES

DESCRIPTION

The **U74ACT32** is an advanced high-speed CMOS QUAD 2-INPUT OR GATES. Each Gate perform the Boolean function $Y=A+B$ or $Y = \overline{A} \cdot \overline{B}$.

FEATURES

- * Operation Voltage Range: 4.5~5.5V
- * Low Power Dissipation: $I_{CC}=2\mu A$ (Max.)
- * High Noise Immunity
- * Compatible With TTL Output

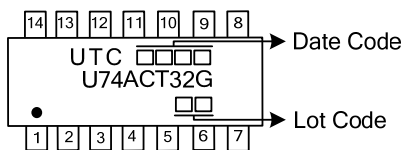


ORDERING INFORMATION

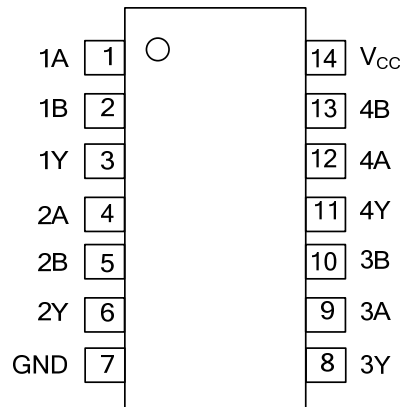
Ordering Number	Package	Packing
U74ACT32G-P14-R	TSSOP-14	Tape Reel

U74ACT32G-P14-R		
(1) Packing Type	(1) R: Tape Reel	
(2) Package Type	(2) P14: TSSOP-14	
(3) Green Package	(3) G: Halogen Free and Lead Free	

MARKING



■ PIN CONFIGURATION

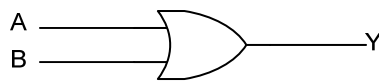


■ FUNCTION TABLE

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	X	H
X	H	H
L	L	L

H = High voltage level : L = Low voltage level : X = Don't care

■ LOGIC DIAGRAM (each gate)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage (Note 2)	V_{IN}		-0.5 ~ + V_{CC} +0.5	V
Output Voltage	V_{OUT}		-0.5 ~ + V_{CC} +0.5	V
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±50	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0$ or $V_{IN} > V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	±20	mA
Continuous Current Through V_{CC} or GND	I_{CC}		±200	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$				8	ns/V
Operating Temperature	T_A		-40		+85	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High Level Input Voltage	V_{IH}	$V_{CC}=4.5\sim 5.5V$	2			V	
Low Level Input Voltage	V_{IL}	$V_{CC}=4.5\sim 5.5V$			0.8	V	
High-Level Output Voltage	V_{OH}	$V_{CC}=4.5V$	$I_{OH}=-24mA$	3.86		V	
			$I_{OH}=-50\mu A$	4.4		V	
		$V_{CC}=5.5V$	$I_{OH}=-24mA$	4.86		V	
			$I_{OH}=-50\mu A$	5.4		V	
Low-Level Output Voltage	V_{OL}	$V_{CC}=4.5V$	$I_{OL}=24mA$		0.36	V	
			$I_{OL}=50\mu A$		0.001	0.1	V
		$V_{CC}=5.5V$	$I_{OL}=24mA$			3.6	V
			$I_{OL}=50\mu A$		0.001	0.1	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND			±0.1	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$			2	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=5.5V$, One input at 3.4V, Other inputs at V_{CC} or GND		0.6		mA	
Input Capacitance	C_I	$V_{CC}=5V, V_{IN}=V_{CC}$ or GND		2.6		pF	

■ SWITCHING CHARACTERISTICS ($C_L=50pF, R_L=500\Omega, T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output(Y)	t_{PLH} / t_{PHL}	$V_{CC}=5V\pm 0.5V$	1.0	6.5	9.0	ns

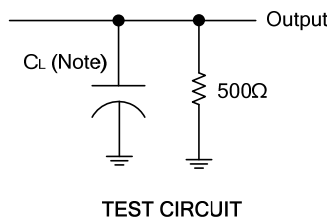
■ OPERATING CHARACTERISTICS ($C_L=50pF, f=10MHz, T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=5.0V$		40		pF

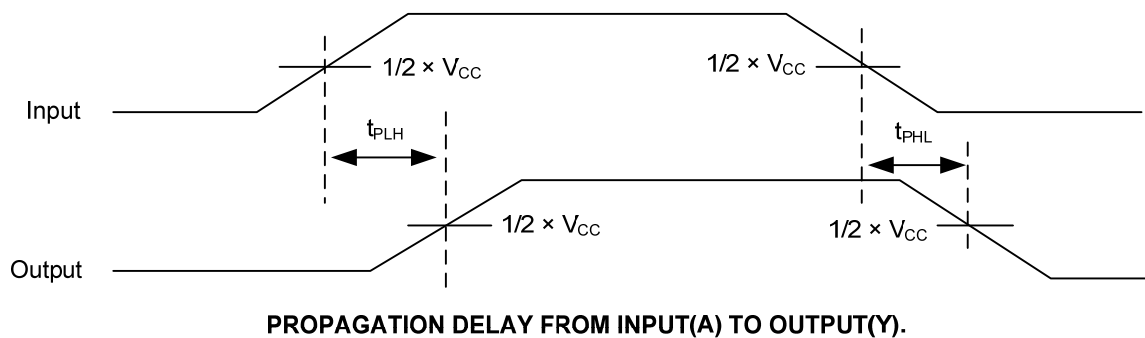
Notes: 1. C_{PD} is used to determine the dynamic power consumption, per inverter.

2. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

■ TEST CIRCUIT AND WAVEFORMS



Note : CL includes probe and jig capacitance.



- Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω.

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