

## RPT7050J

The RPT7050J uses Rakon's new patented, Pluto+ ASIC. Pluto+ advances on the world famous, ‘best-in-class’ Pluto ASIC technology by providing enhanced frequency versus temperature stability. It also delivers to the industry the lowest jitter achievable from an ultra-stable TCXO. This allows the oscillator to be compliant with various standards including GR-1244, GR-253, G.812, G.813, G.8262 and G.827x.

### Features

- Best in class frequency versus temperature
- RMS phase jitter down to 0.13ps
- Phase noise <-160dBc/Hz floor
- Excellent holdover stability

### Applications

- Stratum 3 / IEEE 1588 / SyncE
- SONET / SDH / WDM / OTN
- Carrier Ethernet / Microwave
- Backhaul / Transport Equipment

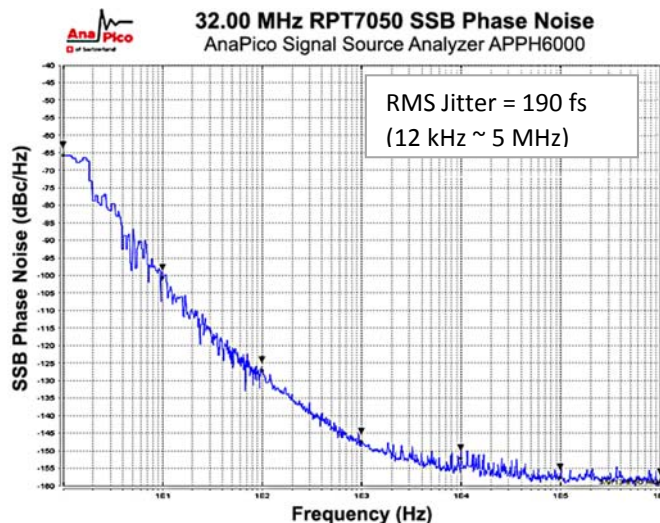
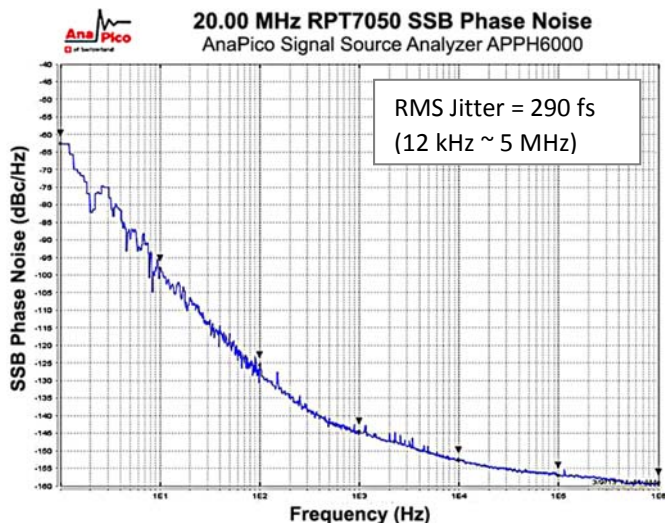
7.0 x 5.0 x 2.0 mm



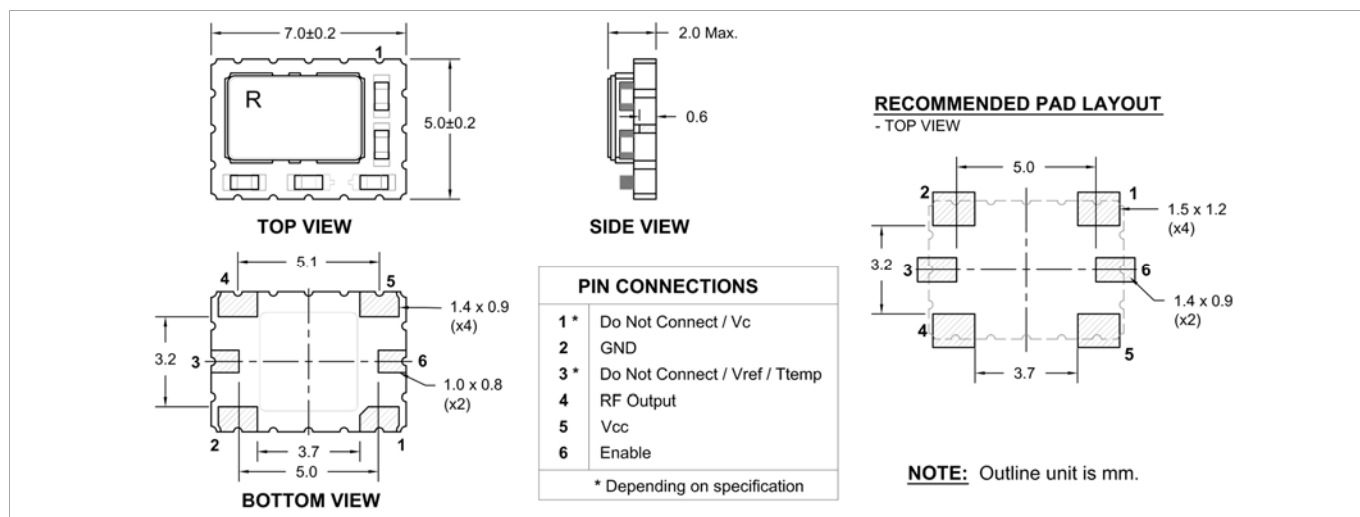
## Standard Specifications

| Parameter                                    | Min.               | Typ.    | Max.               | Unit              | Test Condition / Description  |
|--|--------------------|---------|--------------------|-------------------|---|
| Nominal frequency                            |                    | 10 – 40 |                    | MHz               | Standard frequencies: 10, 12.8, 16.384, 19.44, 20, 20.48, 24.576, 25, 30.72, 38.88 and 40MHz  |
| Operating temperature range                  | -40                |         | 85                 | °C                |   |
| Holdover stability, variable temperature     |                    |         | ±100 – ±280        | ppb               | The default reference for holdover stability, variable temperature is (Fmax + Fmin)/2   |
| Holdover stability, constant temperature     |                    |         | ±10 – ±40          | ppb               | ±10ppb after 10 days of continuous operation, ±40ppb after 48 hours of continuous operation   |
| Slope over temperature (ΔF/ΔT)               |                    |         | ±20 – ±100         | ppb/°C            |   |
| Free-run accuracy                            |                    |         | ±4.6               | ppm               | Inclusive of calibration tolerance at 25°C, temperature, supply voltage variation ±5%, load variation ±5pF, reflow soldering and 20 years ageing reference to the nominal frequency |
| Wander generation<br>TDEV / MTIE             |                    |         |                    |                   | TDEV compliant with GR-1244 fig 5-4, G.812 types II & III fig 2, G.813, G.8262<br>MTIE compliant with GR-1244 Fig 5-5, G.812 types II & III fig 1, G.813, G.8262                    |
| Supply voltage stability                     |                    | ±0.025  |                    | ppm               | ±5% variation, reference to frequency at nominal supply voltage   |
| Acceleration stability                       |                    | < 2     |                    | ppb/g             | Gamma vector, 3 axes, 30 – 1500Hz   |
| Start-up time                                |                    |         | 5 – 15             | ms                | 90% amplitude   |
| Root Allan Variance                          |                    | 5       |                    | 10 <sup>-11</sup> | tau = 1.0s  |
| Supply voltage, V <sub>CC</sub>              |                    | 3.3     |                    | V                 | ±5%   |
| Supply current                               | 3                  |         | 6                  | mA                | Depending on nominal frequency  |
| Oscillator output – HCMOS                    |                    |         |                    |                   | LVC MOS & LV TTL compatible as per JESD8C   |
| Output voltage level high (V <sub>OH</sub> ) | 0.9V <sub>CC</sub> |         |                    | V                 |   |
| Output voltage level low (V <sub>OL</sub> )  |                    |         | 0.1V <sub>CC</sub> | V                 |   |
| Duty cycle                                   | 45                 |         | 55                 | %                 | At 50% level  |
| Rise & fall time                             |                    |         | 8                  | ns                | Between 10% and 90%   |
| Load   | 0                  | 15      | 30                 | pF                |   |
| Tri-state control                            |                    |         |                    |                   |   |
| Input level low (pin 6)                      |                    |         | 0.2V <sub>CC</sub> | V                 | Device disabled, output in high impedance state   |
| Input level high (pin 6)                     | 0.6V <sub>CC</sub> |         |                    | V                 | Device enabled and operating  |

### SSB Phase Noise (Typical value at 25°C)



### Model Outline and Recommended Pad Layout



### Test Circuit

