CDB61880

Octal E1 Line Interface Evaluation Board

Features

- Socketed CS61880 Octal Line Interface Unit
- Binding post connectors for power and line interface connections
- Components supplied for all operational modes E1 75 Ω and E1 120 Ω
- Socketed termination circuitry for easy testing
- Connector for IEEE 1149.1 JTAG Boundary Scan
- LED Indicators for Loss of Signal (LOS) and power
- Supports Hardware, Serial, and Parallel Host Modes
- Easy-to-use evaluation software
- On-board socketed reference clock oscillator

Description

The CS61880 evaluation board is used to demonstrate the functions of a CS61880 Octal Line Interface Unit in either E1 75 Ω or E1 120 Ω.

The evaluation board can be operated in either Hardware mode or Host mode. In Hardware mode, switches and bed stake headers are used to control the line configuration and channel operations for all eight channels. In Host mode (Serial or Parallel), the evaluation software, switches, and bed stake headers are used to control the line configuration and operating mode settings for each channel.

In both Hardware and Host modes, the board may be configured for E1 75 Ω or E1 120 Ω operating modes. In both modes binding post connectors provide easy connections between the line interface connections of the CS61880 and any E1 analyzing equipment, which may be used to evaluate the CS61880 device. Bed stake headers allow easy access to each channel's clock and data I/O digital interface.

Eight LED indictors display the Loss of Signal (LOS) conditions for each channel during Hardware and Host modes. An LED indictor is used on the Interrupt pin to indicate a change of state.

Note: Click on any text in blue to go to cross-references

ORDERING INFORMATION
CS61880-IQ   -40° to 85° C   144-pin LQFP
CDB61880   Evaluation Board

Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CDB61880 EVALUATION BOARD LAYOUT

Figure 1. CDB61880 Board Layout

2. BOARD COMPONENT DESCRIPTIONS

2.1 Power Connections

Power for the CDB61880 evaluation board is supplied by an external +3.3 V DC power supply. A +5 V DC power supply can also be connected to the on-board control logic. The LED labeled "D3" will illuminate when power is supplied to the on-board control logic.

- Connect the +3.3 VDC power supply to the +3 V binding post and the +5 VDC power supply to the +5 V binding post if 5 Volt logic is required
- Jumper J13 shown in Figure 2 allows all the external logic on the evaluation board to be connected to either +3 V or +5 V binding post.

On-board logic connected to +3 V binding post

On-board logic connected to +5 V binding post
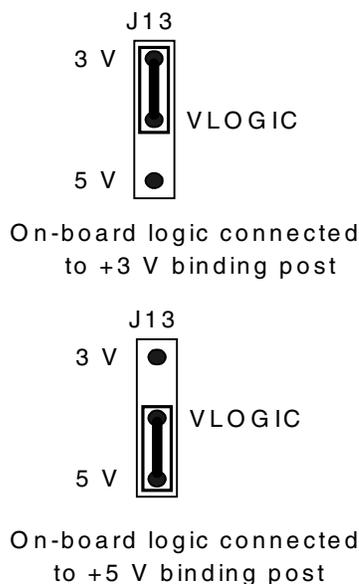
Figure 2. On-board Logic Power Selection

- To measure the current consumption of only the CS61880 device, place a short block on Jumper J13 to connect the Vlogic power supplies to the +5 V binding post. This will isolate the CS61880 device from all the on-board logic, to allow the current measurement to be made at the +3 V binding post.

2.2 Master Clock Selection

In both Hardware and Host modes, the MCLK pin is configured by placing a short block on one of the positions of bed stake header J1. Figure 3 shows the different positions of the J1 bed stake header.
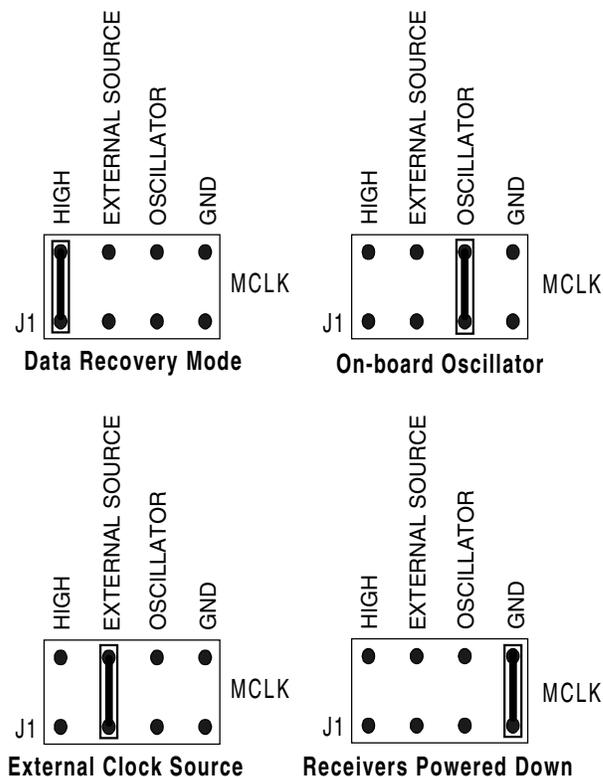
Figure 3. Master Clock Selections

- A 2.048 MHz clock oscillator is provided on the evaluation board for use as the on-board clock source for all E1 modes.
- A BNC connector (labeled J16) provides the connection for an external clock source.

2.3 Operating Mode Selection

The operating mode for the CS61880 can be selected by setting switch S15 to one of the positions shown in Figure 4.
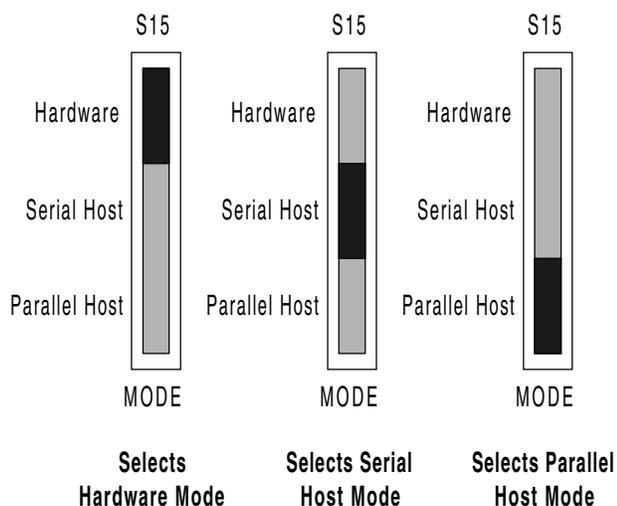
Figure 4. Hardware/Host Mode Selection

2.4 Line Interface Connections

In both hardware and host modes, the receive line signals (RTIP/RRING) are connected to the binding post labeled RXT 0-7 and RXR 0-7. The line signals from the binding posts are coupled to the device through two octal transformers (T1 and T9).

The receivers of the device use external resistors to match the line impedance. These resistors are socketed for ease in changing the line impedance, for internal or external line impedance matching. During internal line impedance matching mode, the resistor values are the same (15 Ω) for all modes of operation: E1 75 Ω and E1 120 Ω. During external line impedance matching mode the receiver resistors need to be change to the values shown in Table 1.

Table 1. External Impedance Resistor Values

E1 75 Ω	E1 120 Ω
9.31Ω	15Ω

The jumpers listed in Table 2 are used to place or bypass 1 KΩ protection resistors in series with the receive line signals (RTIP/RRING). These resistors are used for receiver protection while in external line impedance matching mode and should not be used during internal line impedance matching mode. To place the 1 KΩ resistors in series with the receive line signals, remove the short blocks from each of the jumpers described in Table 2. To bypass the 1 KΩ resistors, place a short block on each jumper shown in Table 2.

Table 2. Protection Resistor Selection

Jumper	Description
J29	Channel 0 RRING signal
J30	Channel 0 RTIP Signal
J37	Channel 1 RTIP Signal
J38	Channel 1 RRING Signal
J46	Channel 2 RRING Signal
J47	Channel 2 RTIP Signal
J54	Channel 3 RTIP Signal
J55	Channel 3 RRING Signal
J65	Channel 4 RRING Signal
J66	Channel 4 RTIP Signal
J73	Channel 5 RTIP Signal
J74	Channel 5 RRING Signal
J81	Channel 6 RRING Signal
J82	Channel 6 RTIP Signal
J89	Channel 7 RTIP Signal
J90	Channel 7 RRING Signal

The transmit line signals (TTIP/TRING) from the device are coupled to the line binding post (TXT 0-7 and TXR 0-7) through two octal transformers (T1 and T9). External protection circuitry such as diodes or chokes are recommended for protection. For further information on line protection refer to Application Note AN34, *Secondary Line Protection for T1 and E1 Line Cards* (AN34REV1 SEP '94).

2.5 TXOE Selection

Jumper J23 is used to enable or High-Z all eight transmitters in both hardware and host mode. A shorting block on Jumper J23 places all the trans-

mitters in a high impedance state. Removing the shorting block, enables the transmitters. See Figure 5.
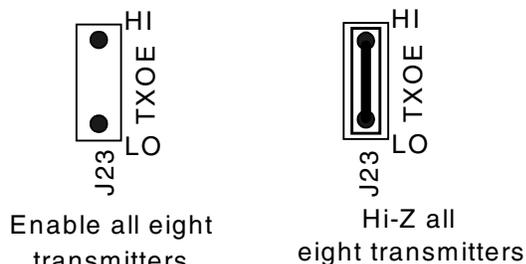
Figure 5. Transmitter Enable Selection

2.6 Clock Edge Selection

In clock/data recovery mode, jumper J93 selects the edge of RCLK and SCLK on which the RPOS/RDATA, RNEG, and SDO data signals are valid. When in data recovery mode, jumper J93 selects the output polarity of RPOS/RNEG. The function of J93 applies to both the Hardware and Host mode. Figure 6 shows the settings for jumper J93 and the effect in both clock/data recovery and data recovery only mode.
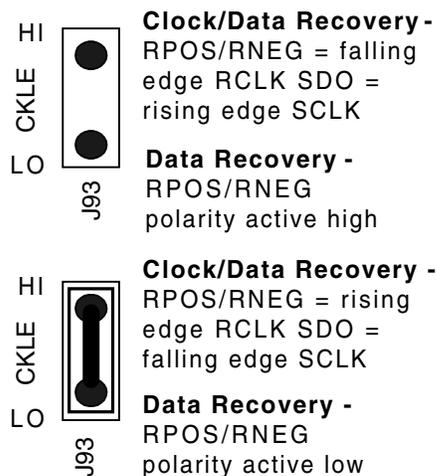
Figure 6. Clock Edge Selection

2.7 Jitter Attenuator Selection

In Hardware mode, switch S10 (JASEL) controls the position of the jitter attenuator for all eight channels. The corner frequency and FIFO length

can not be changed in Hardware mode. Figure 7 shows the settings for switch S10.

In Host mode, switch S10 has no effect on the CS61880 device and should be set to the open (middle) position.
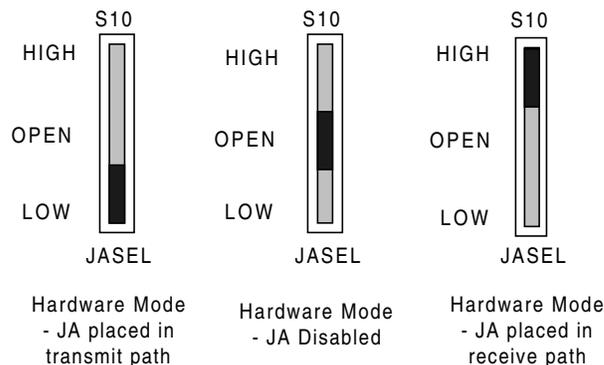
Figure 7. Jitter Attenuator Selection

2.8 Loopback Mode Selection

In Hardware mode, the Loopback modes are configured with switches S1 through S8 (0-7). Figure 8 shows the three different settings for all eight loop back switches.

In Host mode, switches S1 through S8 must be set to the NONE (middle) position to allow host interface control.
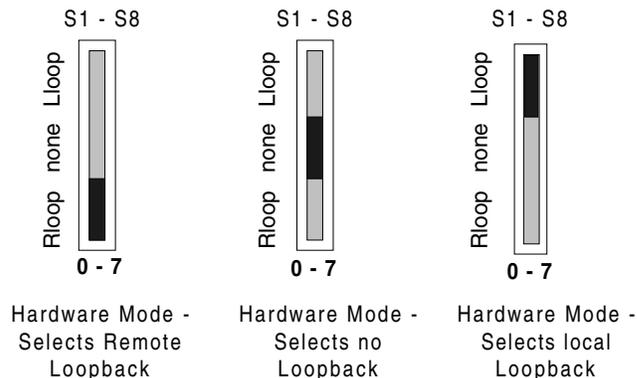
Figure 8. Loopback Mode Selection

2.9 Line Length/Impedance Selection

In Hardware mode, switch S11 (CBLSEL) is used to set the internal or external line impedance for all eight channels. The CBLSEL switch is also used to select the desired pulse shape to be transmitted by the device. Refer to the *CS61880 Data Sheet* for the CBLSEL settings.

In Host mode, switch S11 has no effect on the CS61880 device and should be set to the NC (middle) position.

2.10 Coder/Motorola/Intel Selection

In Hardware mode, switch 1 ($\overline{\text{MOT}}$/INTL) inside switch block S9 (S9 #1) is used to enable AMI or HDB3 line coding. Setting switch S9 #1 to the open (HIGH) position enables AMI coding and the closed (low) position enables HDB3 coding.

In Host mode, switch S9 #1 is used to select either Motorola or Intel Parallel Host mode. When set to the open (HIGH) position Intel mode is selected and the closed (LOW) position enables Motorola mode. Figure 9 shows the settings for switch S9 #1 in Hardware and Parallel Host mode.

2.11 G.772 Monitoring Address Selection

In Hardware mode, the address for the G.772 Non-Intrusive monitoring feature is selected by switches 3 through 7 (A4-A0) inside switch block S9. When switches 3 through 7 inside switch block S9 are all set to the closed "LOW" position, the G.772 Non-Intrusive monitoring function is disabled. Refer to the *CS61880 Data Sheet* for more address settings.

In Host mode, switches 3 through 7 inside switch block S9 must be set to the open (high) position so that the host interface can have control over the address signals during Parallel Host modes.

2.12 Mux/Non-Mux/BITS Clock Selection

In Hardware mode, switch 2 (MUX) inside switch block S9 enables or disables the Channel #0 G.703 BITS Clock function. Placing switch S9 #2 in the open "HIGH" position enables Channel #0 G.703 BITS Clock function and the closed "LOW" position disables this function.

In Host mode, switch S9 #2 (MUX) is used to select multiplex or non-multiplex. Placing switch S9 #2 in the open "HIGH" position selects multiplex and the closed "LOW" position selects Non-multiplex.

Hardware Mode - Enables AMI coding & enables Channel 0 G.703 Bits Clock function

Hardware Mode - Enables HDB3/B8ZS coding & disables Channel 0 G.703 Bits Clock function

Parallel Host Mode - Enables Motorola Non-Multiplex parallel host mode
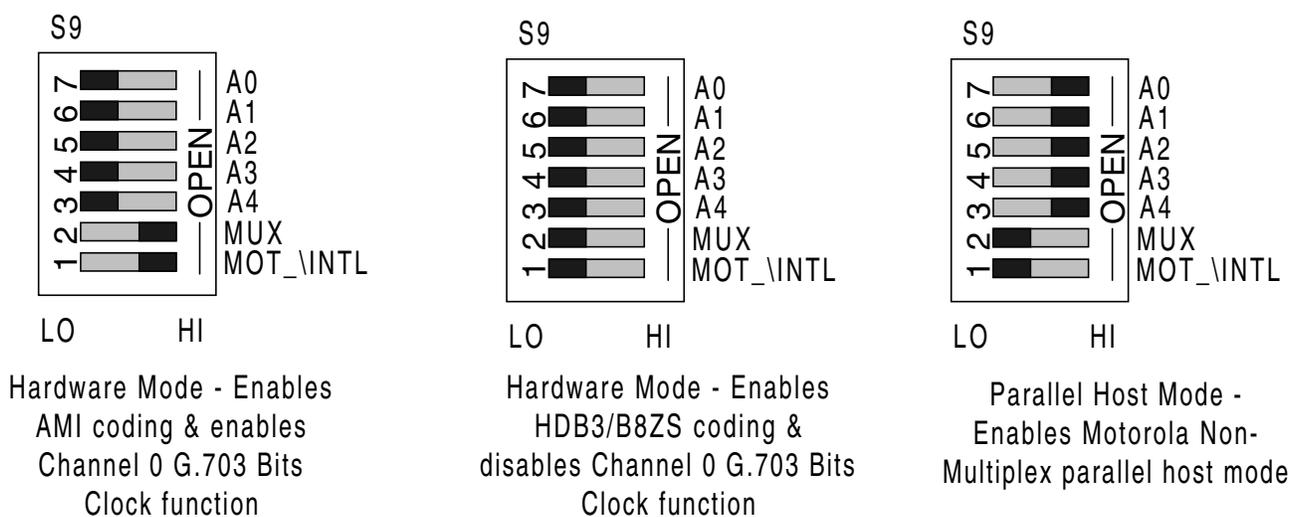
Figure 9. Switch S9 Settings

2.13 Digital Signal Connections

There are eight fourteen pin bed stake headers (labeled J4 through J11) that provide access to the digital signals used to interface with back-end devices (framers, mappers, ASIC, etc.) and all eight LOS signals, in both Hardware And Host mode. Figure 10 shows the layout for one of the eight 14-pin bed stake headers used to access the back-end digital signals, LOS signals and the different settings for the TCLK/TNEG pins.
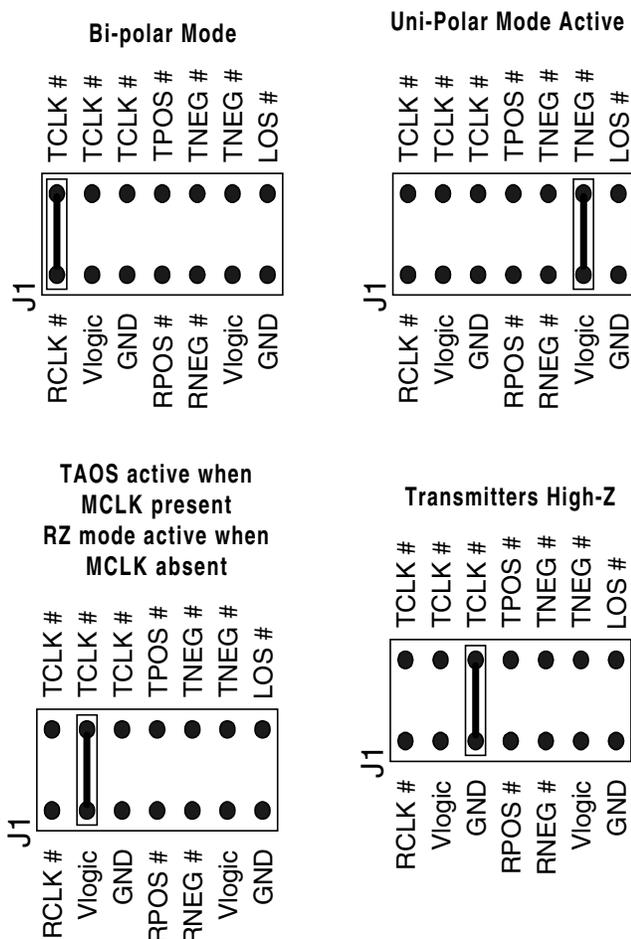
Figure 10. Digital Signal Control/Access

2.14 LOS Indicators

The two 4-LED packs D1 and D2 (labeled ALOS 0-7) represent the LOS signal status for LOS 0-7 pins. The ALOS 0-7 LEDs will illuminate when the corresponding receiver has detected a loss of signal condition. Refer to the *CS61880 Data Sheet* for LOS conditions.

2.15 JTAG Connection

A 5-pin bed stake header (J60) is provided to allow easy access to the IEEE 1149.1 JTAG Boundary Scan signals from the device.

2.16 Host Interface Connection

Connector J12 is used to connect the CS61880 evaluation board to the host computer, through a standard 25 pin male to female parallel port cable. No external μController board is required for host interface connection. This connector is used for both serial and parallel interface.

3. HOST SETUP DESCRIPTION

Place the switches shown in Table 3 to the stated configuration before setting the Mode switch (S15) to Serial or Parallel Host mode. Refer to Figure 4 on page 6 for switch S15 settings.

Table 3. Switch Settings for Host Mode

Switch	Position
S1 through S8	NONE (middle)
S9 # 3 through # 7	OPEN (low)
S10	OPEN (middle)
S11	NC (middle)
S12 through S14	OPEN (middle)

- Switches #1 and #2 inside of switch block S9 are used in Parallel Host mode to select Motorola, Intel, multiplex or Non-multiplex modes. Switch S9 #1 and #2 are not used in Serial Host mode.

4. HOST SOFTWARE INTERFACE

The software provided with the CDB61880 evaluation board is used to control and monitor the CS61880 device. The program is designed to automatically read back each bit after each write. If the bit is read back incorrectly an error will occur. The following registers do not have the automatic read back function:

- AWG Phase Address
- AWG Phase Data,
- Software Reset registers.

4.1 Starting the Software

There is no installation procedure associated with the CS61880 software, simply click on the appropriate CS61880 software icon (Win95 or NT) on the CD in the CDB61880 kit. The CS61880 software is used to evaluate the CS61880 device.

NOTE: The software can be used with Windows$^{®}$ 95$^{®}$, 98$^{®}$, NT$^{®}$ or 2000$^{®}$.

Figure 11 shows the opening screen that appears after you have launched the software.

4.2 Software Interface Buttons

The following subsections explain the functions of buttons that are common to the register configuration screens in the CS61880 software.

4.2.1 Bit Indicator Description

The **Register Bit** checkbox shown in Figure 12 shows one bit, each register consists of eight bits (0 through 7). The grayed-out bits in some registers are bits that can not be accessed. Figure 12 shows a bit with a check mark and without a check mark. A check represents a "1" and no check mark equals a "0".

Figure 12. Register Bit Box

4.3 Set All Button Description

The **Set All** button shown in Figure 13 is used to set all the bits in the corresponding register to 1s. This button is placed to the left of each register that has write access.

Figure 13. Set All Button

Figure 11. CS61884 Software Opening Screen

4.3.1 Clear All Button Description

The **CLR All** Button shown Figure 14 is used to set all the bits in the corresponding register to 0s. This button is placed to the left of each register that has write access.

Figure 14. Clear All Button

4.3.2 Write All Button Description

The **Write All** button shown in Figure 15 writes every bit of every register on the current register screen. This button is located in the bottom right corner of each register screen.

Figure 15. Write All Button

4.3.3 Read All Button Description

The **Read All** button shown in Figure 16 reads every bit of every register on the current register screen. This button is located in the bottom left corner of each register screen.

Figure 16. Read All Button

4.4 Write Button Description

The **Write** button shown in Figure 17 writes the bits of the corresponding register. This button is located to the right of every register that allows write access.

Figure 17. Write Button

4.5 Read Button Description

The **Read** button shown in Figure 18 reads the bits of the corresponding register. This button is located to the right of every register.

Figure 18. Read Button

4.6 Program Exit Function

To exit any of the register screens simple press the X in the top right hand corner of each screen. This

5. CS61880 CONFIGURATION SCREENS

5.1 Choose Parallel Port Settings

The opening screen shown before in Figure 11 and now in Figure 19 is used for the following configuration activities:

- Select the Parallel Port mode of operation
- Select the parallel port address

Click the appropriate radio button to choose the operational modes you wish to use.

Important Notes:
1. If the mode of operation does not match the mode switches on the evaluation board, an error will occur.
2. If the parallel port address does not match the address of the control parallel port, access to the register bits will not be permitted.

5.2 Access and Configure the Read / Write Registers

You also use the opening screen to access the tabbed configuration screens for the Read / Write Registers.

5.2.1 Access Configuration Screens

Click on the **Read/ Write Registers** button on the opening screen to start configuring these registers.

5.2.2 Select Register to Configure

When the next screen appears, select the desired register screen by clicking on one of the TABs labeled **Loopback/Bits Clk**, **LOS/AIS/DFM**, **XMIT**, **AWG,** or **GCR** at the top of the Read/Write Register screen.
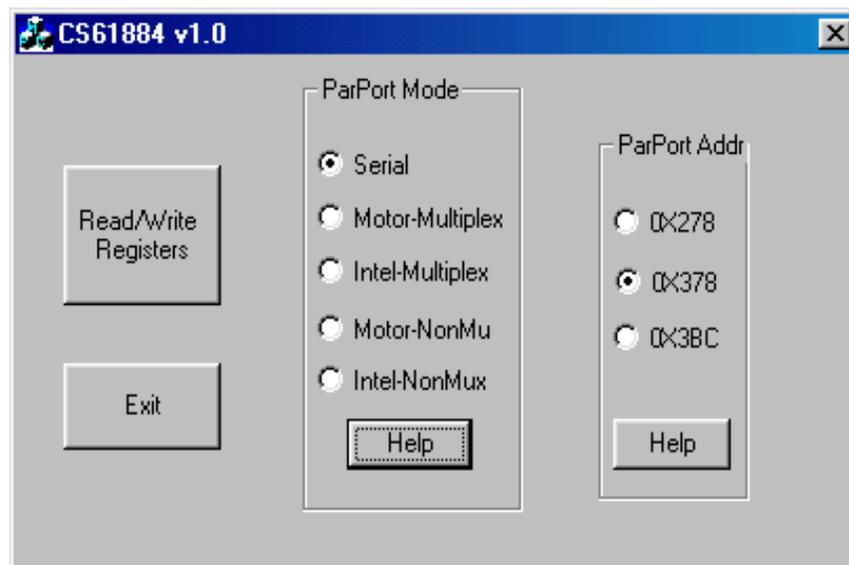
Figure 19. Opening Screen for Port and Address Selection Screen

5.3 Loopback /Bits Clock Screen

The Loopback /Bits Clock Register tabbed screen shown in Figure 20 allows access to the following registers:

- Remote loop back
- Analog loop back
- Digital Loopback
- G.703 Bits Clock
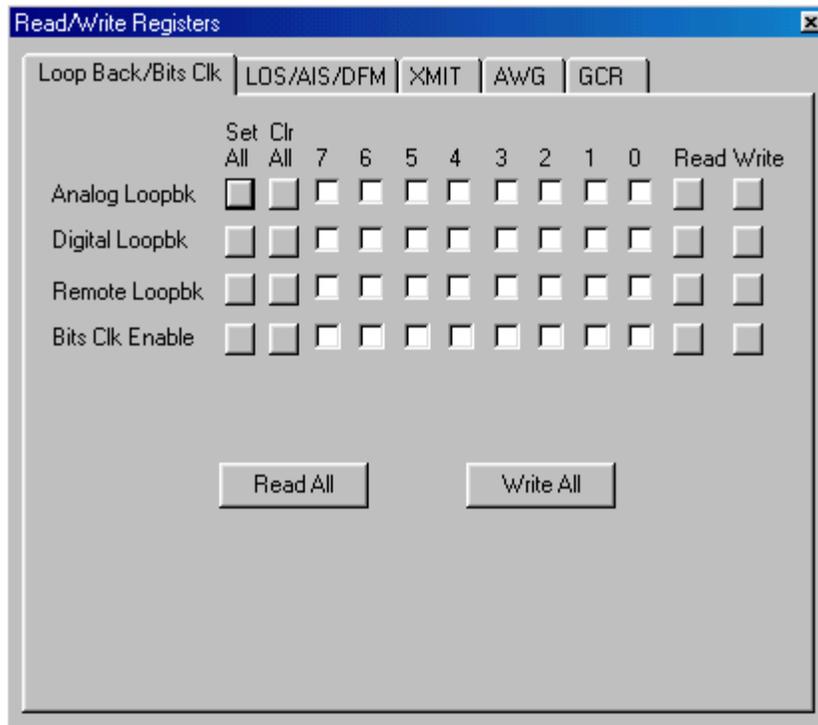
Figure 20. Loopback/G.703 Bits Clock Selection Screen

5.4 LOS/AIS/DFM/JA Register Screen

The LOS/AIS/DFM/JA Register tabbed screen shown in Figure 21 allows access to the following registers:

- LOS Status
- LOS Interrupt Enable
- LOS Interrupt Status
- LOS/AIS Mode Enable

- DFM Status
- DFM interrupt Status
- DFM Interrupt Enable
- AIS Status
- AIS Interrupt Enable
- AIS Interrupt Status
- JA Error Interrupt Enable
- JA Error Interrupt Status.
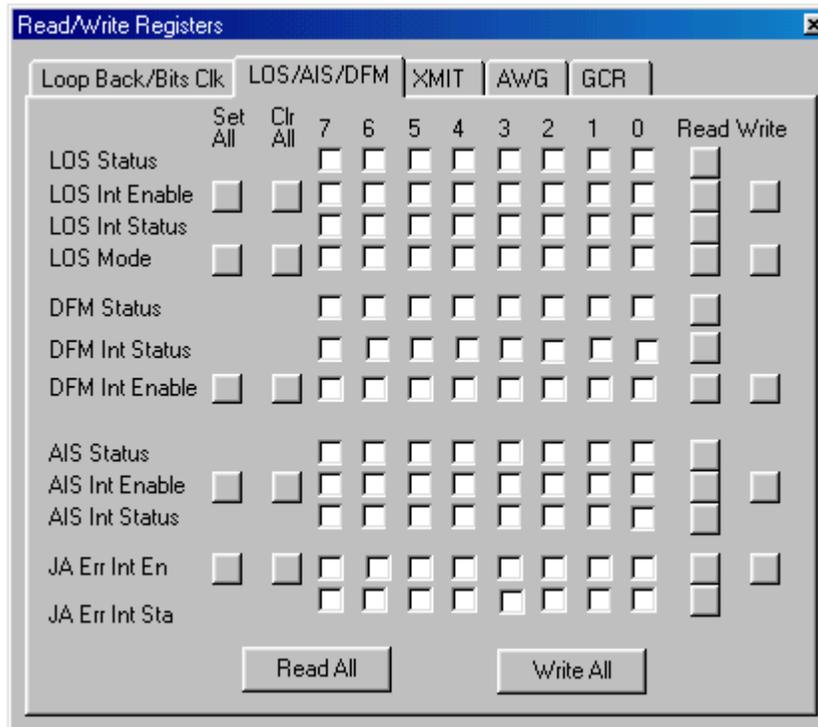
Figure 21. LOS/AIS/DFM/JA ERR Status/Enable Selection Screen

5.5 Transmitter Register Screen

The Transmitter Register screen shown in Figure 22 consists of the following registers:

- Automatic TAOS
- TAOS Enable
- Performance Monitor

- Line Length Channel ID
- Line Length Data
- Output Disable.

NOTE: Some indictor boxes (bits) in the Performance Monitor, Line Length Channel ID, and Line Length Data registers are grayed out, this means that these bits can not be accessed.
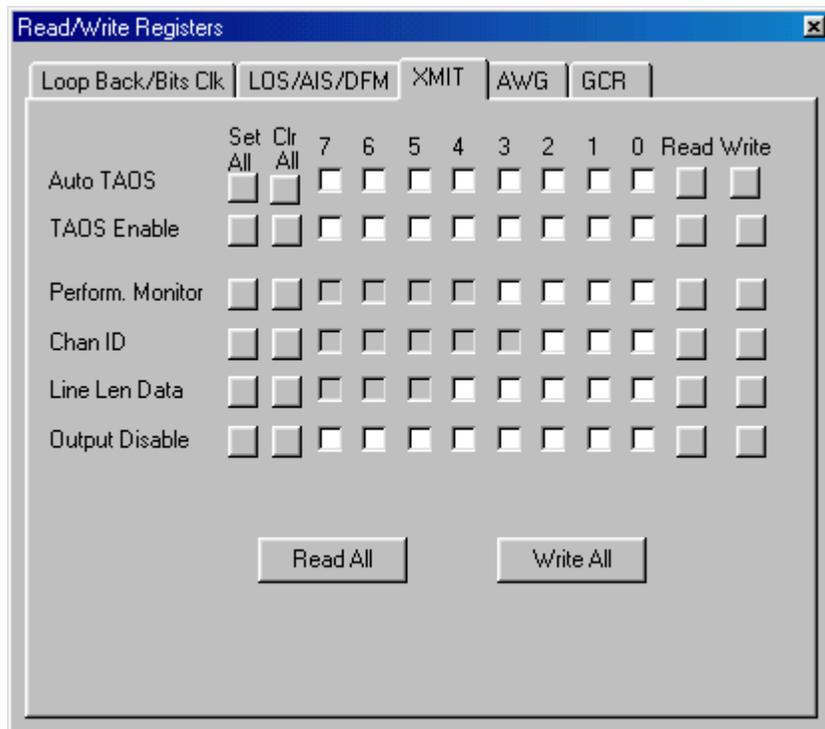
Figure 22. Transmitter Register Screen

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5.6 AWG Register Screen

The AWG Register screen shown in Figure 23 allows access to the following AWG registers:

- AWG Broadcast
- AWG Enable
- AWG Overflow Interrupt Enable
- AWG Overflow Interrupt Status
- AWG Phase Address
- AWG Phase Data.

The AWG Phase Address Register is broken up into two easy-to-use data input boxes: the **Chan Address** (i.e., channel address) and the **Sample Address**. For example, to access the AWG function for channel 5, write 05 into the **Chan Address** input box. This is the same for every channel. The **Chan Address**, **Sample Address**, and **Phase Data** input boxes use the values discussed in the AWG section of the *CS61880 Data Sheet*.
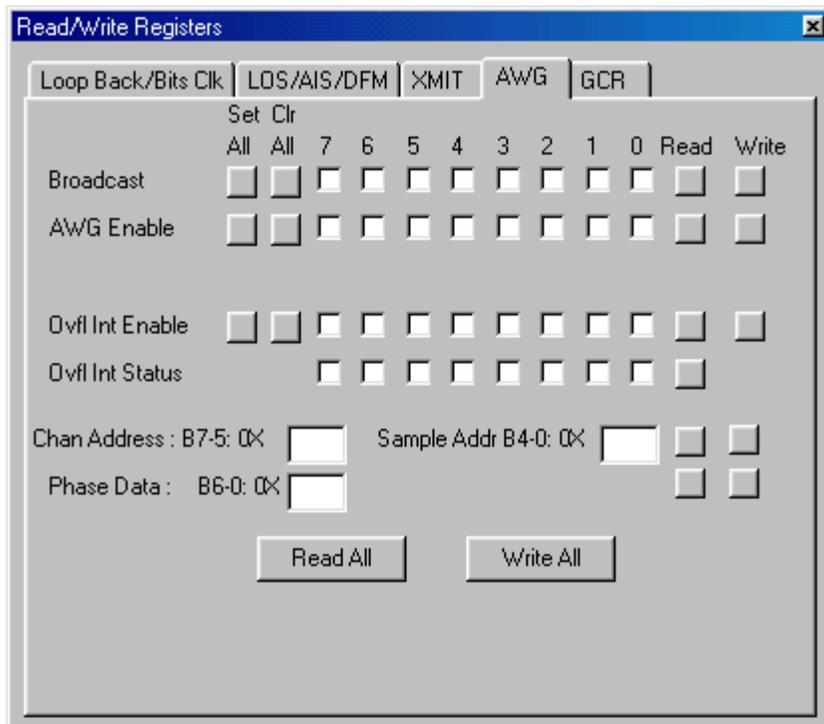
Figure 23. AWG Registers Screen

16   DS450DB1

5.7 Global Control Register Screen

Figure 24 shows the Global Control Register (GCR) screen, The GCR register screen consists of the following registers:

- Software reset
- ID registers.

Each bit in the Global Control Register can be access by writing directly to the bit in the Global Control Register on the top of this screen or by changing the radio buttons in one of the following windows:

- Jitter Attenuator
- JA FIFO Length
- AWG Auto Increment
- Raisen
- Coden
- Jitter Corner Freq.

The variables listed above change the corresponding bit in the Global Control Register. The Software Reset Register is a write only register and will clear after the write. The ID Register is a read only register.

Figure 24. Global Control Screen

6. BOARD CONFIGURATIONS

6.1 E1 75 Ω Mode Setup

Table 4 shows the position of the different switches and jumpers used to set up the CDB61880 evalua-tion board to operate in E1 75 Ω Hardware, Serial Host and Parallel Host operational modes. Before selecting Host mode, the switches in Table 4 in bold should be set to the position stated.

Table 4. E1 75 Ω Operational Mode Switch/Jumper Position

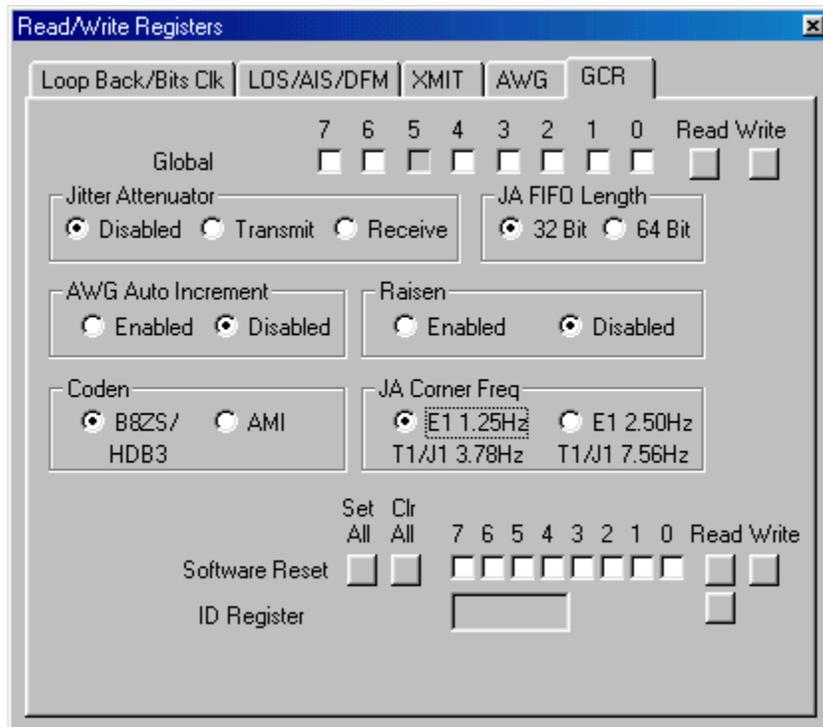| Switches/Jumpers	Hardware	Serial Host (Note 3)	Parallel Host (Note 3)
S15 (MODE)	HARDWARE	SERIAL HOST	PARALLEL HOST
S1 (0)	LOOP FUNCTION	**NONE**	**NONE**
S2 (1)	LOOP FUNCTION	**NONE**	**NONE**
S3 (2)	LOOP FUNCTION	**NONE**	**NONE**
S4 (3)	LOOP FUNCTION	**NONE**	**NONE**
S5 (4)	LOOP FUNCTION	**NONE**	**NONE**
S6 (5)	LOOP FUNCTION	**NONE**	**NONE**
S7 (6)	LOOP FUNCTION	**NONE**	**NONE**
S8 (7)	LOOP FUNCTION	**NONE**	**NONE**
S9 #1 (MOT_\INTL)	HIGH	**HIGH**	MOTOROLA/INTEL
S9 #2 (MUX)	LOW (Note 4)	**HIGH**	MUX/NON-MUX
S9 #3 (A4)	LOW (Note 5)	**HIGH**	**HIGH**
S9 #4 (A3)	LOW (Note 5)	**HIGH**	**HIGH**
S9 #5 (A2)	LOW (Note 5)	**HIGH**	**HIGH**
S9 #6 (A1)	LOW (Note 5)	**HIGH**	**HIGH**
S9 #7 (A0)	LOW (Note 5)	**HIGH**	**HIGH**
S10 (JASEL)	ANY POSITION	**OPEN**	**OPEN**
S11 (CBLSEL)	HIGH (Note 6)	**NC**	**NC**
J13 (VLOGIC)	3 V	3 V	3 V
J1 (MCLK)	OSCILLATOR	OSCILLATOR	OSCILLATOR
J93 (CLKE)	OPEN	OPEN	OPEN
J23 (TXOE)	OPEN	OPEN	OPEN

3. Connect a standard 25-pin male to female parallel port cable to connector J12 and the control PC.

4. Set "HIGH" to enable BITS Clock Recovery function for only Channel #0 in Hardware Mode.

5. Other settings may be used to enter G.772 Non-Intrusive Monitoring in Hardware Mode. Refer to the *CS61880 Data Sheet* for other settings.

6. Set "LOW" to disable receiver Internal line impedance matching function. The external resistors for all eight receivers must be changed to 9.31 Ω to properly match the input line impedance.

6.2 E1 120 Ω Mode Setup

Table 5 shows the position of the different switches and jumpers used to set up the CDB61880 evaluation board to operate in E1 120 Ω Hardware, Serial Host and Parallel Host operational modes. Before selecting Host mode, the switches in Table 5 in bold should be set to the position stated.

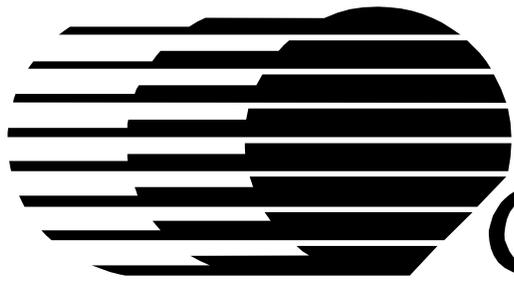**Table 5. E1 120 Ω Operational Mode Switch/Jumper Position**

Switches/Jumpers	Hardware	Serial Host (Note 3)	Parallel Host (Note 3)
S15 (MODE)	HARDWARE	SERIAL HOST	PARALLEL HOST
S1 (0)	LOOP FUNCTION	**NONE**	**NONE**
S2 (1)	LOOP FUNCTION	**NONE**	**NONE**
S3 (2)	LOOP FUNCTION	**NONE**	**NONE**
S4 (3)	LOOP FUNCTION	**NONE**	**NONE**
S5 (4)	LOOP FUNCTION	**NONE**	**NONE**
S6 (5)	LOOP FUNCTION	**NONE**	**NONE**
S7 (6)	LOOP FUNCTION	**NONE**	**NONE**
S8 (7)	LOOP FUNCTION	**NONE**	**NONE**
S9 #1 (MOT_\INTL)	HIGH	**OPEN**	MOTOROLA/INTEL
S9 #2 (MUX)	LOW (Note 4)	**OPEN**	MUX/NON-MUX
S9 #3 (A4)	LOW (Note 5)	**OPEN**	**OPEN**
S9 #4 (A3)	LOW (Note 5)	**OPEN**	**OPEN**
S9 #5 (A2)	LOW (Note 5)	**OPEN**	**OPEN**
S9 #6 (A1)	LOW (Note 5)	**OPEN**	**OPEN**
S9 #7 (A0)	LOW (Note 5)	**OPEN**	**OPEN**
S10 (JASEL)	ANY POSITION	**OPEN**	**OPEN**
S11 (CBLSEL)	NC (Note 7)	**NC**	**NC**
J13 (VLOGIC)	3 V	3 V	3 V
J1 (MCLK)	OSCILLATOR	OSCILLATOR	OSCILLATOR
J93 (CLKE)	OPEN	OPEN	OPEN
J23 (TXOE)	OPEN	OPEN	OPEN

7. Set to "NC" to disable receiver Internal line impedance matching function. The external resistors for all eight receivers must be changed to 15 Ω to properly match the input line impedance.

7. EVALUATION HINTS

- Pin #1 of the socket is indicated by an arrow with U1 below it.
- A short in the desired position must be placed on Jumper J13 to connect the CS61880 to one of the power supply binding post. LED D3 will illuminate when jumper J13 is connected to a power supply.
- Before selecting any Host mode place the CBLSEL, LOOP, ADDRESS and JASEL switches in the open or none position.
- When using the CS61880 device in Internal Match Impedance mode, be sure that the 1 KΩ resistors are not in series with the receivers.

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• Notes •

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