AK7707
Multi Core DSP with SRC

1. General Description

The AK7707 is a highly integrated digital signal processor, including 6 stereo sampling rate convertors supporting sampling frequency up to 192kHz, a DIR, a DIT and two types of DSPs for Audio and Voice processing. The DSP1 supports a 295MHz core and is optimized for C-language support. DSP2 and DSP3 have 4608 step/fs (when fs=48kHz) processing power. The AK7707 is able to process multiple sample rates simultaneously. This function is ideal for full bandwidth audio and voice processing, such as hands-free function along with audio. This simultaneous processing is enabled because the two types of DSPs can work on different but synchronized sampling frequencies. The AK7707 is a RAM based DSP, so it can be freely programmed for user requirements, such as acoustic effects and proprietary high performance hands-free function. The AK7707 is available in a space saving 64-pin HTQFP package.

2. Features

☐ DSP1(Tensilica Hifi2):
- Word Length: 64-bit
- Operation Clock: 294.912MHz (DSP1 Fast Mode)
- IRAM: 128KB
- DRAM: 384KB
- GPIO: 8 ports
- SPI Control Master Port x 1
- JTAG for On-chip Debugging
- Independent Power Management

☐ DSP2, 3(AKM DSP)
- Word Length: 28-bit (Data RAM: Simple floating point)
- Operation Clock 221.184MHz (4608steps, fs= 48kHz, DSP2/3 Fast Mode)
- Multiplier: 24 x 24 → 48-bit (Double precision arithmetic available)
- Divider: 24 / 24 → 24-bit (Floating point normalization function)
- ALU: 52-bit Arithmetic Operation (with overflow margin 4-bit)
- Program RAM (PRAM): 10kword x 36-bit (DSP2+DSP3 Total)
- Coefficient RAM (CRAM): 10kword x 24-bit (DSP2+DSP3 Total)
- Data RAM (DRAM): 10kword x 28-bit (DSP2+DSP3 Total)
- Delay RAM(DLRAM): 24kword x 28-bit (DSP2+DSP3 Total)
- JX pins (Interrupt)
- Independent Power Management Function

☐ SRC
- 2ch x 6
- FSI = 8kHz ~ 192kHz, FSO= 8kHz ~ 192kHz (FSO/FSI= 0.167 ~ 6.0)

- ☐ DIR
  - S/PDIF, IEC60958, AES/EBU, EIAJ CP1201
  - Amplifier: 2 Inputs Selector
  - De-emphasis Filter (32, 44.1, 48, 96kHz, ON/OFF function)
  - Non-PCM Data Stream Detection Function
  - DTS-CD Data Stream Detection Function
  - Sampling Frequency Detection Function (32kHz, 44.1kHz, 48kHz, 88.2kHz 96kHz)
  - Unlock & Parity Error Detection Function
  - Validity Detection Register Read back Function
  - 42-bit Channel Status Buffer
  - Q-sub code Buffer for CD bit stream
- ☐ DIT
  - S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible
  - 24-bit Stereo Output
- ☐ Digital Interfaces
  - Digital Input 8-Port (Max. 64ch, TDM mode)
  - Digital Output 8-Port (Max. 64ch, TDM mode)
  - Independent LRCK/BICK In/Output Port x 5 Lines
  - Data Format: MSB 32, 24-bit/ LSB24, 20, 16-bit/ I^2S
  - Shot/ Long Frame
  - TDM In/Output Mode
  - Digital Microphone Input Ports (2ch x 2 Lines)
- ☐ Digital Mixer Circuit
- ☐ PLL Circuit
- ☐ µP Interface: SPI (7MHz Max.) / I^2C (1MHz Fast Mode plus)
- ☐ Power Supply:

  Digital: VDD12: 1.14V ~ 1.3V (Typ. 1.2V)

  I/F: VDD33: 3.13V ~ 3.47V (Typ. 3.3V)

  TVDD1: 1.7V ~ 3.47V (Typ. 3.3V)

  TVDD2: 1.7V ~ 3.47V (Typ. 3.3V)

  AVDD: 3.13V ~ 3.47V (Typ. 3.3V)
- ☐ Operation Temperature Range: Ta= -40 ~ 85ºC
- ☐ Package: 64-pin HTQFP (10mm x 10mm, 0.5mm pitch)

3. Table of Contents

4. Block Diagram and Functions

■ Device Block Diagram

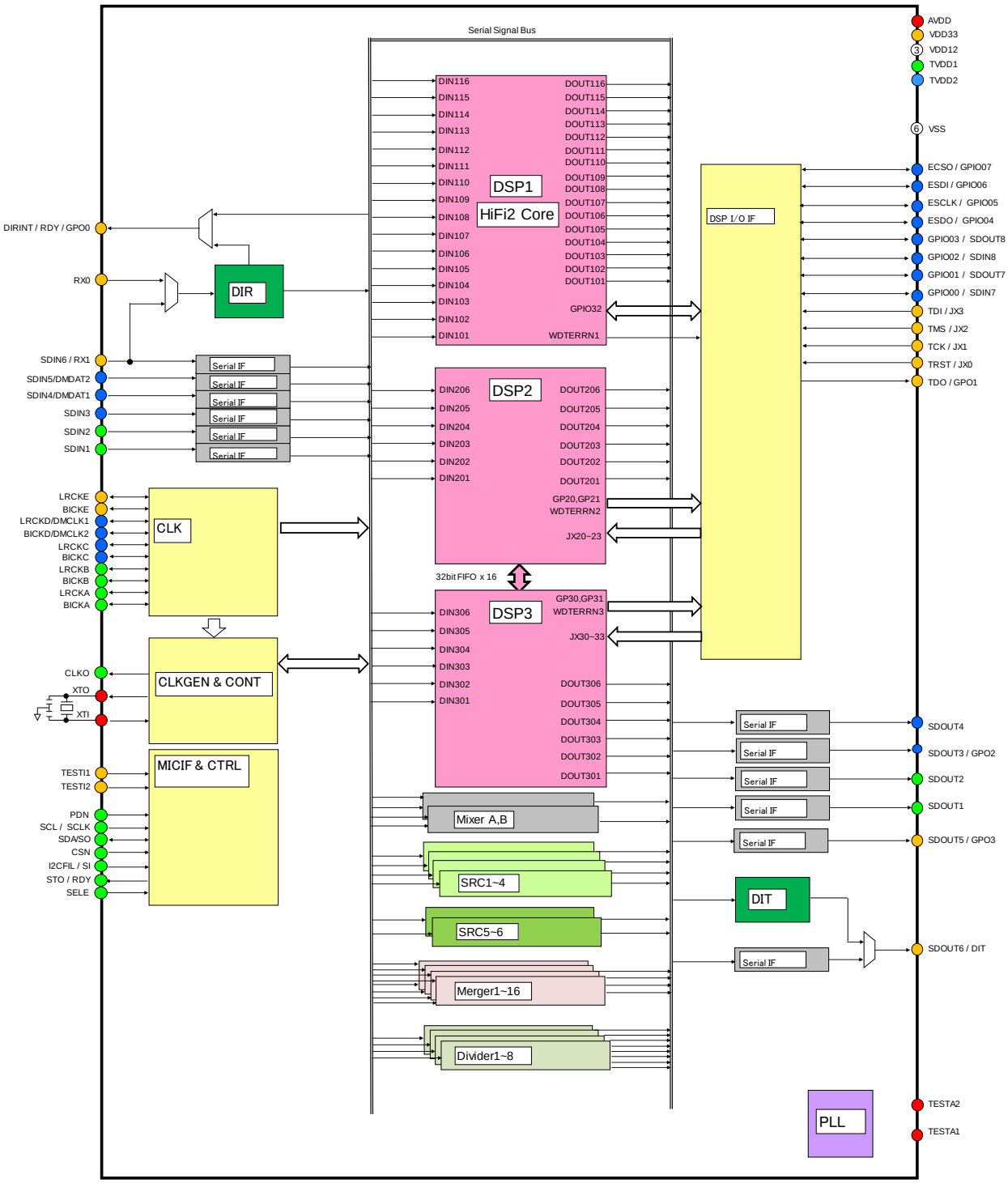


Figure 1. AK7707 Device Block Diagram

■ DSP1 Block Diagram

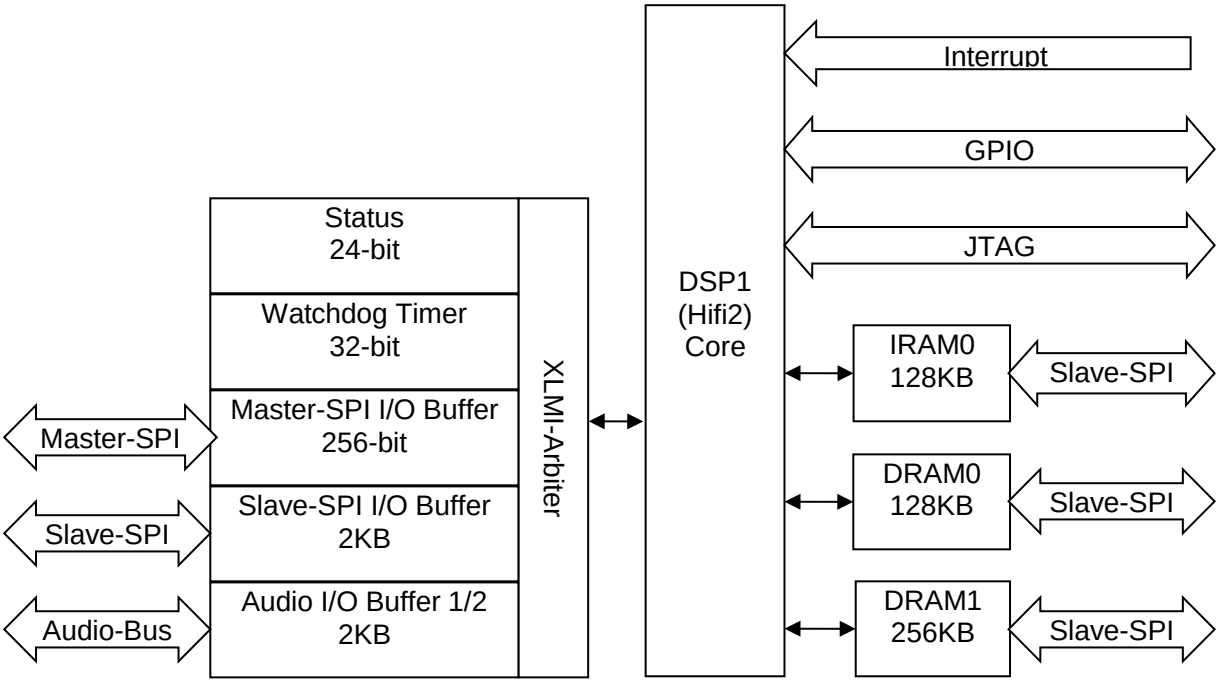


Figure 2. DSP1 Block Diagram

■ DSP2 Block Diagram

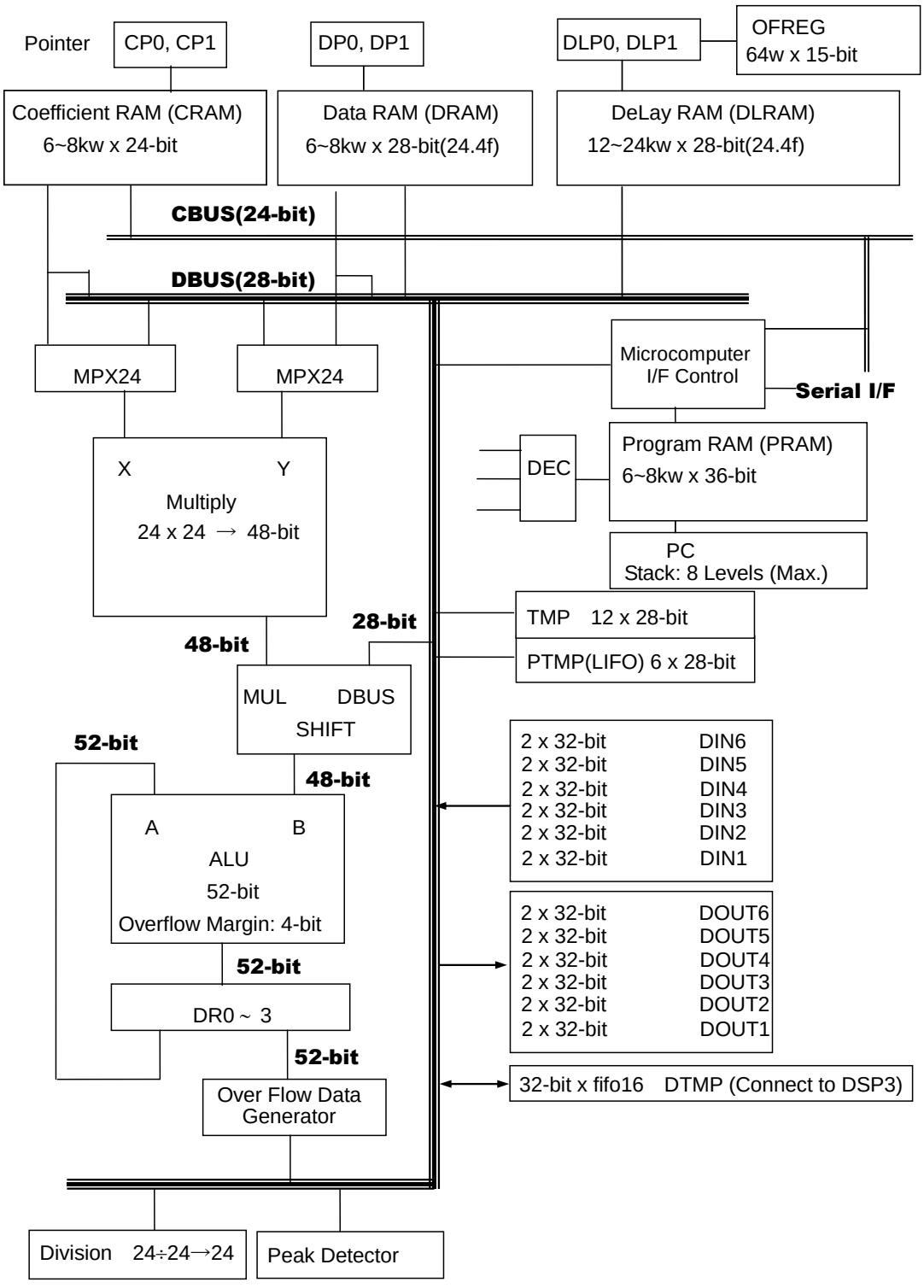


Figure 3. DSP2 Block Diagram

■ DSP3 Block Diagram

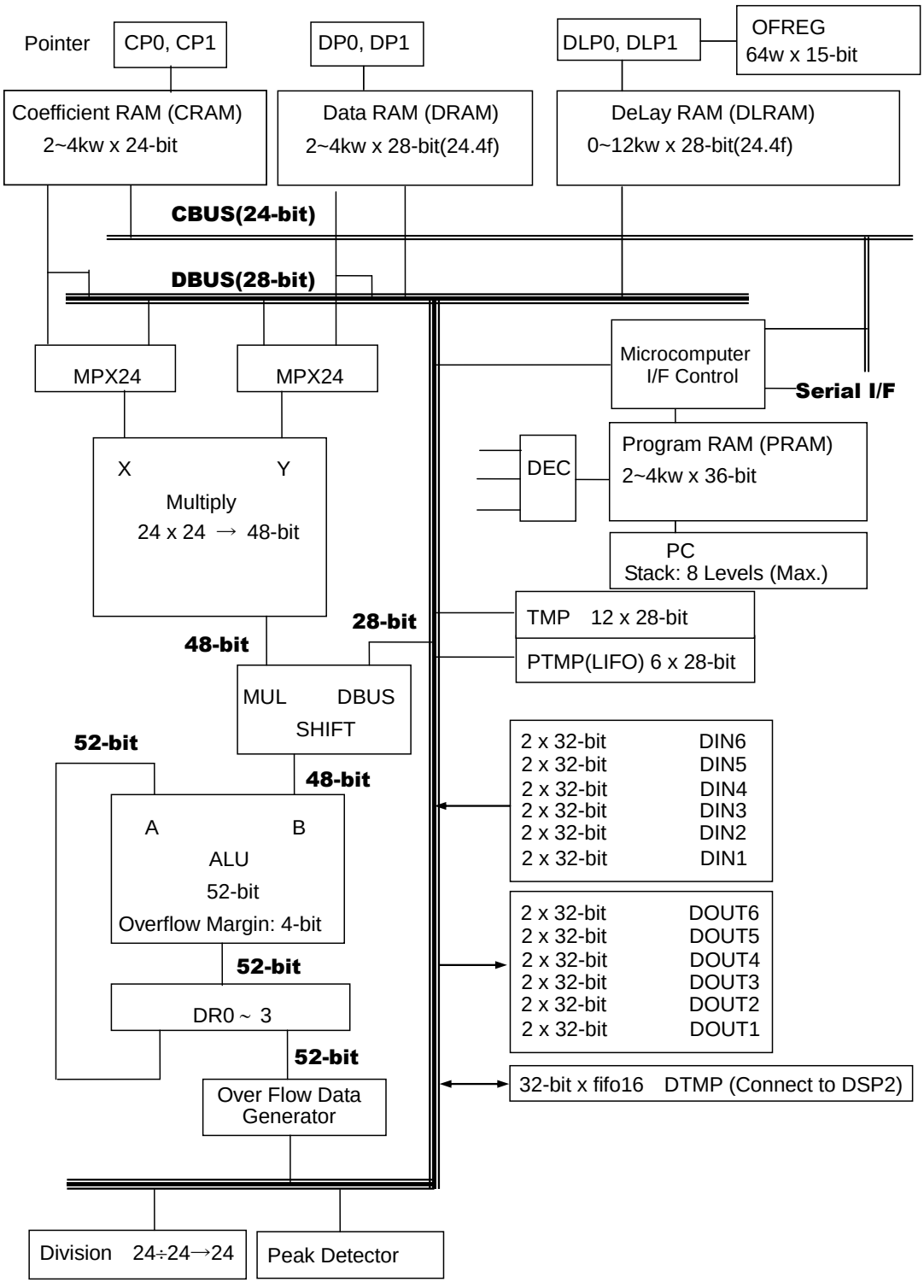
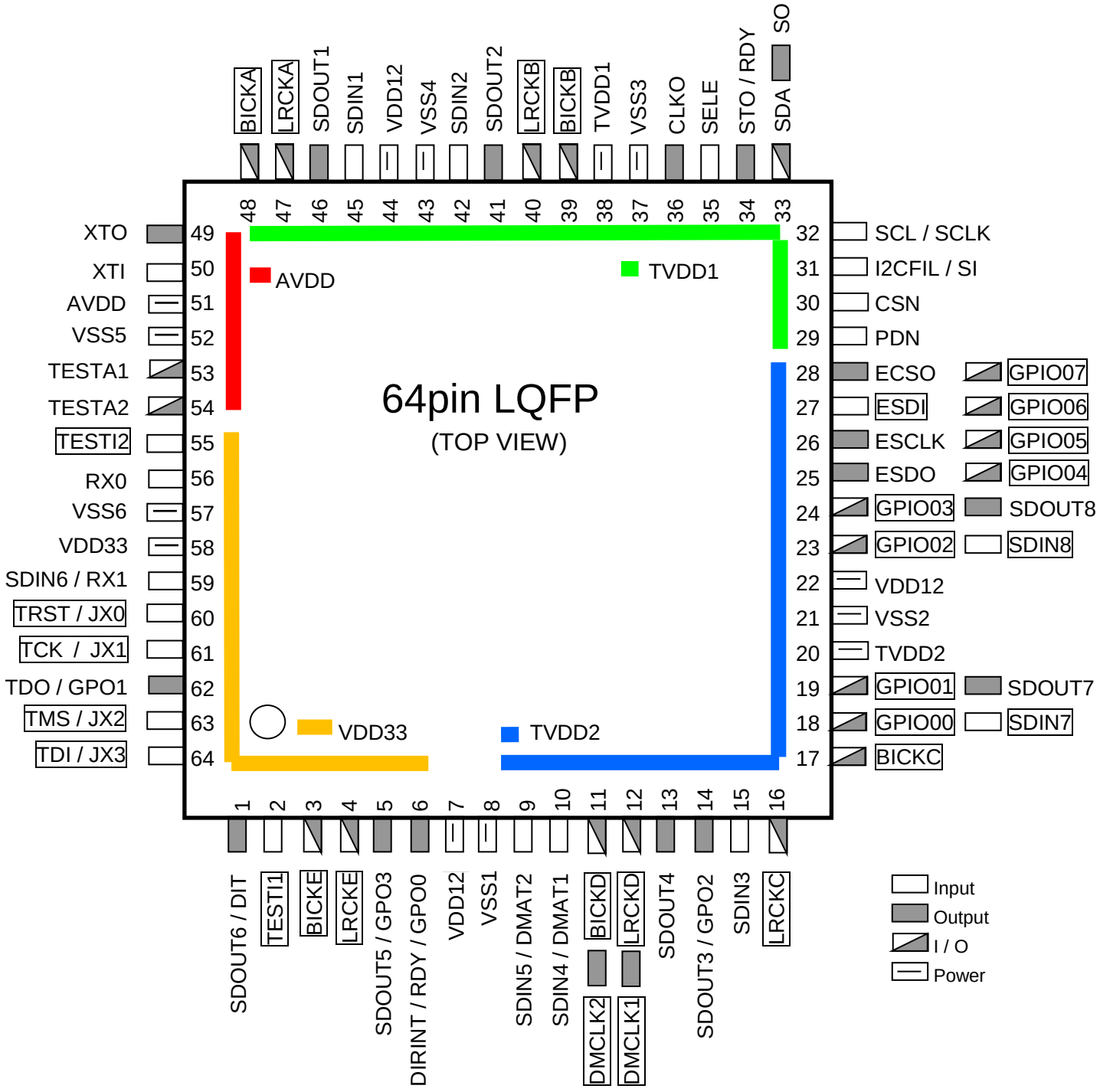


Figure 4. DSP3 Block Diagram

5. Pin Configurations and Functions

■ Pin Layout



*** Framed pin names indicate that they are pull-down pins

Preceded pin names are default pins.
(Default Example: 1-pin SDOUT6, 32-pin SCL, 33-pin SDA and 64-pin TDI)

■ **Pin Functions**

No.	Pin Name	I/O	Function	Supply
1	SDOUT6	O	Serial Data Output 6	VDD33
	DIT	O	DIT Output	
2	TESTI1	I	Test Input (Pulled-down) Connect this pin to "L"	VDD33
3	BICKE	I/O	Serial Bit Clock E (Input Pulled-down)	VDD33
4	LRCKE	I/O	LR Channel Select Clock E (Input Pulled-down)	VDD33
5	SDOUT5	O	Serial Data Output 5	VDD33
	GPO3	O	General Output 3 (DSP3-GP1)	
6	DIRINT	O	DIR Interrupt Output	VDD33
	RDY	O	RDY Pin	
	GPO0	O	General Output 0 (DSP2-GP0)	
7	VDD12	-	Digital Power Supply Typ. 1.2V (1.14V ~ 1.3V)	-
8	VSS1	-	Ground 1 0V	-
9	SDIN5	I	Serial Data Input 5	TVDD2
	DMDAT2	I	DATA2 Pin for Digital Microphone	
10	SDIN4	I	Serial Data Input 4	TVDD2
	DMDAT1	I	DATA1 Pin for Digital Microphone	
11	BICKD	I/O	Serial Bit Clock D (Input Pulled-down)	TVDD2
	DMCLK2	O	Clock Output 2 for Digital Microphone	
12	LRCKD	I/O	LR Channel Select Clock D (Input Pulled-down)	TVDD2
	DMCLK1	O	Clock Output 1 for Digital Microphone	
13	SDOUT4	O	Serial Data Output 4	TVDD2
14	SDOUT3	O	Serial Data Output 3	TVDD2
	GPO2	O	General Output 2 (DSP3-GP0)	
15	SDIN3	I	Serial Data Input 3	TVDD2
16	LRCKC	I/O	LR Channel Select Clock C (Input Pulled-down)	TVDD2
17	BICKC	I/O	Serial Bit Clock C (Input Pulled-down)	TVDD2
18	GPIO00	I/O	DSP1 GPIO Pin Controlled by DSP1 program. (Input Pulled-down)	TVDD2
	SDIN7	I	Serial Data Input 7	
19	GPIO01	I/O	DSP1 GPIO Pin Controlled by DSP1 program. (Input Pulled-down)	TVDD2
	SDOUT7	O	Serial Data Output 7	
20	TVDD2	-	Digital Power Supply 2 Typ. 3.3V (1.7V ~ 3.47V)	-
21	VSS2	-	Ground 2 0V	-
22	VDD12	-	Digital Power Supply 12 Pin Typ. 1.2V (1.14V ~ 1.3V)	-
23	GPIO02	I/O	DSP1 GPIO2 Pin Controlled by DSP1 program. (Input Pulled-down)	TVDD2
	SDIN8	I	Serial Data Input 8 (Pulled-down)	
24	GPIO03	I/O	DSP1 GPIO Pin Controlled by DSP1 program. (Input Pulled-down)	TVDD2
	SDOUT8	O	Serial Data Output 8	
25	ESDO	O	SPI Control Data Output for External Devices (Connect to the SI pin of External Device) (Pulled-down)	TVDD2
	GPIO04	I/O	DSP1 GPIO4 Pin Controlled by DSP1 program. (Pulled-down)	

No.	Pin Name	I/O	Function	Supply
26	ESCLK	O	SPI Control Data Output for External Devices (Connect to the SCLK pin of External Device)	TVDD2
	GPIO05	I/O	DSP1 GPIO5 Pin Controlled by DSP1 program. (Input Pulled-down)	
27	ESDI	I	SPI Control Data Input for External Devices (Connect to the SO pin of External Device) (Pulled-down)	TVDD2
	GPIO06	I/O	DSP1 GPIO6 Pin Controlled by DSP1 program. (Input Pulled-down)	
28	ECSO	O	SPI Control Data Output for External Devices (Connect to the CS pin of External Device)	TVDD2
	GPIO07	I/O	DSP1 GPIO7 Pin Controlled by DSP1 program. (Input Pulled-down)	
29	PDN	I	Power Down N Pin • Use this pin to power down the AK7707. • Set this pin to “L” when power up the AK7707.	TVDD1
30	CSN	I	I^2C Mode: Bus Address Pin for I^2C Interface • This pin must be pulled up or pulled down. • Inverted polarity is used as bus address.	TVDD1
		I	SPI Mode: Chip Select N Pin for SPI Interface • Put this pin to “H” in power-down state or when not interfacing to a microcontroller.	
31	I2CFIL	I	I^2C Interface Mode Select Input • I2CFIL = “L” Fixed: Fast Mode (400kHz) • I2CFIL = “H” Fixed: Fast Mode Plus (1MHz) (fixed to TVDD1)	TVDD1
	SI	I	Serial Data Input for SPI Interface	
32	SCL	I	Serial Data Clock Input for I^2C Interface	TVDD1
	SCLK	I	Serial Data Clock Input for SPI Interface	
33	SDA	I/O	SDA Pin for I^2C Interface	TVDD1
	SO	O	Serial Data Output for SPI Interface	
34	STO	O	Status Output	TVDD1
	RDY	O	RDY Pin	
35	SELE	I	Self-Boot Enable	TVDD1
36	CLKO	O	Clock Output	TVDD1
37	VSS3	-	Ground 3 Pin 0V	-
38	TVDD1	-	Digital IO Power Supply 1 Typ. 3.3V (1.7V ~ 3.47V)	-
39	BICKB	I/O	Serial Bit Clock B (Input Pulled-down)	TVDD1
40	LRCKB	I/O	LR Channel Select Clock B (Input Pulled-down)	TVDD1
41	SDOUT2	O	Serial Data Output 2	TVDD1
42	SDIN2	I	Serial Data Input 2	TVDD1
43	VSS4	-	Ground 4 0V	-
44	VDD12	-	Digital Power Supply 12 Typ. 1.2V (1.14V ~ 1.3V)	-
45	SDIN1	I	Serial Data Input 1	TVDD1
46	SDOUT1	O	Serial Data Output 1	TVDD1
47	LRCKA	I/O	LR Channel Select Clock A (Input Pulled-down)	TVDD1
48	BICKA	I/O	Serial Bit Clock A (Input Pulled-down)	TVDD1

No.	Pin Name	I/O	Function	Supply
49	XTO	O	Oscillation Circuit Output • When using crystal oscillator, the XTI and the XTO pins should be connected to a crystal oscillator. • When not using crystal oscillator, this pin should be open.	AVDD
50	XTI	I	Oscillation Circuit Input • When using crystal oscillator, the XTI and the XTO pins should be connected to a crystal oscillator. • When not using crystal oscillator, this pin should be connected to external clock or VSS5.	AVDD
51	AVDD	-	Analog Power Supply Typ. 3.3V (3.13V ~ 3.47V)	-
52	VSS5	-	Ground 5 0V	-
53	TESTA1	I/O	Test In/Output (This pin must be open)	AVDD
54	TESTA2	I/O	Test In/Output (This pin must be open)	AVDD
55	TESTI2	I	Test Input 2 (Pulled-down) Connect this pin to VSS6.	VDD33
56	RX0	I	DIR Data Input 0	VDD33
57	VSS6	-	Ground 6 0V	-
58	VDD33	-	Digital Power Supply 33 Typ. 3.3V (3.13V ~ 3.47V)	-
59	SDIN6	I	Serial Data Input 6	VDD33
	RX1	I	DIR Data Input 1	
60	TRST	I	JTAG Input	VDD33
	JX0	I	JX Input 0 (DSP2/3-JX0)	
61	TCK	I	JTAG Input	VDD33
	JX1	I	JX Input 1 (DSP2/3-JX1)	
62	TDO	O	JTAG Out	VDD33
	GPO1	O	General Output 1 (DSP2-GP1)	
63	TMS	I	JTAG Input	VDD33
	JX2	I	JX Input 2 (DSP2/3-JX2)	
64	TDI	I	JTAG Input	VDD33
	JX3	I	JX Input 3 (DSP2/3-JX3)	

* The exposed pad on the bottom surface of the package must be connected to the ground to reduce the need for heat-sinking.

■ Handling the Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name (Pin No.)	Setting
Digital	SDOUT6/DIT(1), SDOUT5/GPO3(5), DIRINT/RDY/GPO0(6), SDOUT4(13), SDOUT3/GPO2(14), ESDO/GPIO04(25),ESCLK/GPIO05(26), ECSO/GPIO07(28),SO/SDA(33), STO/RDY(34), CLKO(36), SDOUT2(41), SDOUT1(46), TDO/GPO1(62)	Open
	BICKE(3), LRCKE(4), SDIN5/DMDAT2(9), SDIN4/DMDAT1(10), BICKD/DMCLK2(11), LRCKD/DMCLK1(12), SDIN3(15), LRCKC(16), BICKC(17), GPIO00/SDIN7(18), GPIO01/SDOUT7(19), GPIO02/SDIN8(23), GPIO03/SDOUT8(24), ESDI/GPIO06(27), CSN(30), I2CFIL/SI(31), SCL/SCLK(32), SELE(35), BICKB(39), LRCKB(40), SDIN2(42), SDIN1(45), LRCKA(47), BICKA(48), TESTI1(55), RX0(56), TESTI2(57), SDIN6/RX1(59), TRST/JX0(60), TCK/JX1(61), TMS/JX2(63), TDI/JX3(64),	Connect to VSS1~4, 6
Analog	XTO(49), TESTA1(53),TESTA2(54)	Open
	XTI(50)	Connect to VSS5

Table 1. Handling of Unused Pins

■ Relationship between Digital Power Supply and Input/Output Pins

Power Supply	Input/output Pins
TVDD1 (1.7~3.3V)	BICKA(48), LRCKA(47), SDOUT1(46), SDIN1(45), SDIN2(42), SDOUT2(41), LRCKB(40), BICKB(39), CLKO(36), SELE(35),STO/RDY(34), SDA/SO(33), SCL/SCLK(32), I2CFIL/SI(31), CSN(30), PDN(29)
TVDD2 (1.7~3.3V)	SDIN5/DMDAT2(9),SDIN4/DMDAT1(10),BICKD/DMCLK2(11),LRCKD/DMCLK1(12), SDOUT4(13),SDOUT3/GPO2(14),SDIN3(15),LRCKC(16),BICKC(17), GPIO00/SDIN7(18),GPIO01/SDOUT7(19),GPIO02/SDIN8(23),GPIO03/SDOUT8(24), ESDO/GPIO04(25), ESCLK/GPIO05(26), ESDI/GPIO06(27), ECSO/GPIO07(28)
VDD33 (3.3V)	TESTI2(55), RX0(56) , SDIN6/RX1(59), TRST/JX0(60), TCK/JX1(61), TDO/GPO1(62), TMS/JX2(63) , TDI/JX3(64) , SDOUT6/DIT(1) , TESTI1(2), BICKE(3) , LRCKE(4), SDOUT5/GPO3(5),DIRINT/GPO0(6)
AVDD (3.3V)	XTO(49), XTI(50), TESTA1(53), TESTA2(54)

Table 2. Relationship between Digital Power Supply and Input/output Pins

■ Power-down Pin Status

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
1	SDOUT6	O	“L” Output	32	SCL	I	Input
2	TESTI1	I	Input (Pulled-down)	33	SDA	I/O	Input
3	BICKE	I/O	Input(Pulled-down)	34	STO	O	“L” Output
4	LRCKE	I/O	Input (Pulled-down)	35	SELE	I	Input
5	SDOUT5	O	“L” Output	36	CLKO	O	Output
6	DIRINT	O	“L” Output	39	BICLKB	I/O	Input (Pulled-down)
9	SDIN5	I	Input	40	LRCKB	I/O	Input (Pulled-down)
10	SDIN4	I	Input	41	SDOUT2	O	“L” Output
11	BICKD	I/O	Input (Pulled-down)	42	SDIN2	I	Input
12	LRCKD	I/O	Input (Pulled-down)	45	SDIN1	I	Input
13	SDOUT4	O	“L” Output	46	SDOUT1	O	“L” Output
14	SDOUT3	O	“L Output	47	LRCKA	I/O	Input (Pulled-down)
15	SDIN3	I	Input	48	BICKA	I/O	Input (Pulled-down)
16	LRCKC	I/O	Input (Pulled-down)	49	XTO	O	SELE= “L”: “H” Output SELE= “H”: Inverted Output of XTI
17	BICKC	I/O	Input (Pulled-down)	50	XTI	I	Input
18	GPIO00	I/O	Input (Pulled-down)	53	TESTA1	I/O	“Hi-Z” Output
19	GPIO01	I/O	Input (Pulled-down)	54	TESTA2	I/O	“Hi-Z” Output
23	GPIO02	I/O	Input (Pulled-down)	55	TESTI2	I	Input (Pulled-down)
24	GPIO03	I/O	Input (Pulled-down)	56	RX0	I	Input
25	ESDO	I/O	“L” Output (Pulled-down)	59	SDIN6	I	Input
26	ESCLK	I/O	“L” Output (Pulled-down)	60	TRST	I	Input (Pulled-down)
27	ESDI	I/O	Input (Pulled-down)	61	TCK	I	Input (Pulled-down)
28	ECSO	I/O	“H” Output	62	TDO	O	“L” Output
29	PDN	I	“L” Input	63	TMS	I	Input (Pulled-down)
30	CSN	I	Input	64	TDI	I	Input (Pulled-down)
31	I2CFIL	I	Input				

Table 3. Power-down Pin Status (just after Power-up)

6. Absolute Maximum Ratings

(VSS1~6 = 0V;* 1)

Parameter	Symbol	Min.	Max.	Unit
Power Supply				
Analog	AVDD	-0.3	3.9	V
Digital1(Core)	VDD12	-0.3	1.4	V
Digital2(I/F)	TVDD1	-0.3	3.9	V
Digital3(I/F)	TVDD2	-0.3	3.9	V
Digital4(I/F)	VDD33	-0.3	3.9	V
Difference (VSS1 ~ VSS6) (* 1)	ΔGND	-0.3	0.3	V
Input Current (Except power pins)	IIN	-	±10	mA
Analog Input Voltage (* 2)	VINA	-0.3	(AVDD+0.3) or 3.9	V
Digital Input Voltage (* 3)	VIND1	-0.3	(TVDD1+0.3) or 3.9	V
Digital Input Voltage (* 4)	VIND2	-0.3	(TVDD2+0.3) or 3.9	V
Digital Input Voltage (* 5)	VIND3	-0.3	(VDD33+0.3) or 3.9	V
Ambient Temperature	Ta	-40	85	ºC
Storage Temperature	Tstg	-65	150	ºC

Notes:

* 1. All voltages are with respect to ground. VSS1 ~ VSS6 must be connected to the same ground.
* 2. The maximum analog input voltage of the XTI pin is the smaller value between (AVDD+0.3)V and 3.9V.
* 3. The maximum digital input voltage of SDIN1, SDIN2, LRCKA, BICKA, LRCKB, BICKB, SELE, SO/SDA, CSN, SI/I2CFIL, SCLK/SCL and PDN pins is the smaller value between (TVDD1+0.3)V and 3.9V.
* 4. The maximum digital input voltage of SDIN3, SDIN4/DMDAT1,SDIN5/DMDAT2, LRCKD/DMCLK2, BICKD/DMCLK1, GPIO00/SDIN7, GPIO01/SDOUT7, GPIO02/SDIN8, GPIO03/SDOUT8, ESDO/GPIO04, ESCLK/GPIO05, ESDI/GPIO06, ECSO/GPIO07, LRCKC and BICKC pins is the smaller value between (TVDD2+0.3)V or 3.9V.
* 5. The maximum digital input voltage of SDIN6/RX1, RX0, TDI/JX3, TMS/JX2, TCK/JX1, TRST/JX0, LRCKE, BICKE, TESTI1 and TESTI2 pins is the smaller value between (VDD33+0.3)V or 3.9V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1~6 = 0V; * 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply					
Analog	AVDD	3.13	3.3	3.47	V
Digital (3.3V, I/F)	VDD33	3.13	3.3	3.47	V
Digital (1.2V Core)	VDD12	1.14	1.2	1.3	V
Digital (I/F)	TVDD1	1.7	3.3	3.47	V
Digital (I/F)	TVDD2	1.7	3.3	3.47	V

Notes:

* 6. TVDD2 must be supplied from the first regulator that is powered up.
* 7. All power supply pins must be connected to the power supply.
* 8. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
* 9. The power up sequence must be executed from the beginning when changing power supply level of the TVDD1 and TVDD2. (e.g. 1.8V → 3.3V)
* 10. Do not turn off the power supply of the AK7707 with the power supply of the surrounding device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD1 or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ SRC

(Ta= 25°C; VDD12= 1.2V, AVDD= VDD33= TVDD1= TVDD2= 3.3V; VSS1 ~ 6= 0V;
Signal Frequency= 1kHz; 24-bit Data; Measurement Frequency=20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				24	bit
	Input Sample Rate	FSI	8		192 (* 11)	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Audio Mode					
	FSO/FSI=192kHz/48kHz			-122		dB
	FSO/FSI=44.1kHz/48kHz			-125		dB
	FSO/FSI=48kHz/88.2kHz			-122		dB
	FSO/FSI=48kHz/96kHz			-133		dB
	FSO/FSI=44.1kHz/96kHz			-116		dB
	FSO/FSI=48kHz/192kHz			-133		dB
	FSO/FSI=8kHz/48kHz			-130		dB
	Voice Mode					
	FSO/FSI=24kHz/32kHz			-95		dB
	FSO/FSI=16kHz/24kHz			-98		dB
	FSO/FSI=24kHz/44.1kHz			-78		dB
	FSO/FSI=16kHz/44.1kHz			-69		dB
	FSO/FSI=8kHz/32kHz			-130		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Audio Mode					
	FSO/FSI=192kHz/48kHz			132		dB
	FSO/FSI=44.1kHz/48kHz			136		dB
	FSO/FSI=48kHz/88.2kHz			135		dB
	FSO/FSI=48kHz/96kHz			136		dB
	FSO/FSI=44.1kHz/96kHz			136		dB
	FSO/FSI=48kHz/192kHz			136		dB
	FSO/FSI=8kHz/48kHz			130		dB
	Voice Mode					
	FSO/FSI=24kHz/32kHz			132		dB
	FSO/FSI=16kHz/24kHz			135		dB
	FSO/FSI=24kHz/44.1kHz			132		dB
	FSO/FSI=16kHz/44.1kHz			128		dB
	FSO/FSI=8kHz/32kHz			130		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted) FSO/FSI=44.1kHz/48kHz			137		dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

Note:
* 11. Only two SRCs are available out of SRC1-4 when the operation frequency is 192kHz.

■ SPDIF Characteristics

(Ta = −40 ~ 85ºC, VDD33 = 3.13 ~ 3.47V)

Parameter	Symbol	Min	Typ.	Max.	Unit
RX0 input voltage level	VIH	100		VDD33	mV
(internally biased at VDD33 / 2)	VIL	-INVREF		-100	mV
Input Hysteresis	VTY		50		mV
Input Reference Voltage	INVREF		VDD33 / 2		V
Input Resistance	Zin		10		kΩ
Input Sampling Frequency	fs	8		96	kHz

■ Digital Micrephone Interface

(AVDD=3.0~3.6V, TVDD=1.7~3.6V, VDD12=1.14~1.3V, AVSS=DVSS=0V, Ta= -40°C~85°C; CL=100pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DMDAT1, DMDAT2					
Serial Data Input Latch Set Up Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK1, DMCLK2					
Colock Frequency (* 12)	fDMCK	0.5	64fs	6.2	MHz
Duty Ratio	dDMCK	40	50	60	%

Note:

* 12. Clock frequency is determined by the sampling frequency (fs) that is selected by SDDMIC1[2:0] bits/SDDMIN2[2:0] bits

■ Current Consumption

(Ta= 25ºC; AVDD=3.0~3.47V(Typ.=3.3V, Max.=3.47V); VDD33=3.0 ~ 3.47V (Typ.=3.3V, Max.=3.47V); VDD12=1.14 ~ 1.3V (Typ.=1.2V, Max.=1.3V); TVDD1=1.7 ~ 3.47V (Typ.=3.3V, Max.=3.47V); TVDD2=1.7 ~ 3.47V (Typ.=3.3V, Max.=3.47V); VSS1 ~ 6=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up (* 13) (PDN pin= “H”)	AVDD		8	15	mA
	VDD33		6	12	mA
	VDD12		220	650	mA
	TVDD1		17	24	mA
	TVDD2		12	18	mA
Power-Down (PDN pin= “L”)	AVDD		100		uA
	VDD33		10		uA
	VDD12		3		mA
	TVDD1		10		uA
	TVDD2		10		uA

Note:

* 13. The current consumption changes depending on the system frequency and function of DSP program.

9. Digital Filter Characteristics

■ SRC Block

Audio Mode

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V)

Parameter			Symbol	Min.	Typ.	Max	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533 ≤ FSO/FSI < 0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490 ≤ FSO/FSI < 0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450 ≤ FSO/FSI < 0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225 ≤ FSO/FSI < 0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.533 ≤ FSO/FSI < 0.909	SB	0.2974FSI			kHz
		0.490 ≤ FSO/FSI < 0.539	SB	0.2812FSI			kHz
		0.450 ≤ FSO/FSI < 0.495	SB	0.2604FSI			kHz
		0.225 ≤ FSO/FSI < 0.455	SB	0.1802FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI < 0.227	PR			±0.50	dB
Stopband Attenuation		0.450 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.167 ≤ FSO/FSI < 0.455	SA	85.0			dB
Group Delay (Ts=1/fs) (* 14)			GD		67 (55/FSI+12/FSO)		Ts

Notes:

* 14. Calculated delay time in the SRC block only. This time is measured from a rising edge of LRCK after a signal input to the SRC until a rising edge of LRCK before a data output when there is no phase difference between input and output.

Voice Mode

(Ta= -40 ~ 85ºC; VDD12=1.14 ~ 1.3V; AVDD=3.13 ~ 3.47V; VDD33=3.13 ~ 3.47V; TVDD1=1.7 ~ 3.47V; TVDD2=1.7 ~ 3.47V; VSS1 ~ 6= 0V)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711 ≤ FSO/FSI < 0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653 ≤ FSO/FSI < 0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450 ≤ FSO/FSI < 0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327 ≤ FSO/FSI < 0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225 ≤ FSO/FSI < 0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.711 ≤ FSO/FSI < 0.910	SB	0.3735FSI			kHz
		0.653 ≤ FSO/FSI < 0.718	SB	0.3320FSI			kHz
		0.450 ≤ FSO/FSI < 0.660	SB	0.2490FSI			kHz
		0.327 ≤ FSO/FSI < 0.455	SB	0.1660FSI			kHz
		0.225 ≤ FSO/FSI < 0.330	SB	0.1248FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI ≤ 0.539	PR			±0.50	dB
Stopband Attenuation		0.900 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.653 ≤ FSO/FSI < 0.909	SA	90.0			dB
		0.450 ≤ FSO/FSI ≤ 0.660	SA	70.0			dB
		0.167 ≤ FSO/FSI < 0.455	SA	60.0			dB
Group Delay (Ts=1/fs) (* 14)			GD		67 (55FSI+12FSO)		Ts

Echo Canceller Mode

(Ta= -40 ~ 85ºC; VDD12=1.14 ~ 1.3V; AVDD=3.13 ~ 3.47V; VDD33=3.13 ~ 3.47V; TVDD1=1.7 ~ 3.47V; TVDD2=1.7 ~ 3.47V; VSS1 ~ 6= 0V)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
Stopband		0.167 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
Passband Ripple		0.167 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
Stopband Attenuation		0.167 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
Group Delay (Ts=1/fs) (* 14)			GD		67 (55FSI+12FSO)		Ts

Note:

* 15. This time is measured from a rising edge of LRCK after a signal input to the SRC until a rising edge of LRCK before a data output when there is no phase difference between input and output.
* 16. Calculated delay time in the SRC block only. This time is measured from a rising edge of LRCK after a signal input to the SRC until a rising edge of LRCK before a data output when there is no phase difference between input and output.

10. DC Characteristics

■ DC Characteristics

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 (* 17)		VIH1	80%TVDD1			V
Low-Level Input Voltage 1 (* 17)		VIL1			20%TVDD1	V
High-Level Input Voltage 2 (* 18)		VIH2	80%TVDD2			V
Low-Level Input Voltage 2 (* 18)		VIL2			20%TVDD2	V
High-Level Input Voltage 2 DMDAT1/2		VIH2DM	65%TVDD2			V
Low-Level Input Voltage 2 DMDAT1/2		VIL2DM			35%TVDD2	V
High-Level Input Voltage 3 (* 19)		VIH3	80%VDD33			V
Low-Level Input Voltage 3 (* 19)		VIL3			20%VDD33	V
High-Level Input Voltage A (* 20)		VIHA	80%AVDD			V
Low-Level Input Voltage A (* 20)		VILA			20%AVDD	V
SCL, SDA High-Level Input Voltage		VIH4	70%TVDD1			V
SCL, SDA Low-Level Input Voltage		VIL4			30%TVDD1	V
High-Level Input Voltage Iout= -100μA (* 17)		VOH1	TVDD1-0.3			V
Low-Level Input Voltage Iout= 100μA (* 17)		VOL1			0.3	V
High-Level Input Voltage Iout= -100μA (* 18)		VOH2	TVDD2-0.3			V
Low-Level Input Voltage Iout= 100μA (* 18)		VOL2			0.3	V
High-Level Input Voltage Iout= -100μA (* 19)		VOH3	VDD33-0.3			V
Low-Level Input Voltage Iout= 100μA (* 19)		VOL3			0.3	V
High-Level Input Voltage Iout= -100μA (* 20)		AVOH	AVDD-0.3			V
Low-Level Input Voltage Iout= 100μA (* 20)		AVOL			0.3	V
SCL, SDA Low-Level Output Voltage	Fast Mode					
	TVDD2 ≥ 2.0V (Iout= 3mA)	VOL4			0.4	V
	TVDD2 < 2.0V (Iout= 3mA)	VOL4			20%TVDD1	V
	Fast Mode Plus					
	TVDD2 ≥ 2.0V (Iout= 10mA) (* 21)	VOL4			0.4	V
	TVDD2 < 2.0V (Iout= 3mA)	VOL4			20%TVDD1	V
Input Leak Current (* 22)		Iin			±10	μA
Input Leak Current, Pulled down pin (* 23)		Iid		80		μA
				43		kΩ
Input Leak Current, XTI pin		Iix			±10	μA

Notes:

* 17. SDIN1, SDIN2, SDOUT1, SDOUT2, LRCKA, BICKA, LRCKB, BICKB CLKO, PDN, SCLK, SO, CSN, SI/I2CFIL, STO/RDY and SELE pins. The SCL and SDA pins are not included.
* 18. SDIN3, SDIN4/DMDAT1, SDIN5/DMDAT2, LRCKD/DMCLK1, BICKD/DMCLK2, SDOUT3/GPO2, SDOUT4, SDIN5, LRCKC, BICKC, LRCKD, GPIO0/SDIN7, GPIO01/SDOUT7, GPIO02/SDIN8, GPIO03/SDOUT8, ESDO/GPIO04, ESCLK/GPIO05, ESDI/GPIO06 and ECSO/GPIO07 pins.
* 19. TDO / GPO1, TDI/JX3, TMS/JX2, TCK/JX1, TRST/JX0, SDIN6/RX1, RX0, SDOUT5/GPO3, DIRINT/GPO0, SDOUT6/DIT, LRCKE, BICKE, TESTI1 and TESTI2 pins.
* 20. At the XTI pin in external input mode.
* 21. Must be pulled up by 347Ω or more and connected to TVDD2.
* 22. Internal Pulled-down pins and the XTI pin are not included.
* 23. For pins with internal pulled-down registers. (Typ. 43 kΩ @3.3V). TESTI1, BICKE, LRCKE, BICKD/DMCLK2, LRCKD/DMCLK1, LRCKC, BICKC, GPIO00/SDIN7, GPIO01/SDOUT7, GPIO02/SDIN8, GPIO03/SDOUT8, ESDO/GPIO04, ESCLK/GPIO05, ESDI/GPIO06, ECSO/GPIO07, BICKB,LRCKB, LRCKA,BICKA, TESTI2, TRST/JX0, TCK/JX1, TMS/JX2, TDI and JX3 pins.

11. Switching Characteristics

■ System Clock

(Ta = -40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2=1.7~3.47V; VSS1~6= 0V; C_L= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896		24.576	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency (* 24)	fBCLK	0.256		24.576	MHz
Duty Cycle	dBCLK	40	50	60	%
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Mode Except PCM Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 s %
BICK Output Timing					
Frequency (* 24)	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note:
* 24. This value must be "fBCLK ≥ 2 x fs x (input/output data length)".

■ Power Down

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (* 25)	tRST	600			ns

Note:
* 25. The PDN pin must be "L" when power up the AK7707.

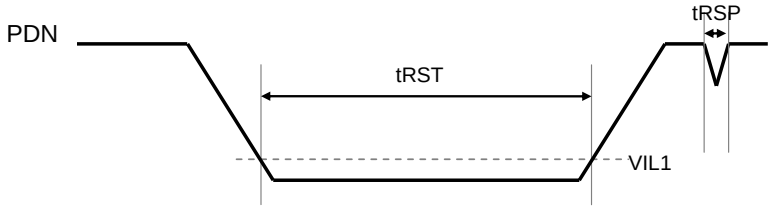


Figure 5. Reset Timing

■ Serial Data Interface (SDIN1~SDIN8, SDOUT1~SDOUT8)

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (* 26)	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" (* 26)	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from LRCK to Serial Data Output (* 27)	tBSOD1			22	ns
Delay Time from BICK"↓" to Serial Data Output (* 26, * 28)	tBSOD2	5		30	ns
Master Mode					
BICK Frequency	fBCLK		32, 48, 64,128, 256,512		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK (* 28)	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from BICK"↓" to Serial Data Output (* 27, * 28)	tBSOD			10	ns

Notes:
* 26. Measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 27. Measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 28. Set SDOPHx bit to "1" and the data should be output based on BICK "↑" if BICK is faster than 12.288MHz such as when using TDM256 mode with 96kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

1. Slave Mode

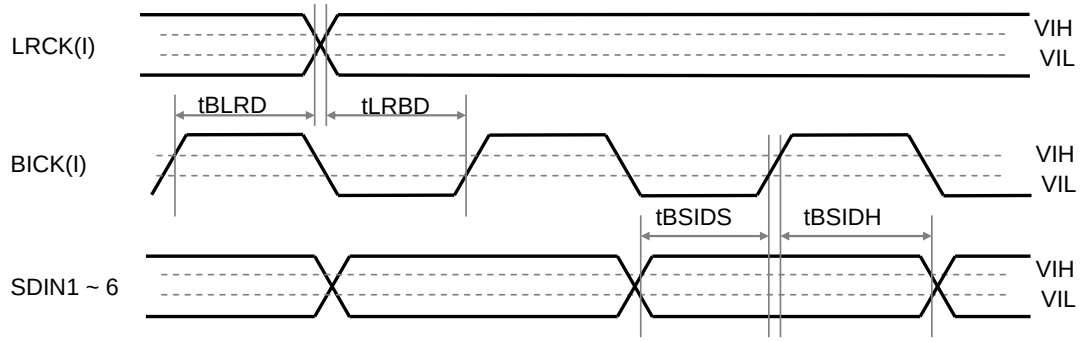


Figure 6. Serial Interface Input Timing in Slave Mode

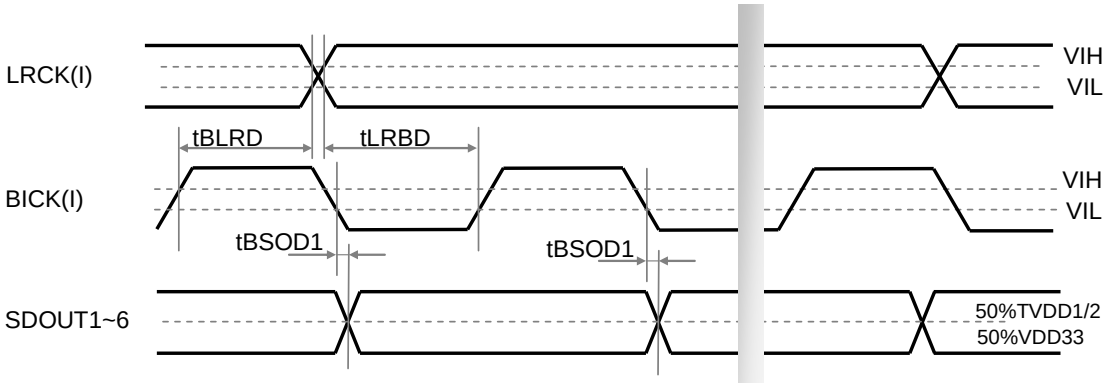


Figure 7. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “0”)

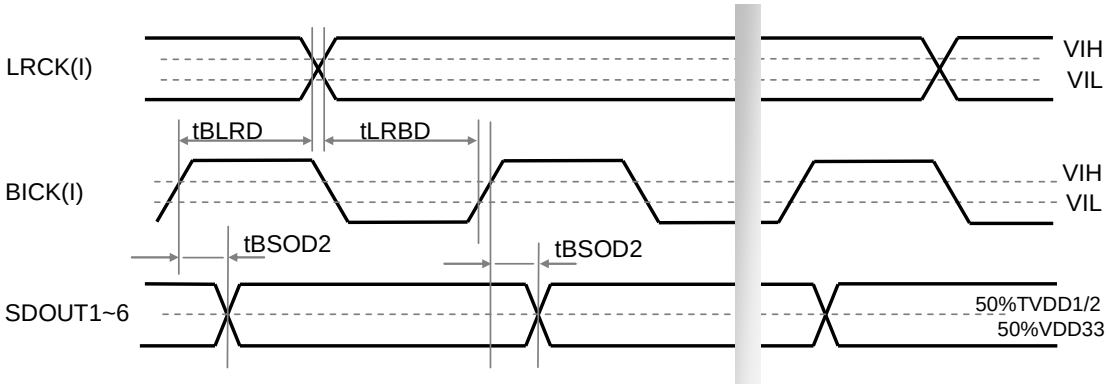


Figure 8. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

2. Master Mode

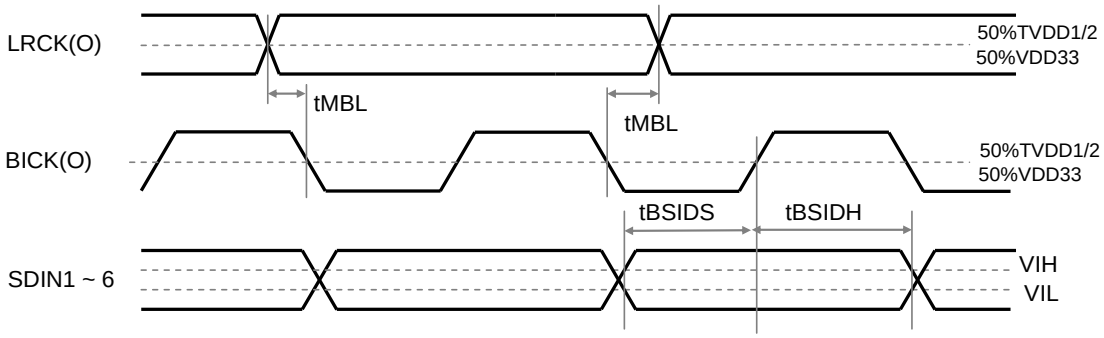


Figure 9. Serial Interface Input Timing in Master Mode

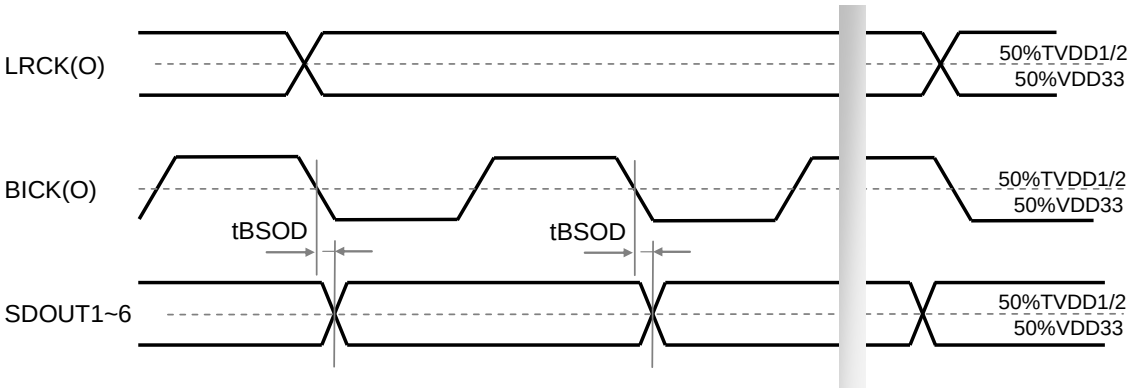


Figure 10. Serial Interface Output Timing in Master Mode

■ SPI Interface

1. Clock Reset (CKRESETN bit = "0")

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V; C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency	fSCLK			3.5	MHz
SCLK Low-level Width	tSCLKL	135			ns
SCLK High-level Width	tSCLKH	135			ns
Microcontroller → AK7707					
CSN High-level Width	tWRQH	300			ns
From CSN "↑" to PDN "↑"	tRST	360			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	300			ns
From SCLK "↑" to CSN "↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7707 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (* 29)	tSOH	120			ns

Note:

* 29. Except when writing the 8th bit of the command code.

2. PLL Lock (CKRESETN bit = "1" and PLL is locked)

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V; C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency (* 30)	fSCLK			7	MHz
SCLK Low-level Width	tSCLKL	60			ns
SCLK High-level Width	tSCLKH	60			ns
Microcontroller → AK7707					
CSN High-level Width	tWRQH	150			ns
From CSN "↑" to PDN "↑"	tRST	180			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	150			ns
From SCLK "↑" to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Setup Time	tSIH	60			ns
AK7707 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (* 29)	tSOH	60			ns

Note:

* 30. It takes maximum 10ms to lock PLL after setting CKRESETN bit = "0"→ "1".
Control registers can always be accessed by 7MHz.

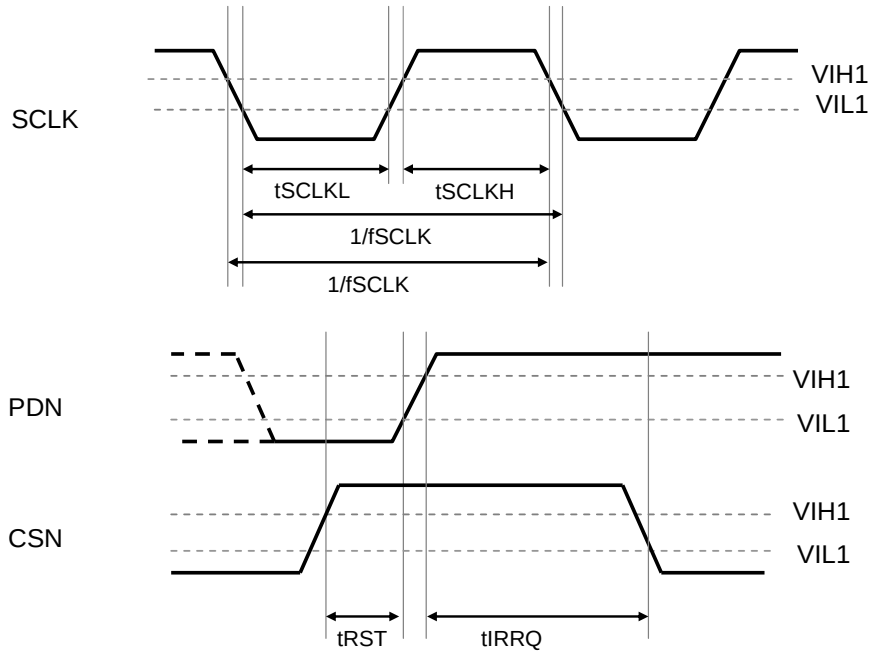


Figure 11. SPI Interface Timing 1

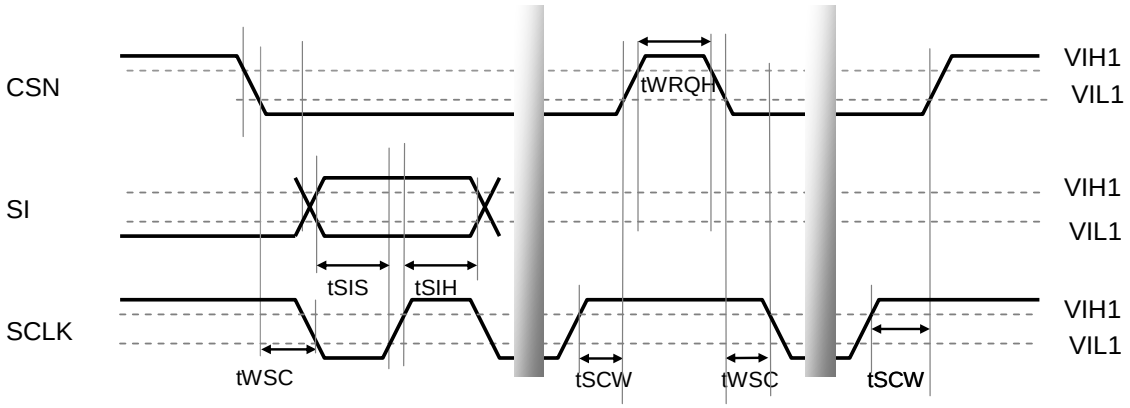


Figure 12. SPI Interface Timing 2 (Microcontroller → AK7707)

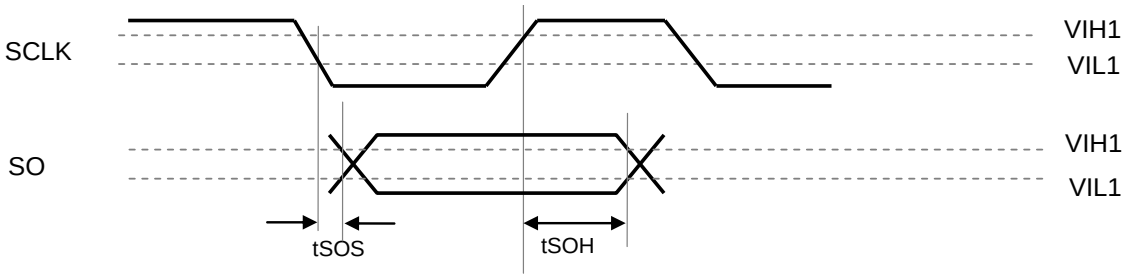


Figure 13. SPI Interface Timing 3 (AK7707 → Microcontroller)

■ I²C Interface

(Ta = −40~85ºC; VDD12 = 1.14~1.3V; AVDD = 3.13~3.47V; VDD33 = 3.13~3.47V; TVDD1 = 1.7~3.47V; TVDD2 = 1.7~3.47V; VSS1~6 = 0V; C_L = 20pF)

<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

<I²C: Fast Mode Plus>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.26	-	-	µs
Clock Low Time	tLOW	0.5	-	-	µs
Clock High Time	tHIGH	0.26	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	550	pF

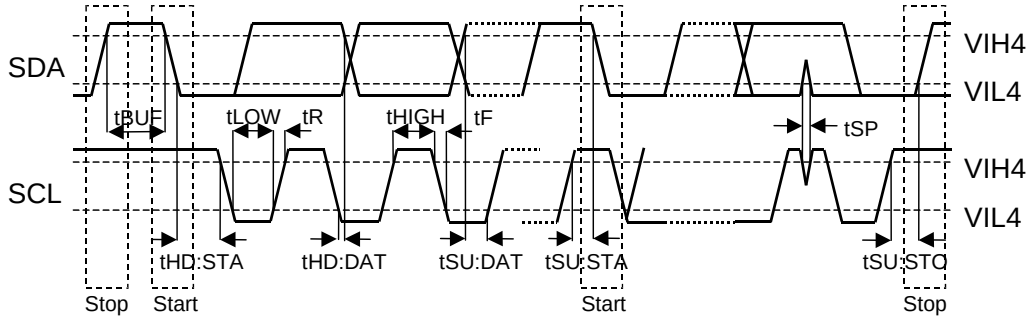


Figure 14. I²C-bus Interface Timing

■ Master SPI Interface

(Ta= -40 ~ 85ºC; VDD12=1.14 ~ 1.3V; AVDD=3.13 ~ 3.47V; VDD33=3.13 ~ 3.47V; TVDD1=1.7 ~ 3.47V; TVDD2=1.7 ~ 3.47V; VSS1 ~ 6= 0V; C_L= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Mode					
SCLK Frequency(* 31)	-			6.144	MHz
SCLK Duty (* 32)	-		50		%
ECSO ↓ to ESCLK ↑	-	80			ns
Delay Time from ESCLK ↓ to ESDO	-	-40		40	ns
ESDI Hold Time from ESCLK Rising	-	40			ns
ESDI Setup Time from ESCLK Rising	-	40			ns
Through Mode					
Slave Port → Master Port					
Delay Time from CSN Input to ECSO Output	-	0		40	ns
Delay Time from SCLK Input to ESCLK Output	-	0		40	ns
Delay Time from SI Input to ESDO Output	-	0		40	ns
Master Port → Slave Port					
Delay Time from ESDI Input to SO Output	-	0		40	ns

* 31. When using self-boot function, a X'tal lower than 12.288MHz is supported.
* 32. When dividing number is even.

■ JTAG Interface

(Ta= -40 ~ 85ºC; VDD12=1.14 ~ 1.3V;AVDD=3.13 ~ 3.47V;VDD33=3.13 ~ 3.47V; TVDD1=1.7 ~ 3.47V; TVDD2=1.7 ~ 3.47V; VSS1 ~ 6= 0V ; C_L= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TCK Frequency				7	MHz
TCK Pulse width Low		60			ns
TCK Pulse width High		60			ns
TMS Setup Time from TCK rising		60			ns
TMS Hold Time from TCK rising		60			ns
TDI Setup Time from TCK rising		60			ns
TDI Hold Time from TCK rising		60			ns
TRST Setup Time from TCK rising		60			ns
From TRST " ↑ " to TCK " ↑ "		120			ns
Delay Time from TCK falling to TDO				60	ns

12. Recommended External Circuits

■ Connection Diagram

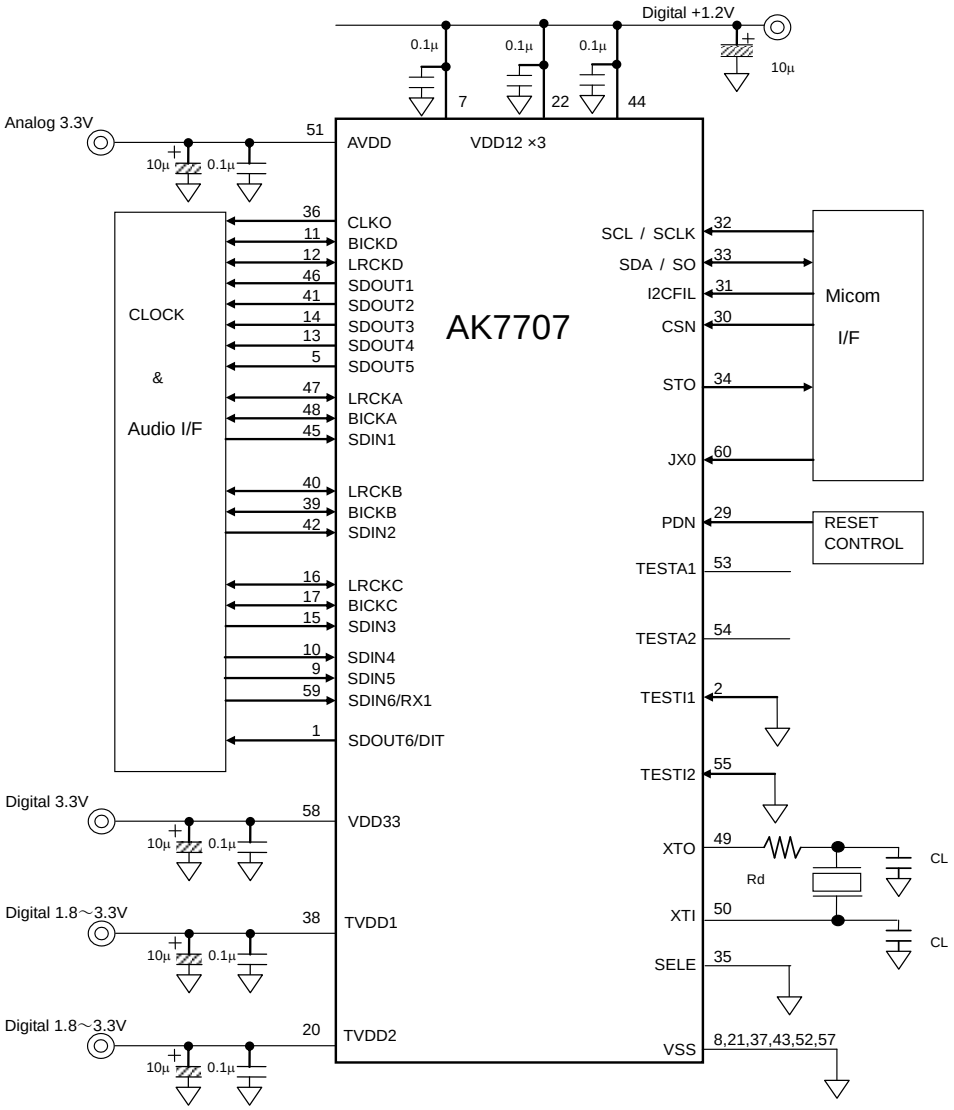


Figure 15. System Connection Diagram

■ Peripheral Circuit

1. Ground

All VSS should be connected to the same analog ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as close as possible to the AK7707.

2. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of the AK7707 must be connected to CMOS or low voltage logic ICs such as 74HC and 74AC for CMOS and 74LV, 74LV-A, 74ALVC and 74AVC for low voltage logic ICs.

3. Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown below.

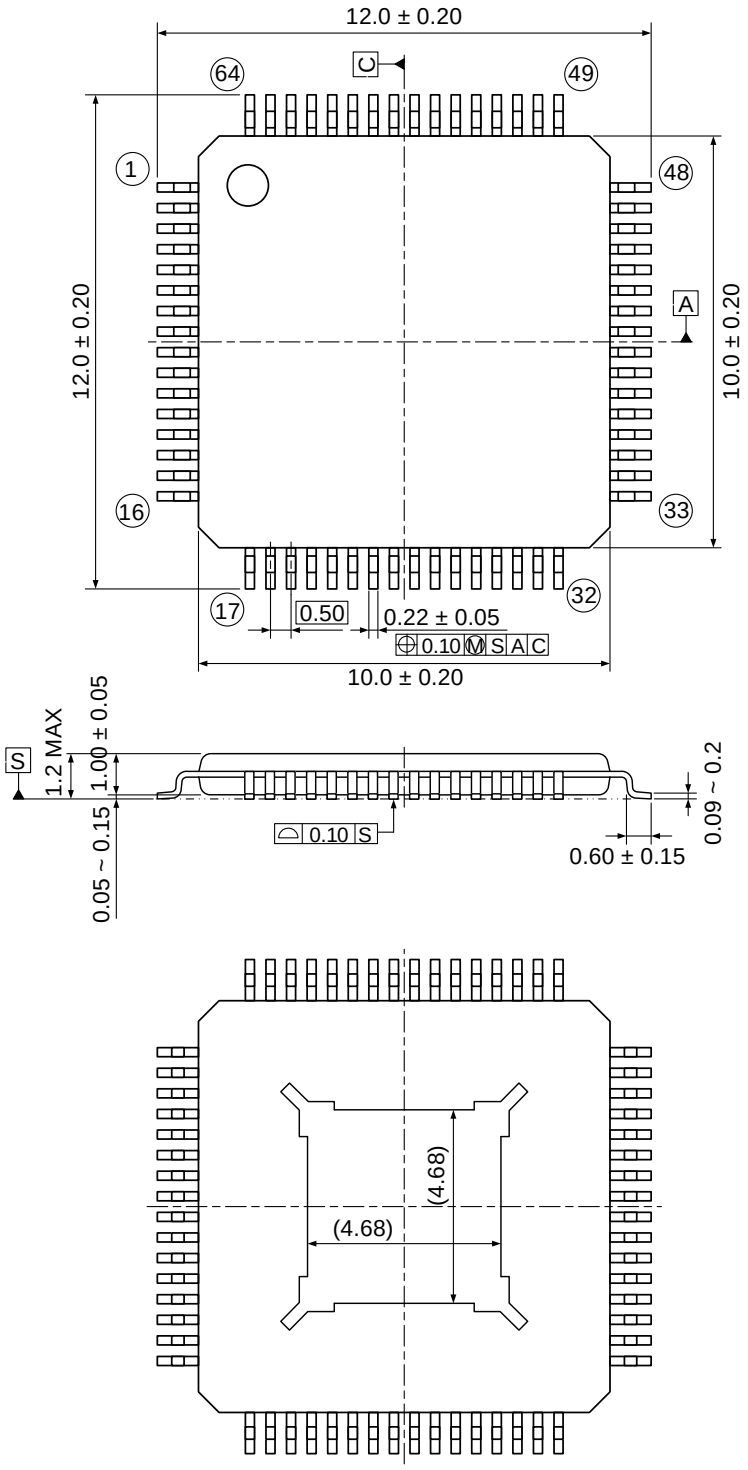
XTAL Oscillator	R1 (Max.)	C0 (Max.)	XTI, XTO pin Capacity (CL)
12.288MHz	80Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	22pF
24.576MHz	40Ω	2.5pF	15pF

Table 4. Recommended Resistance and Capacitance with Crystal Oscillator

13. Package

■ **Outline Dimensions**

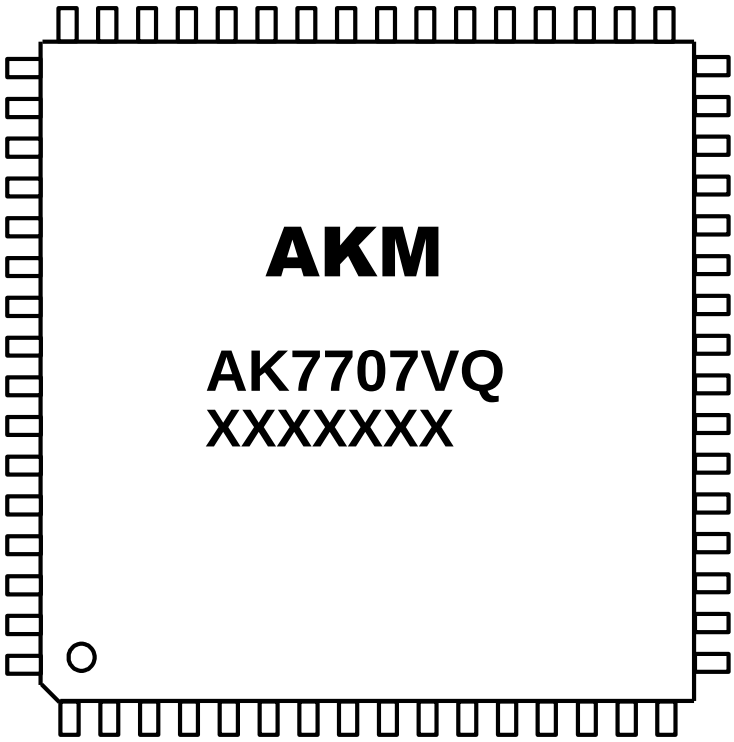
64-pin HTQFP (Unit: mm)



■ **Material and Lead Finish**

Package: Epoxy
Lead frame: Copper
Lead-finish: Soldering (Pb free) plate

■ **Marking**



1) pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7707VQ
4) Asahi Kasei Logo

14. Ordering Guide

■ **Ordering Guide**

AK7707VQ	-40 ~ +85ºC	64-pin HTQFP (0.5mm pitch)
AKD7707	Evaluation board for AK7707	

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