

## Single channel high-side driver with analog for automotive applications

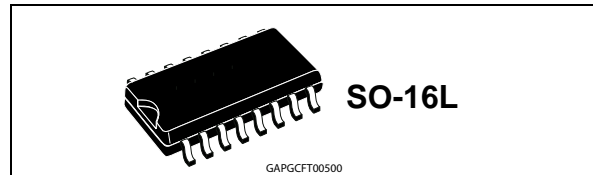
Datasheet – production data

### Features

Max supply voltage	$V_{CC}$	41 V
Operating voltage range	$V_{CC}$	4.5 V to 28 V
Max on-state resistance (per ch.)	$R_{ON}$	160 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	10 A
Off-state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected.

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Very low current sense leakage
  - AEC-Q100 qualified
- Diagnostic functions
  - Proportional load current sense
  - High-precision current sense for wide-range currents
  - Current sense disable
  - OFF-state open-load detection
  - Output short to  $V_{CC}$  detection
  - Overload and short to ground (power limitation) indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self-limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$



- Overtemperature shutdown with autorestart (thermal shutdown)
- Reverse battery protected
- Electrostatic discharge protection

### Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

### Description

The VN5E160ASO-E is a single channel high-side driver manufactured using ST proprietary VIPower<sup>®</sup> M0-5 technology and housed in SO-16L package. The device is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for the use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to  $V_{CC}$  diagnosis and ON-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS\_DIS pin high to share the external sense resistor with similar devices.

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# 1 Block diagram and pin configuration

Figure 1. Block diagram

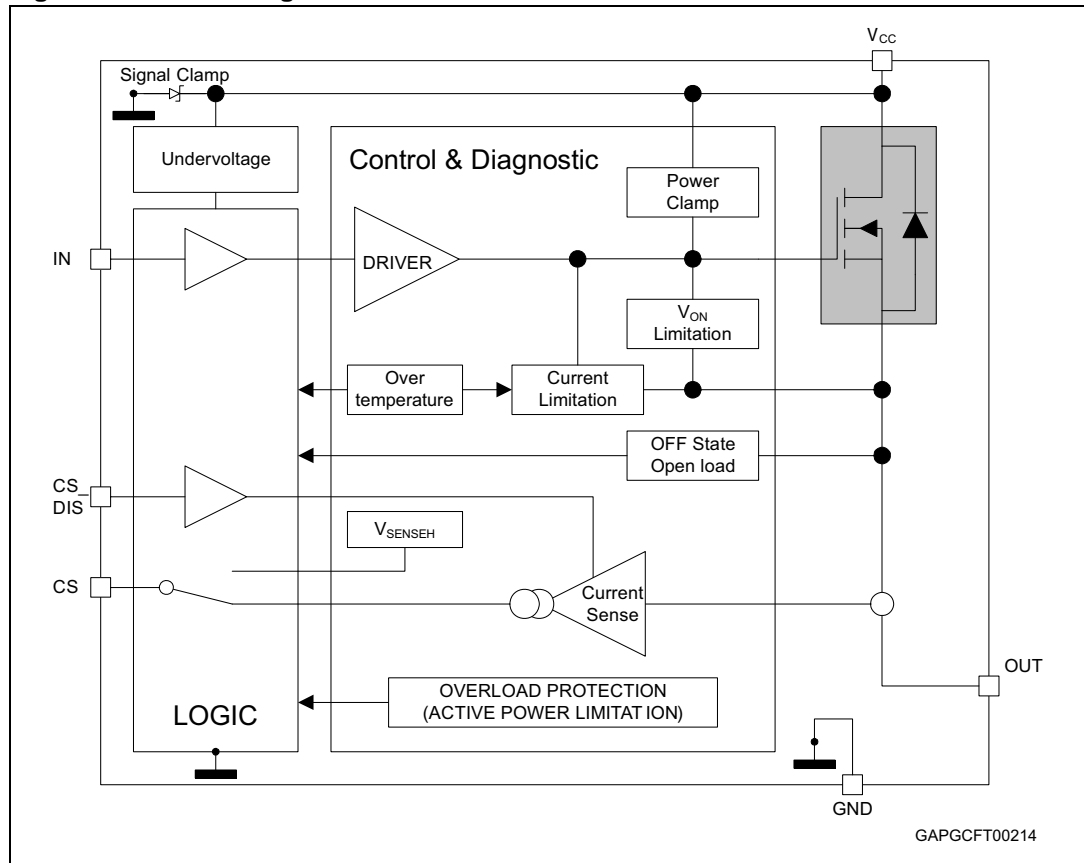


Table 1. Pin function

Name	Function
$V_{CC}$	Battery connection.
OUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
IN	Voltage-controlled input pin with hysteresis, CMOS compatible; it controls output switch state.
CS	Analog current sense pin; it delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

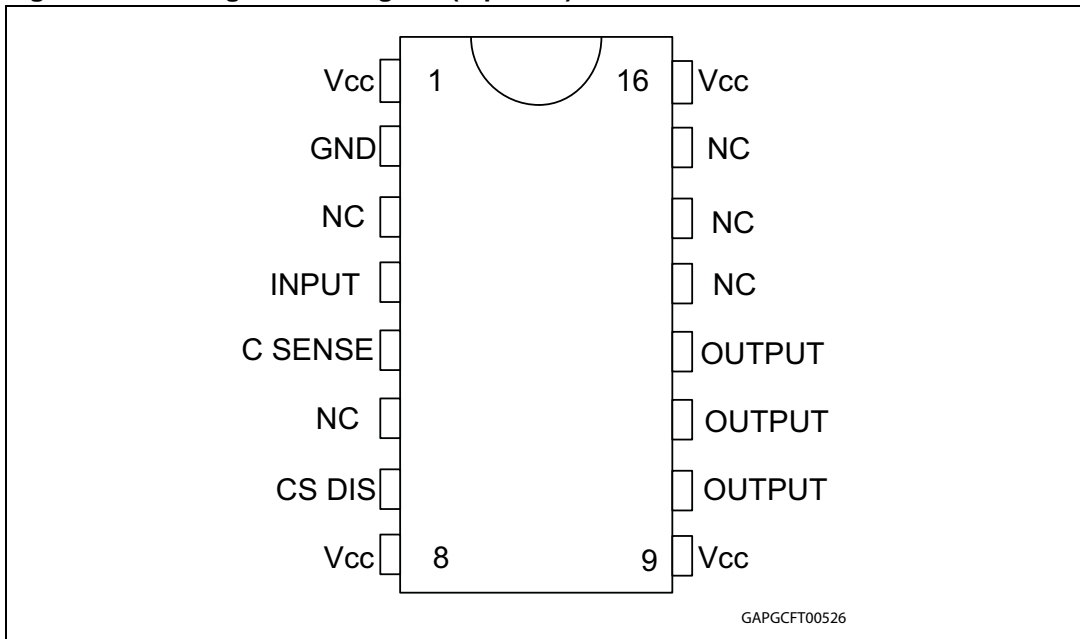


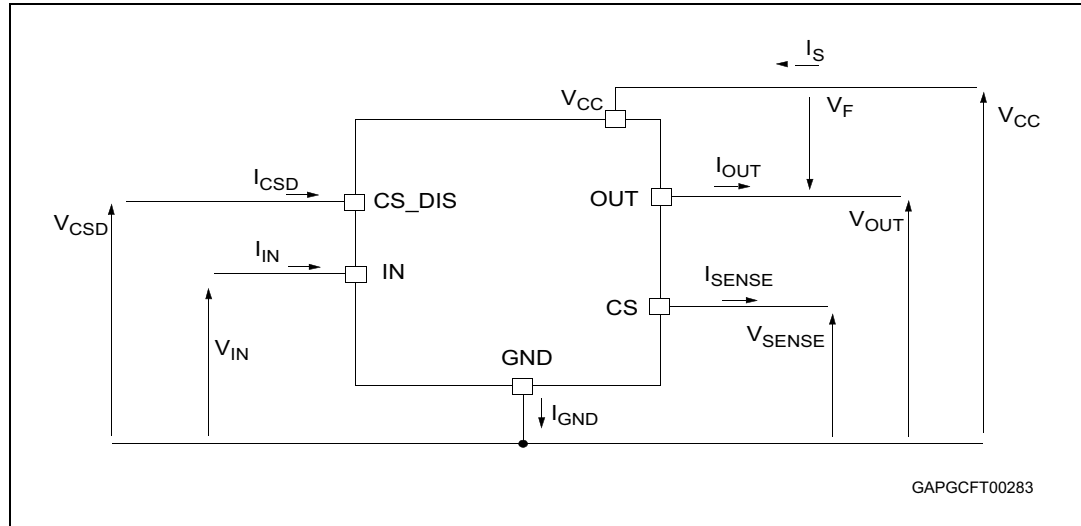
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X <sup>(1)</sup>	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

1. X: do not care.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



1.  $V_F = V_{OUT} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the “absolute maximum ratings” table for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC} - 41$ $+V_{CC}$	V V
$E_{MAX}$	Maximum switching energy (single pulse) ( $L = 8 \text{ mH}$ ; $R_L = 0 \text{ } \Omega$ ; $V_{bat} = 13.5 \text{ V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_{OUT} = I_{limL}(Typ.)$ )	36	mJ

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
V <sub>ESD</sub>	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF)		
	- IN	4000	V
	- CS	2000	V
	- CS_DIS	4000	V
	- OUT	5000	V
	- V <sub>CC</sub>	5000	V
V <sub>ESD</sub>	Charge device model (CDM-AEC-Q100-011)	750	V
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	°C

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Typical value	Unit
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb <sup>(1)</sup>	18.5	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction - ambient on two layers pcb	See <a href="#">Figure 36</a>	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction - ambient on two layers pcb <sup>(2)</sup>	38	°C/W

1. The measure is done in accordance with the JESD 51-8.

2. Four Layers PCB characteristics:

- Cu thickness: 70 um outer layers, 35 um inner layers
- Board finish thickness 1.6 mm +/- 10%
- Thermal vias separation 1.2 mm
- Thermal via diameter 0.3 mm +/- 0.08 mm
- Cu thickness on vias 0.025 mm
- Device soldered at about 2cm from the PCB edge with two sqcm of exposed copper.



## 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 28\text{ V}$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise stated.

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	28	V
$V_{USD}$	Undervoltage shut-down			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
$R_{ON}$	ON-state resistance	$I_{OUT} = 1\text{ A}$ ; $T_j = 25^\circ\text{C}$		160		m $\Omega$
		$I_{OUT} = 1\text{ A}$ ; $T_j = 150^\circ\text{C}$			320	
		$I_{OUT} = 1\text{ A}$ ; $V_{CC} = 5\text{ V}$ ; $T_j = 25^\circ\text{C}$			210	
$V_{clamp}$	Voltage clamp	$I_S = 20\text{ mA}$	41	46	52	V
$I_S$	Supply current	OFF-state: $V_{CC} = 13\text{ V}$ ; $V_{IN} = V_{OUT} = 0\text{ V}$ ; $T_j = 25^\circ\text{C}$		2 <sup>(1)</sup>	5 <sup>(1)</sup>	$\mu\text{A}$
		ON-state: $V_{IN} = 5\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $I_{OUT} = 0\text{ A}$		1.9	3.5	mA
$I_{L(off1)}$	OFF-state output current	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25^\circ\text{C}$	0	0.01	3	$\mu\text{A}$
		$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125^\circ\text{C}$	0		5	
$V_F$	Output - $V_{CC}$ diode voltage	$-I_{OUT} = 1\text{ A}$ ; $T_j = 150^\circ\text{C}$			0.7	V

1. PowerMOS leakage included.

**Table 6. Switching ( $V_{CC} = 13\text{ V}$ ;  $T_j = 25^\circ\text{C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 13\ \Omega$ (see <a href="#">Figure 6</a> )	—	10	—	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L = 13\ \Omega$ (see <a href="#">Figure 6</a> )	—	10	—	$\mu\text{s}$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 13\ \Omega$	—	See <a href="#">Figure 26</a>	—	V/ $\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 13\ \Omega$	—	See <a href="#">Figure 28</a>	—	V/ $\mu\text{s}$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 13\ \Omega$ (see <a href="#">Figure 6</a> )	—	0.05	—	mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 13\ \Omega$ (see <a href="#">Figure 6</a> )	—	0.03	—	mJ

**Table 7. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low-level input voltage				0.9	V
$I_{IL}$	Low-level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	High-level input voltage		2.1			V
$I_{IH}$	High-level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Hysteresis input voltage		0.25			V
$V_{ICL}$	Input voltage clamp	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		
$V_{CSDL}$	Low-level CS_DIS voltage				0.9	V
$I_{CSDL}$	Low-level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{CSDH}$	High-level CS_DIS voltage		2.1			V
$I_{CSDH}$	High-level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{CSD(hyst)}$	Hysteresis CS_DIS voltage		0.25			V
$V_{CSCL}$	CS_DIS voltage clamp	$I_{CSD} = 1\text{ mA}$	5.5		7	V
		$I_{CSD} = -1\text{ mA}$		-0.7		

**Table 8. Protection and diagnostics<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short-circuit current	$V_{CC} = 13\text{ V}$	7	10	14	A
		$5\text{ V} < V_{CC} < 28\text{ V}$			14	A
$I_{limL}$	Short-circuit current during thermal cycling	$V_{CC} = 13\text{ V}; T_R < T_j < T_{TSD}$		2.5		A
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
$T_{RS}$	Thermal reset of STATUS		135			$^{\circ}\text{C}$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		$^{\circ}\text{C}$
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 1\text{ A}; V_{IN} = 0, L = 20\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.03\text{ A}$ (see <a href="#">Figure 8</a> ) $T_j = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V<sub>CC</sub> < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.025 A; V <sub>SENSE</sub> = 0.5 V T <sub>j</sub> = -40°C to 150°C	265	490	715	
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.35 A; V <sub>SENSE</sub> = 0.5 V T <sub>j</sub> = -40°C to 150°C T <sub>j</sub> = 25°C to 150°C	355 385	465 465	575 545	
dK <sub>1</sub> /K <sub>1</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 0.35 A; V <sub>SENSE</sub> = 0.5 V T <sub>j</sub> = -40°C to 150°C	-11		+11	%
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.5 A; V <sub>SENSE</sub> = 4 V T <sub>j</sub> = -40°C to 150°C T <sub>j</sub> = 25°C to 150°C	380 400	455 455	530 510	
dK <sub>2</sub> /K <sub>2</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 0.5 A; T <sub>j</sub> = -40°C to 150°C	-8		+8	%
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 1.5 A; V <sub>SENSE</sub> = 4 V T <sub>j</sub> = -40°C to 150°C T <sub>j</sub> = 25°C to 150°C	420 420	455 455	490 480	
dK <sub>3</sub> /K <sub>3</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 1.5 A; T <sub>j</sub> = -40°C to 150°C	-4		+4	%
I <sub>SENSE0</sub>	Analog sense leakage current	I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 0 V; T <sub>j</sub> = -40°C to 150°C	0		1	μA
		I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 0 V; V <sub>IN</sub> = 5 V; T <sub>j</sub> = -40°C to 150°C	0		2	
		I <sub>OUT</sub> = 1 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 5 V; T <sub>j</sub> = -40°C to 150°C	0		1	
V <sub>SENSE</sub>	Max analog sense output voltage	R <sub>SENSE</sub> = 10 KΩ I <sub>OUT</sub> = 1 A;	5			V
V <sub>SENSEH</sub> <sup>(2)</sup>	Analog sense output voltage in fault condition	V <sub>CC</sub> = 13 V; R <sub>SENSE</sub> = 3.9 KΩ		8		V
I <sub>SENSEH</sub> <sup>(2)</sup>	Analog sense output current in fault condition	V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 5 V		9		mA
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 0.025 A < I <sub>OUT</sub> < 1.5 A I <sub>SENSE</sub> = 90% of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )		40	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 0.025 A < I <sub>OUT</sub> < 1.5 A I <sub>SENSE</sub> = 10% of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )		5	20	μs

**Table 9. Current sense (8 V < V<sub>CC</sub> < 18 V) (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>DSENSE2H</sub>	Delay response time from rising edge of IN pin	V <sub>SENSE</sub> < 4 V; 0.025 A < I <sub>OUT</sub> < 1.5 A I <sub>SENSE</sub> =90% of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )		30	160	μs
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4 V; I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> I <sub>OUTMAX</sub> =1.5A (see <a href="#">Figure 7</a> )			110	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of IN pin	V <sub>SENSE</sub> < 4 V; 0.025 A < I <sub>OUT</sub> < 1.5 A I <sub>SENSE</sub> =10% of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )		80	250	μs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open load OFF-state detection.

**Table 10. Open-load detection (8 V < V<sub>CC</sub> < 18 V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>OL</sub>	OFF-state open-load voltage detection threshold	V <sub>IN</sub> = 0 V; 8 V < V <sub>CC</sub> < 18 V	2		4	V
I <sub>OL</sub>	ON-state open-load current detection threshold	V <sub>IN</sub> = 5V; 8 V < V <sub>CC</sub> < 18 V I <sub>SENSE</sub> = 5 μA	0.5		5	mA
t <sub>DSTKON</sub>	Output short-circuit to V <sub>CC</sub> detection delay at turn-off	See <a href="#">Figure 5</a>	180		1200	μs
I <sub>L(off2)r</sub>	OFF-state output current at V <sub>OUT</sub> = 4 V	V <sub>IN</sub> = 0 V; V <sub>SENSE</sub> = 0 V V <sub>OUT</sub> rising from 0 V to 4 V	-120		0	μA
I <sub>L(off2)f</sub>	OFF-state output current at V <sub>OUT</sub> = 2 V	V <sub>IN</sub> = 0 V; V <sub>SENSE</sub> = V <sub>SENSEH</sub> V <sub>OUT</sub> falling from V <sub>CC</sub> to 2 V	-50		90	
td_vol	Delay response from output rising edge to V <sub>SENSE</sub> rising edge in open-load	V <sub>OUT</sub> = 4 V; V <sub>IN</sub> = 0 V V <sub>SENSE</sub> = 90% of V <sub>SENSEH</sub>			20	μs

Figure 4. Current sense delay characteristics

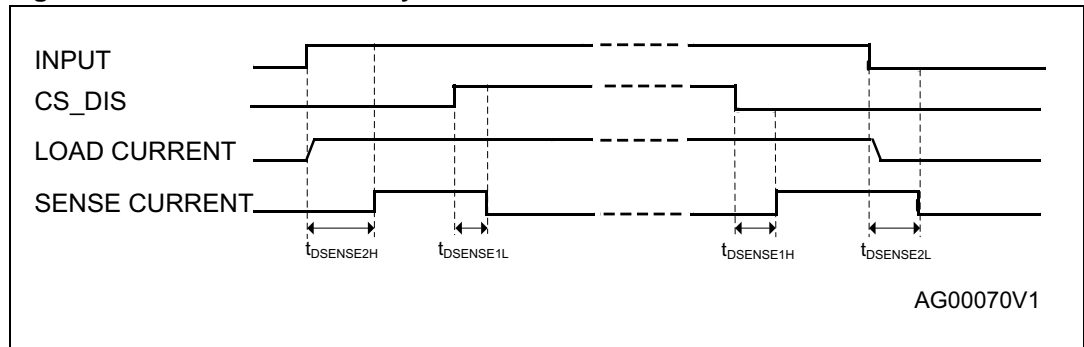


Figure 5. OFF-state open-load delay timing

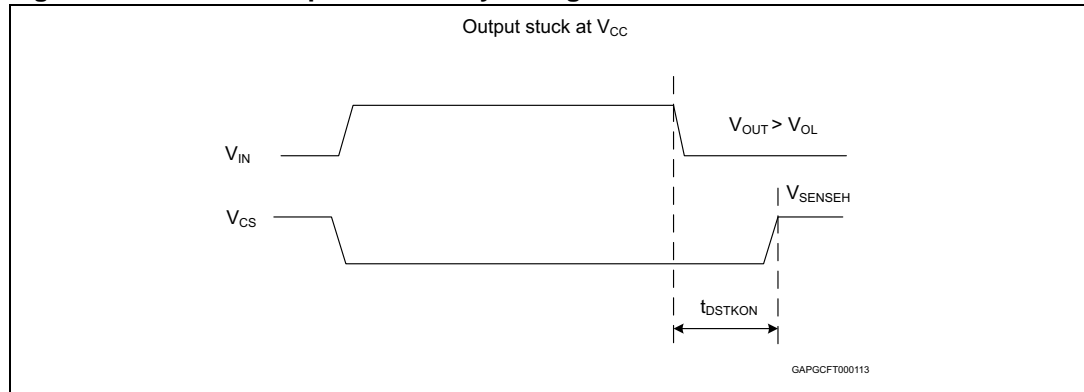
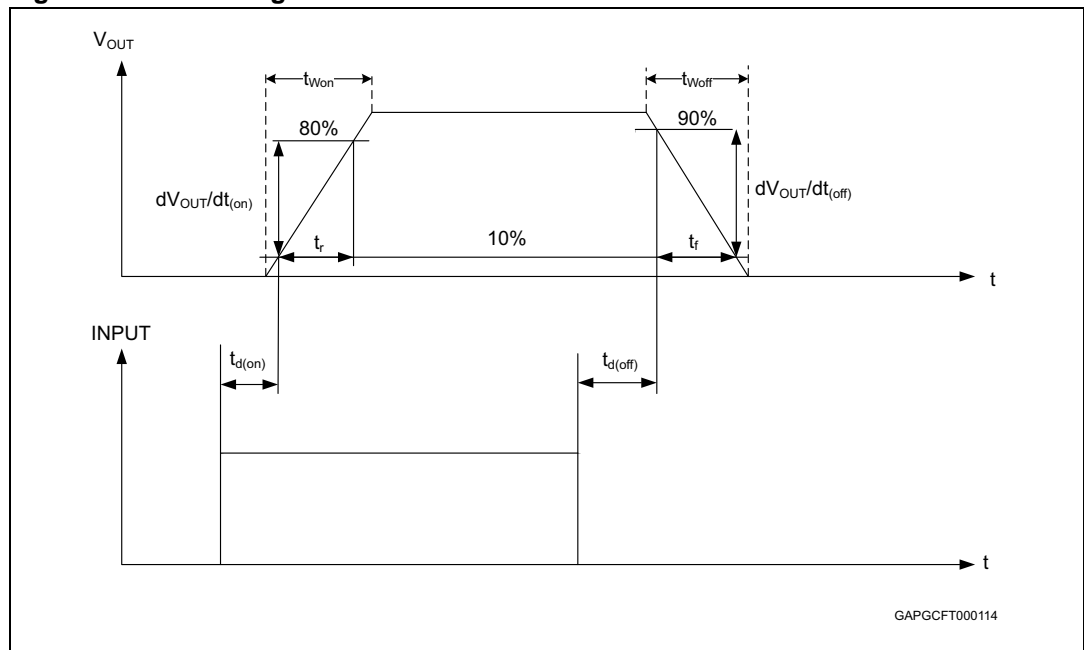
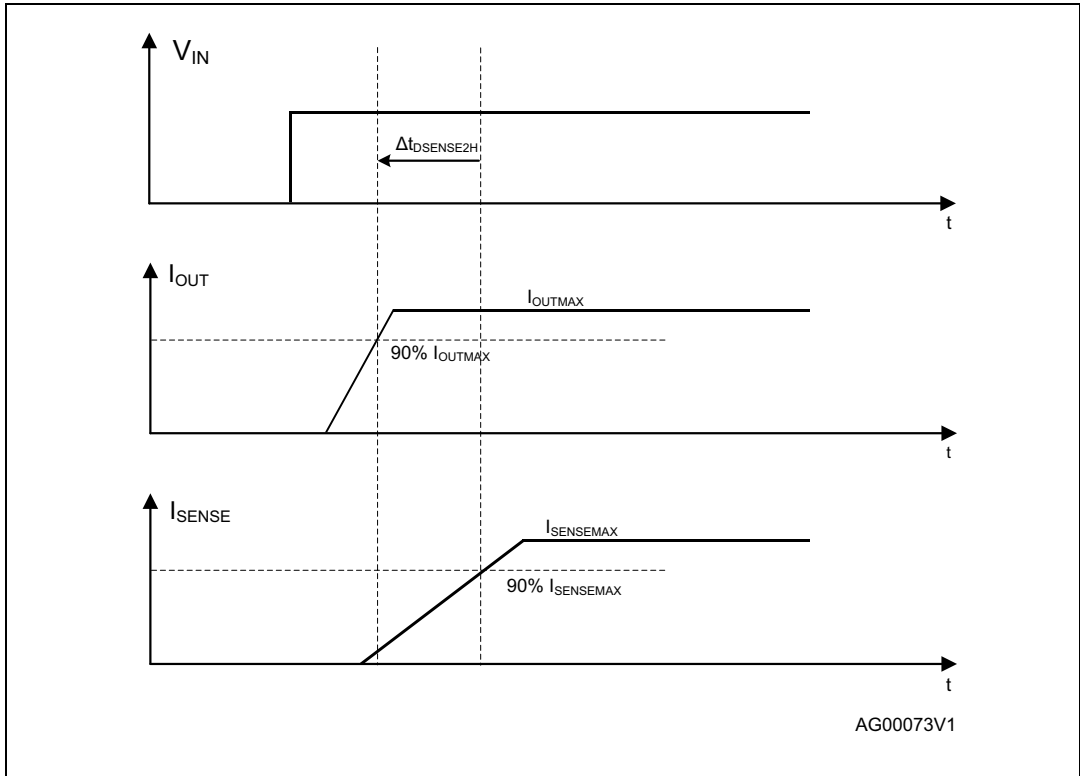


Figure 6. Switching characteristics



**Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)**



**Figure 8. Output voltage drop limitation**

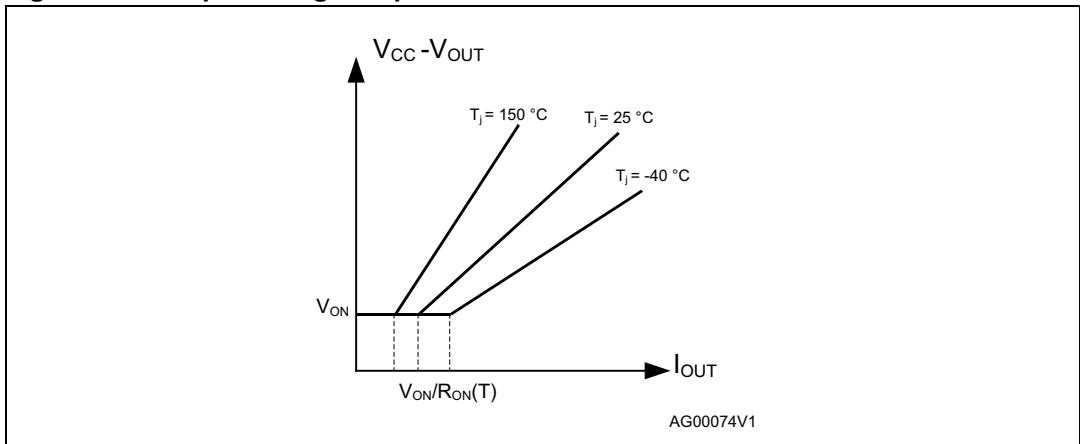


Figure 9.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$

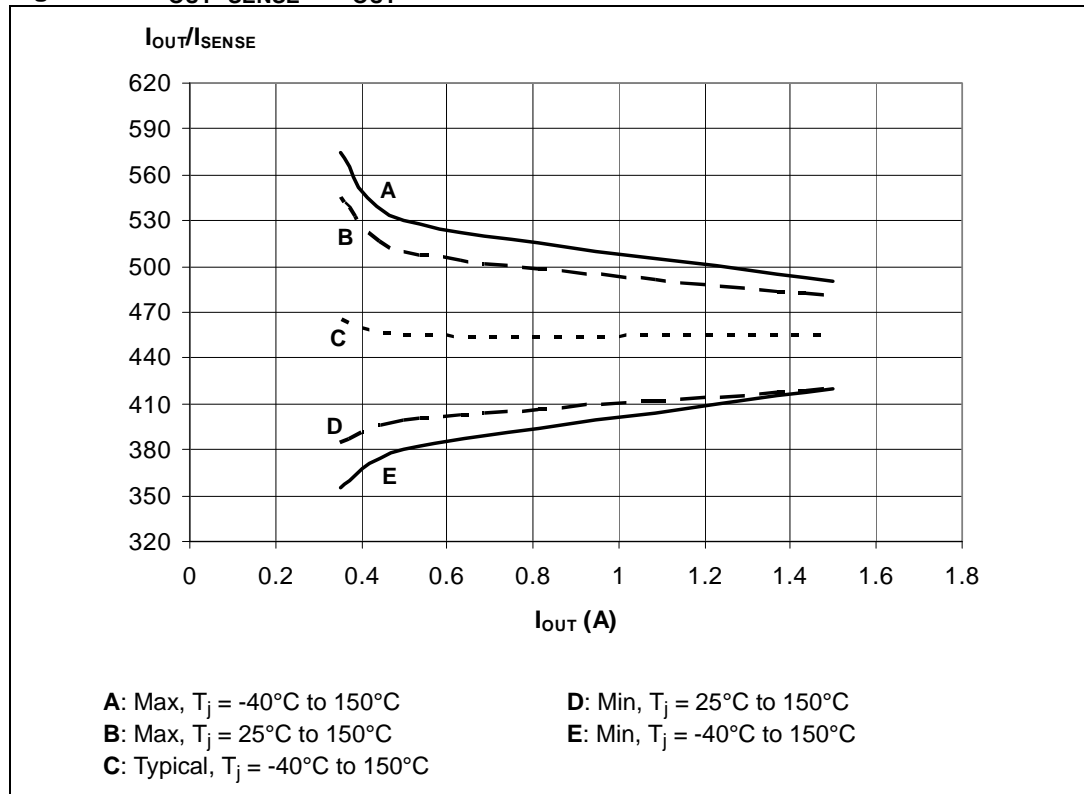
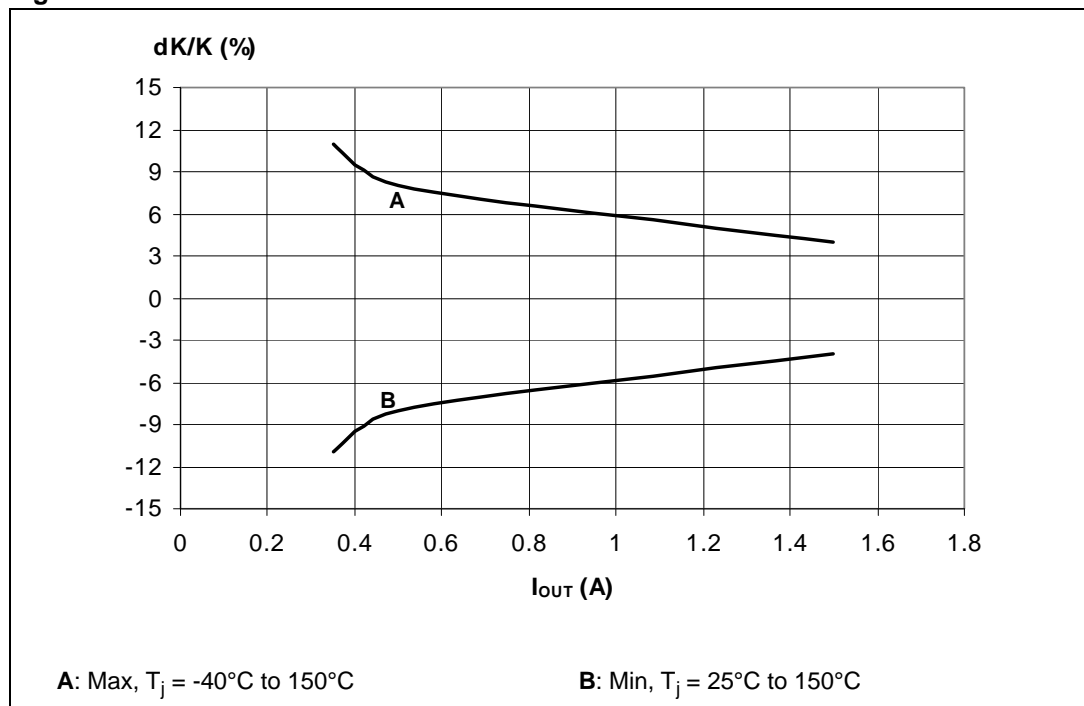


Figure 10. Maximum current sense ratio drift vs load current<sup>(1)</sup>



1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	IN	OUT	SENSE ( $V_{CSD} = 0\text{ V}$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overload	H	X (no power limitation)	Nominal
	H	Cycling (power limitation)	$V_{SENSEH}$
Short circuit to GND (Power limitation)	L	L	0
	H	L	$V_{SENSEH}$
OFF-state open-load (with external pull-up)	L	H	$V_{SENSEH}$

1. If the  $V_{CSD}$  is high, the SENSE output is at high impedance, its potential depends on leakage currents and external circuit.



**Table 12. Electrical transient requirements (part 1)**

ISO 7637-2: 2004(E) Test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b <sup>(2)</sup>	+65 V	+87 V	1 pulse			400 ms, 2 Ω

**Table 13. Electrical transient requirements (part 2)**

ISO 7637-2: 2004(E) Test pulse	Test level results <sup>(1)</sup>	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(2)</sup>	C	C

1. The above test levels must be considered referred to  $V_{CC} = 13.5$  V except for pulse 5b

2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

**Table 14. Electrical transient requirements (part 3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

## 2.4 Waveforms

Figure 11. Normal operation

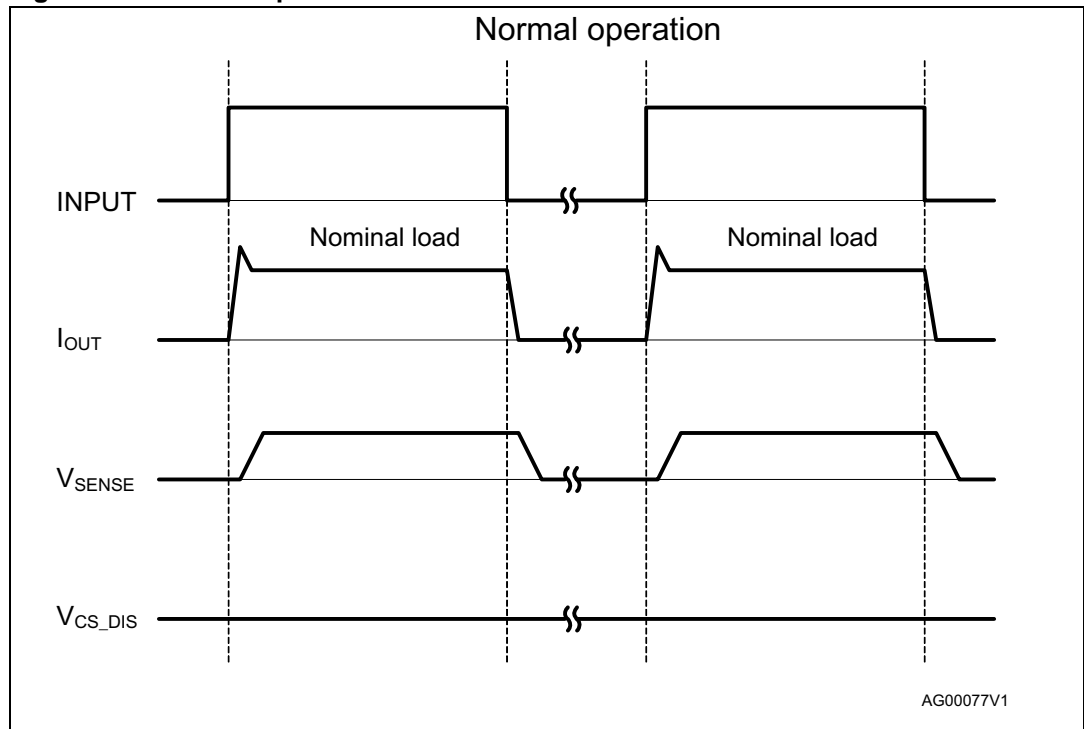


Figure 12. Overload or short to GND

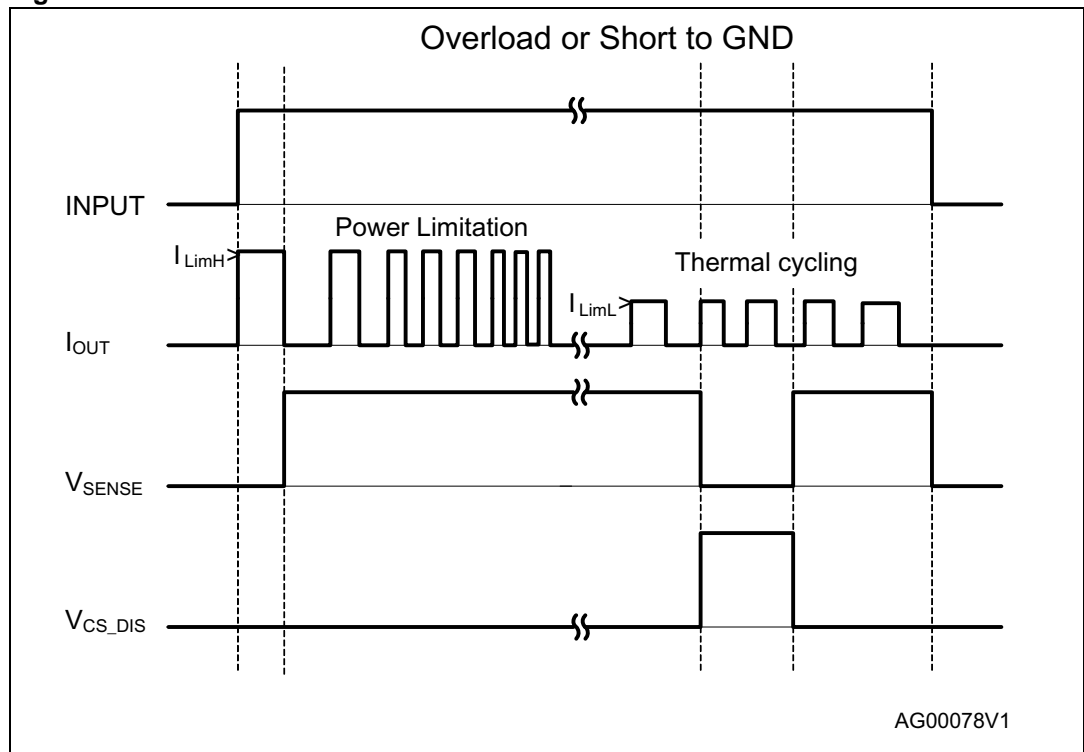
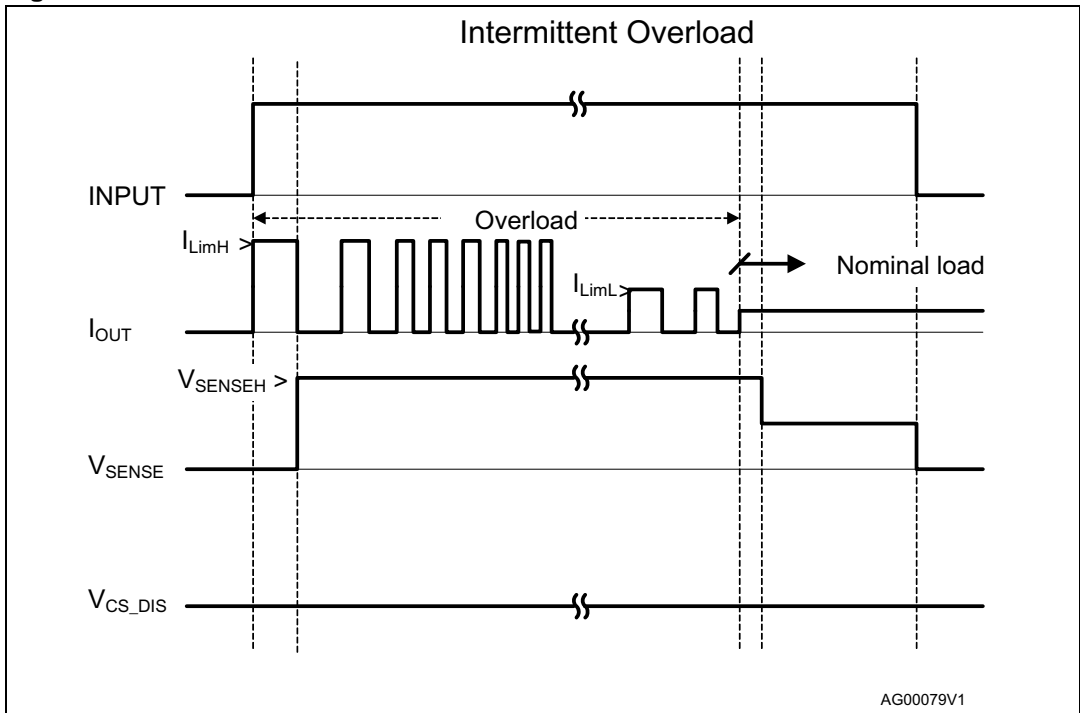
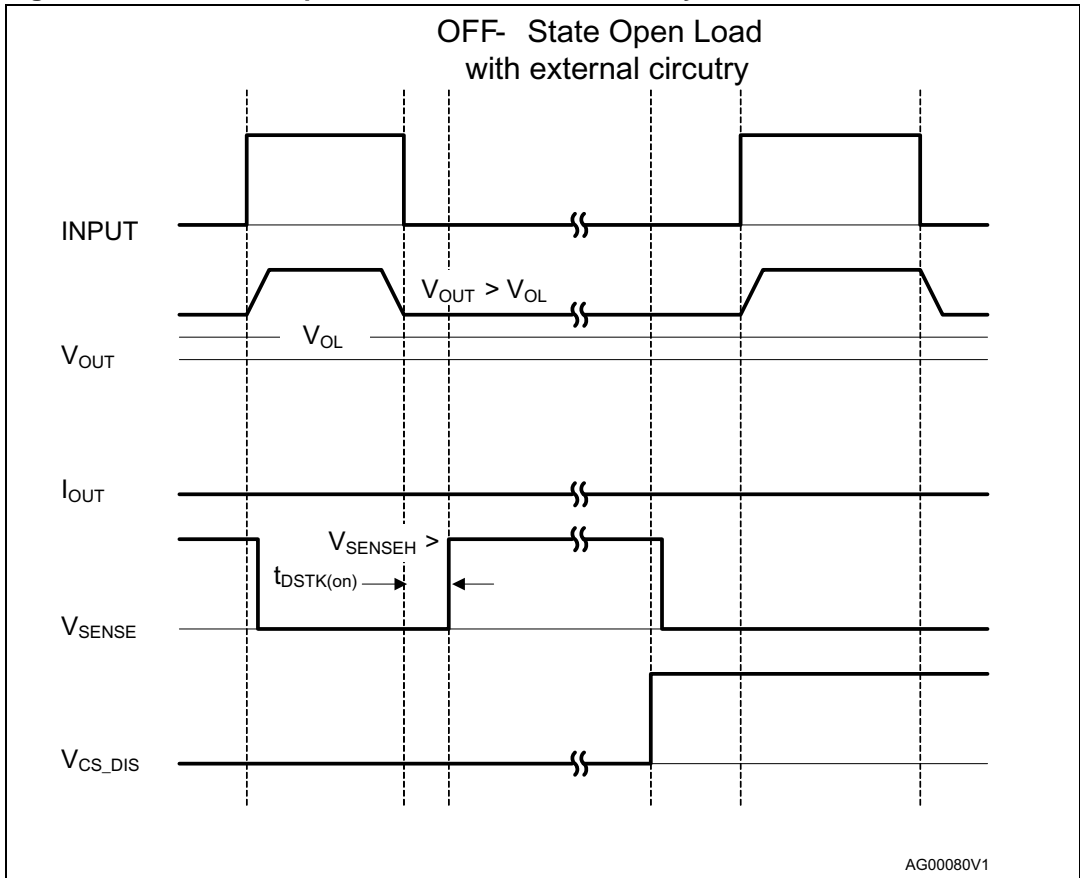


Figure 13. Intermittent overload



AG00079V1

Figure 14. OFF-state open-load with external circuitry



AG00080V1

Figure 15. Short to  $V_{CC}$

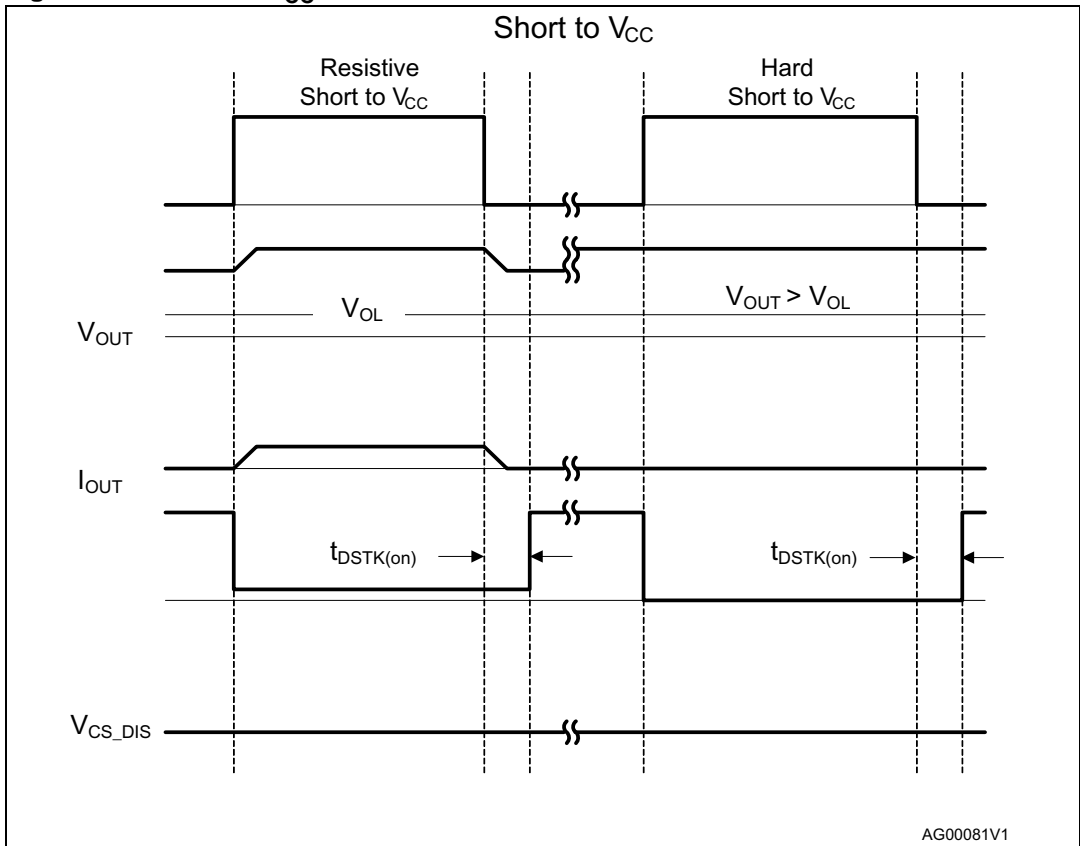
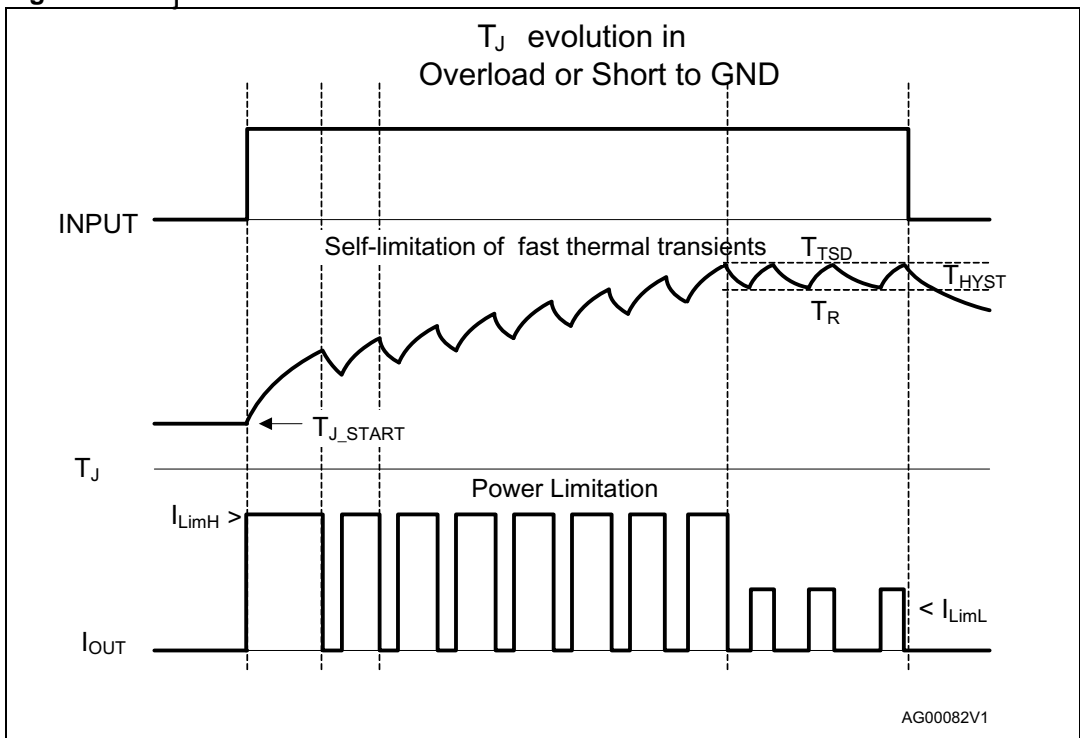


Figure 16.  $T_j$  evolution in overload or short to GND



## 2.5 Electrical characteristics curves

Figure 17. OFF-state output current

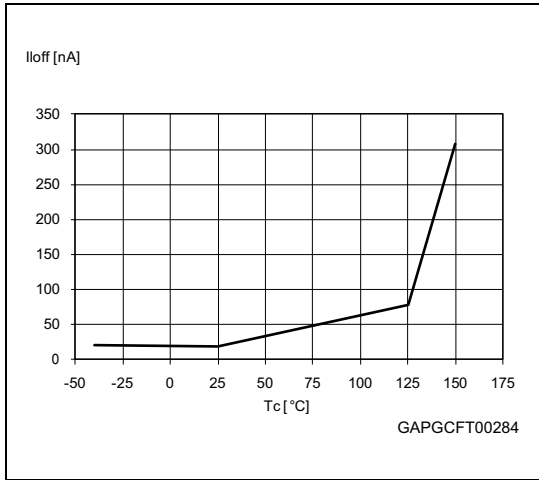


Figure 18. High-level input current

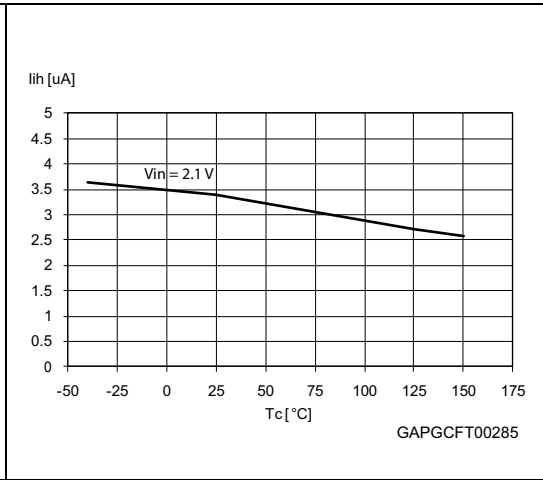


Figure 19. Input voltage clamp

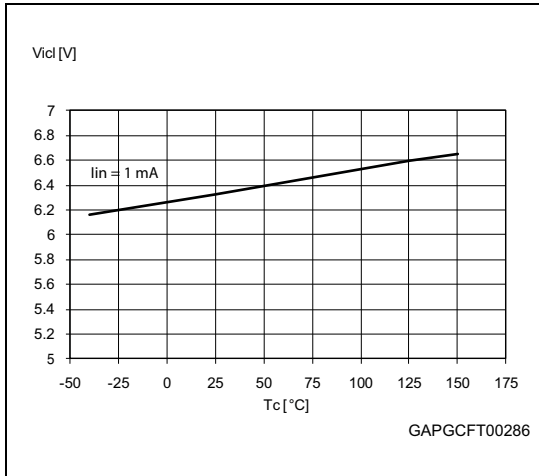


Figure 20. Low-level input voltage

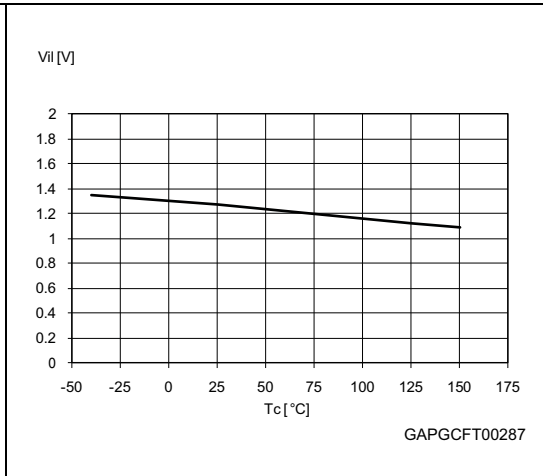


Figure 21. High-level input voltage

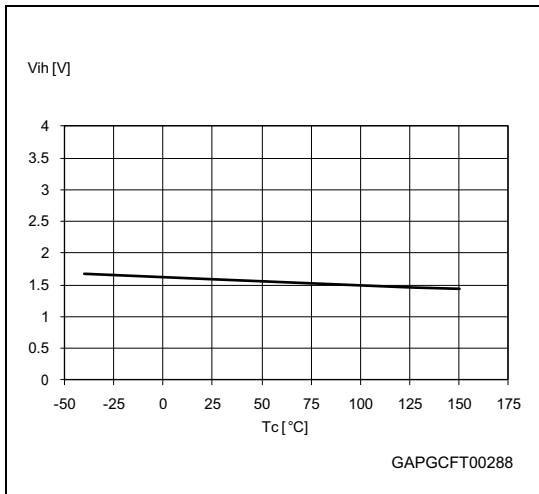


Figure 22. Hysteresis input voltage

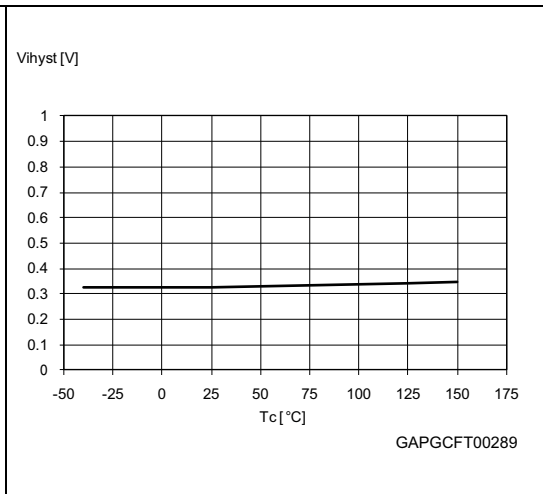


Figure 23. ON-state resistance vs  $T_{case}$

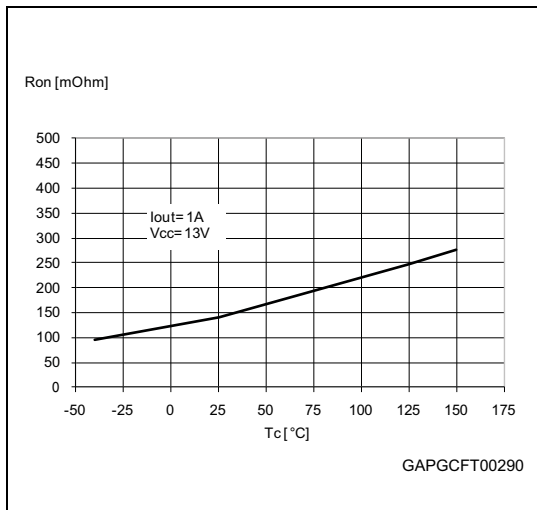


Figure 24. ON-state resistance vs  $V_{CC}$

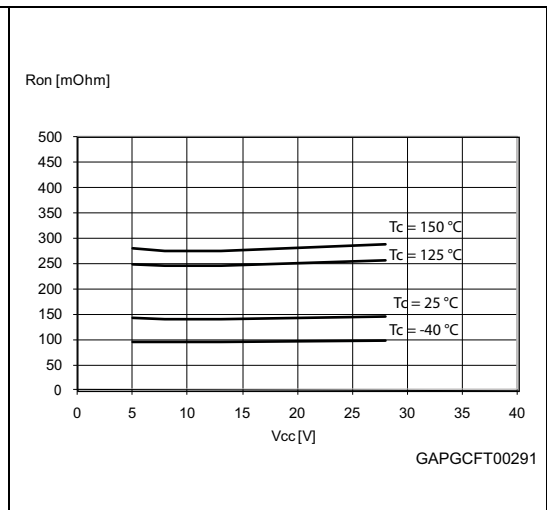


Figure 25. Undervoltage shutdown

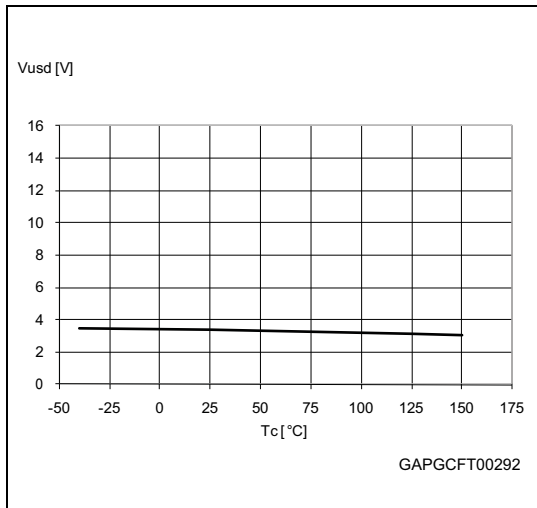


Figure 26. Turn-on voltage slope

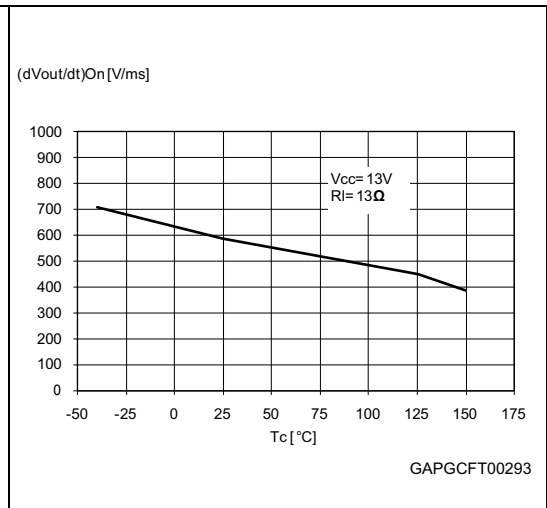


Figure 27.  $I_{LIMH}$  vs  $T_{case}$

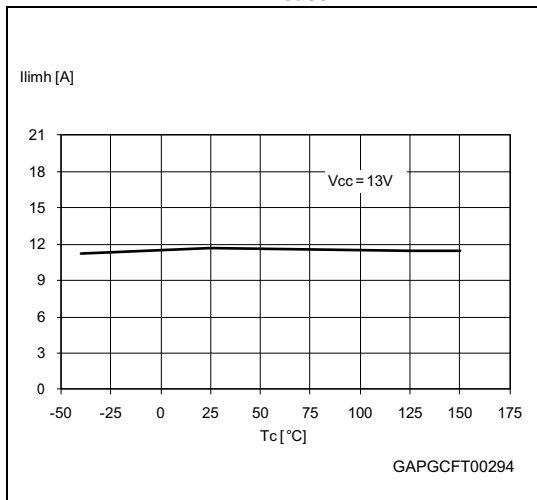
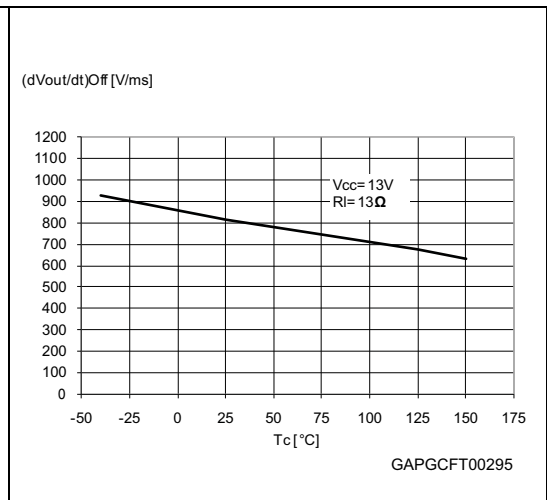
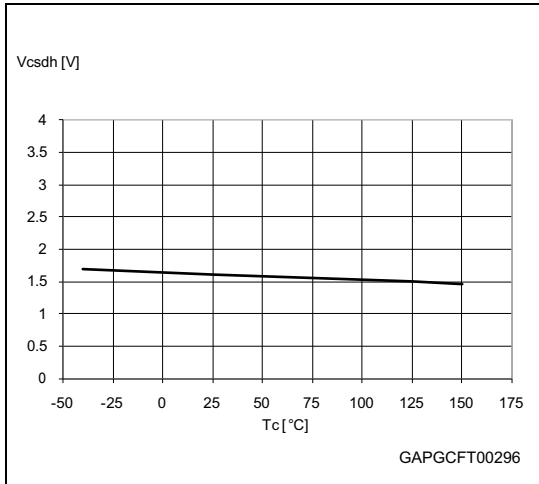


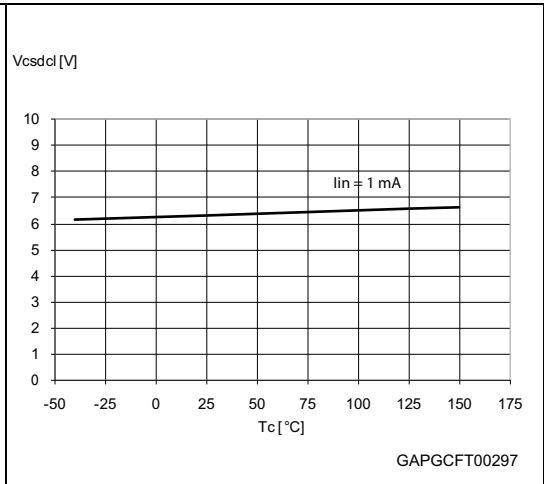
Figure 28. Turn-off voltage slope



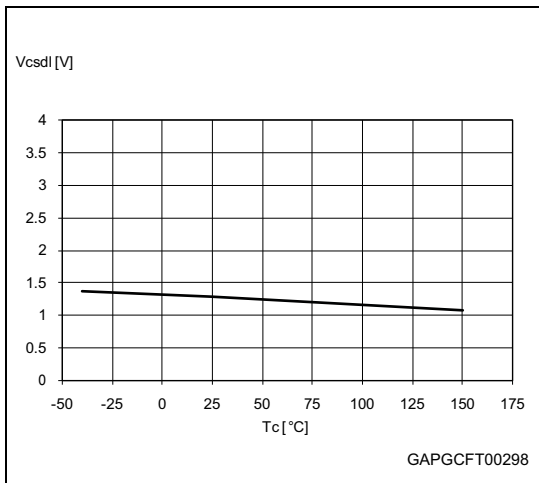
**Figure 29. High-level CS\_DIS voltage**



**Figure 30. CS\_DIS voltage clamp**

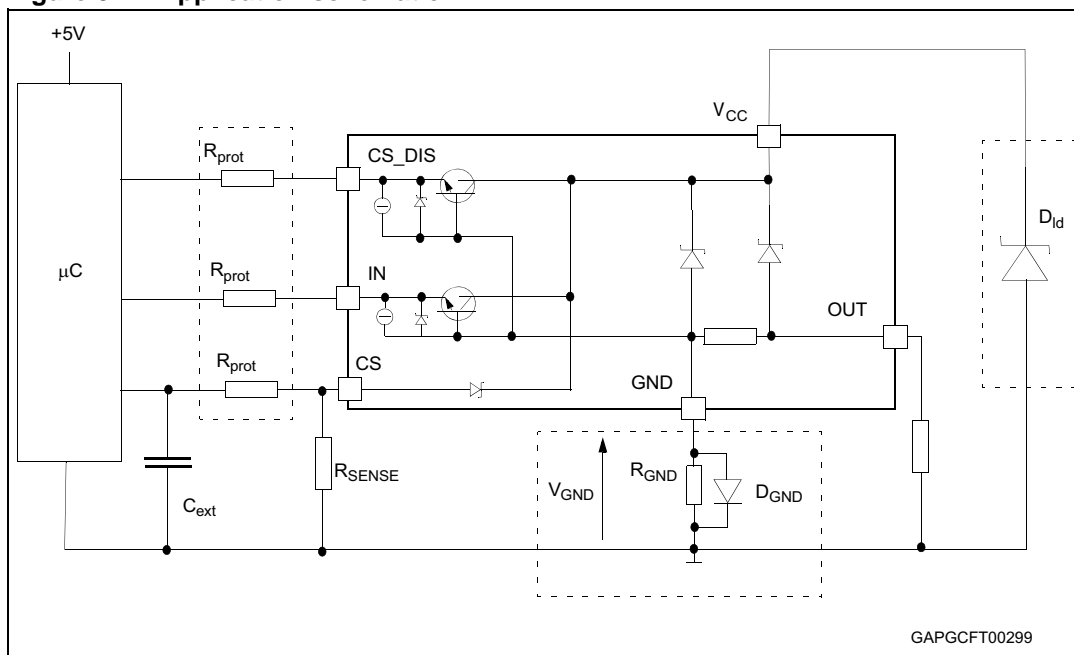


**Figure 31. Low-level CS\_DIS voltage**



### 3 Application information

Figure 32. Application schematic



GAPGCF00299

### 3.1 GND protection network against reverse battery

#### 3.1.1 Solution 1: resistor in the ground line (R\_GND only)

This can be used with any type of load.

The following is an indication on how to resize the R\_GND resistor.

1.  $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R\_GND (when  $V_{CC} < 0$ : during reverse battery situations) is:

#### Equation 1

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R\_GND produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output



values. This shift varies depending on how many devices are ON in case of several high-side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see [Section 3.1.2: Solution 2: a diode \(DGND\) in the ground line](#)).

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\approx 600 \text{ mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

### Equation 2

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100 \text{ V}$ ,  $I_{latchup} \geq 20 \text{ mA}$ ,  $V_{OH\mu C} \geq 4.5 \text{ V}$

$$5 \text{ k}\Omega \leq R_{prot} \leq 180 \text{ k}\Omega.$$

Recommended values:  $R_{prot} = 10 \text{ k}\Omega$ ,  $C_{EXT} = 10 \text{ nF}$ .



### 3.4.1 Short to $V_{CC}$ and OFF-state open-load detection

#### Short to $V_{CC}$

A short-circuit between  $V_{CC}$  and output is indicated by the relevant current sense pin set to  $V_{SENSEH}$  during the device OFF-state. Little or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

#### OFF-state open-load with external circuitry

Detection of an open-load in off-mode requires an external pull-up resistor ( $R_{PU}$ ) connecting the output to a positive supply voltage ( $V_{PU}$ ).

It is preferable that  $V_{PU}$  is switched-off during the module standby mode to avoid an increase in overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull-down resistor ( $R_{PD}$ ) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in OFF-state (see [Figure 33: Current sense and diagnostic](#)).

$R_{PD}$  must be selected in order to ensure  $V_{OUT} < V_{OLmin}$  unless pulled up by the external circuitry:

#### Equation 3

$$V_{OUT}|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2\text{ V}$$

$R_{PD} \leq 22\text{ K}\Omega$  is recommended.

For proper open load detection in OFF-state, the external pull-up resistor must be selected according to the following formula:

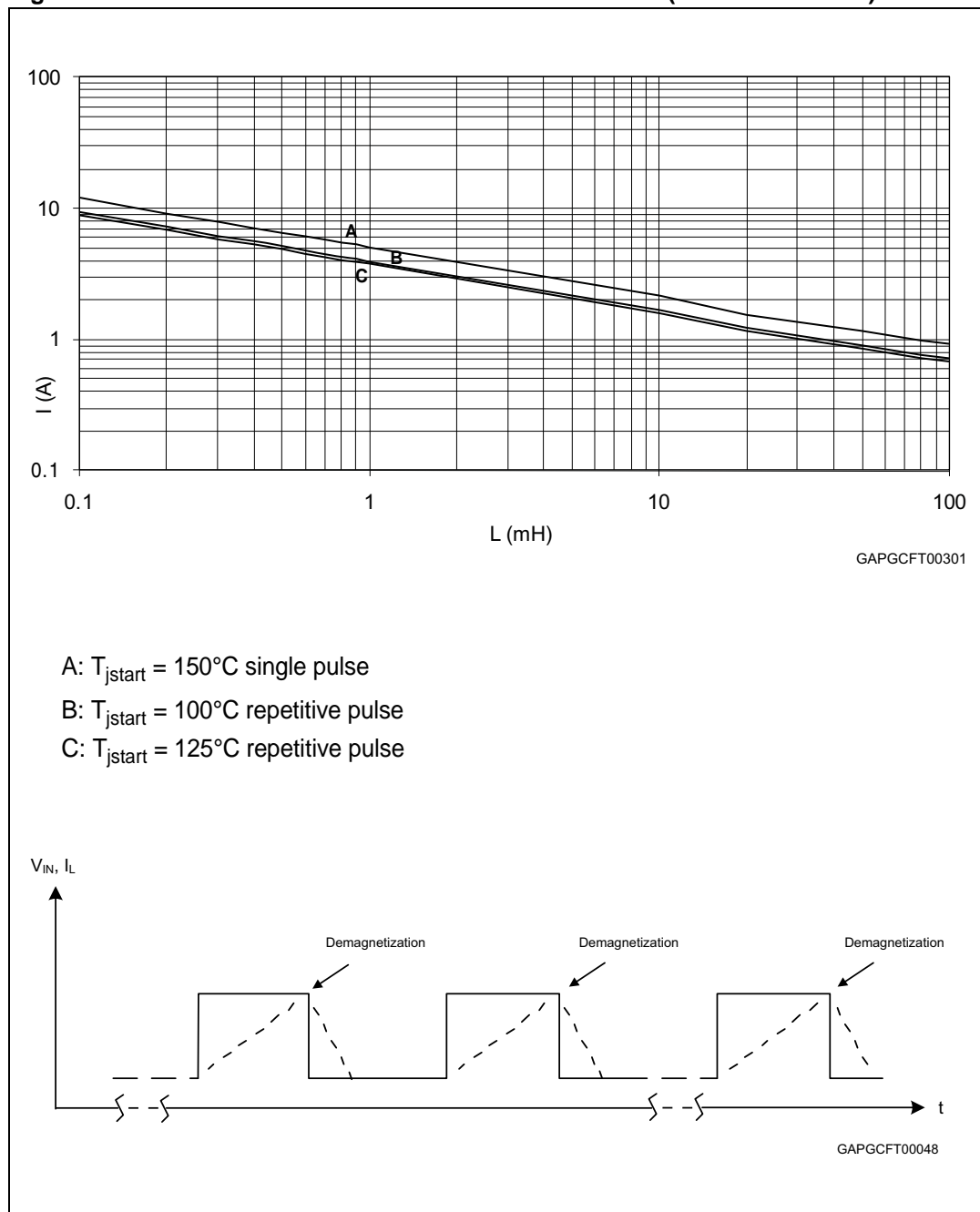
#### Equation 4

$$V_{OUT}|_{Pull-up\_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4\text{ V}$$

For the values of  $V_{OLmin}$ ,  $V_{OLmax}$ ,  $I_{L(off2)r}$  and  $I_{L(off2)f}$  (see [Table 10: Open-load detection \(8 V <  \$V\_{CC}\$  < 18 V\)](#)).

### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

Figure 34. Maximum turn-off current versus inductance (for each channel)<sup>(1)</sup>

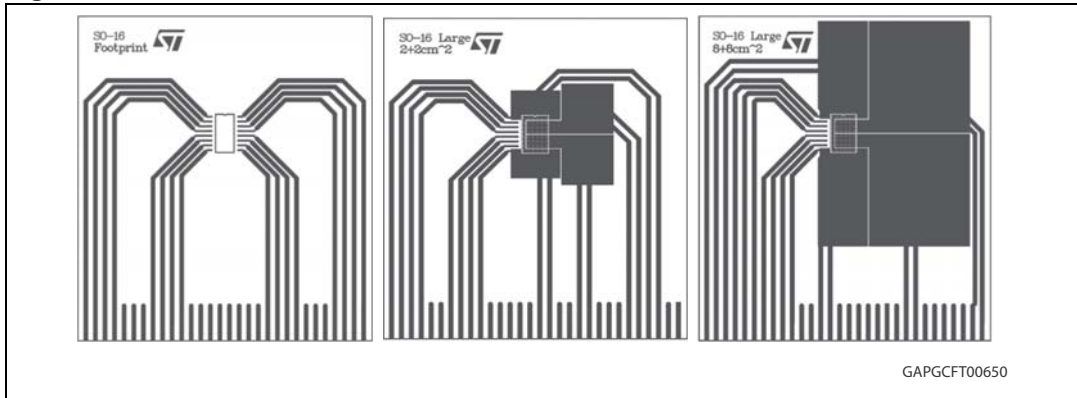


1. Values are generated with  $R_{\theta} = 0\ \Omega$ .  
 In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PC board thermal data

### 4.1 SO-16L thermal data

Figure 35. SO-16L PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double Layers, Thermal Vias, FR4 area 77mm x 86 mm, PCB thickness=1.6mm, Cu thickness = 70 $\mu$ m (front and back side), Copper area from minimum pad lay- out to 24 cm<sup>2</sup> ).

Figure 36.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

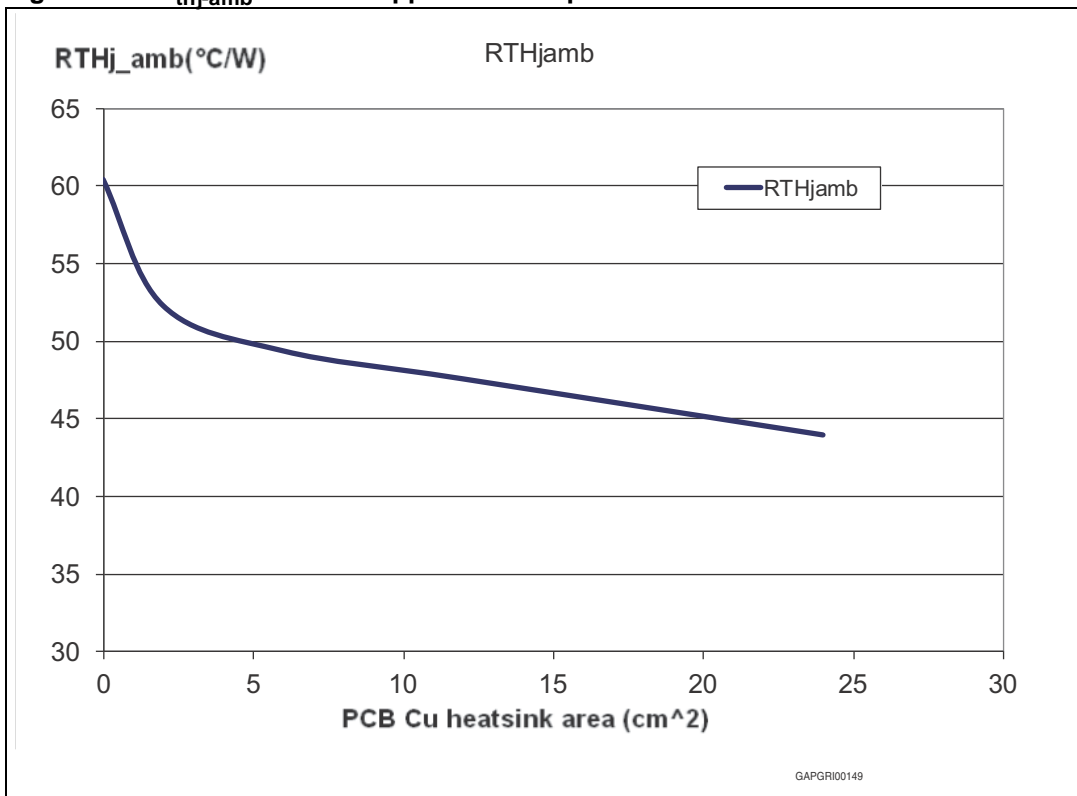


Figure 37. SO-16L thermal impedance junction ambient single pulse

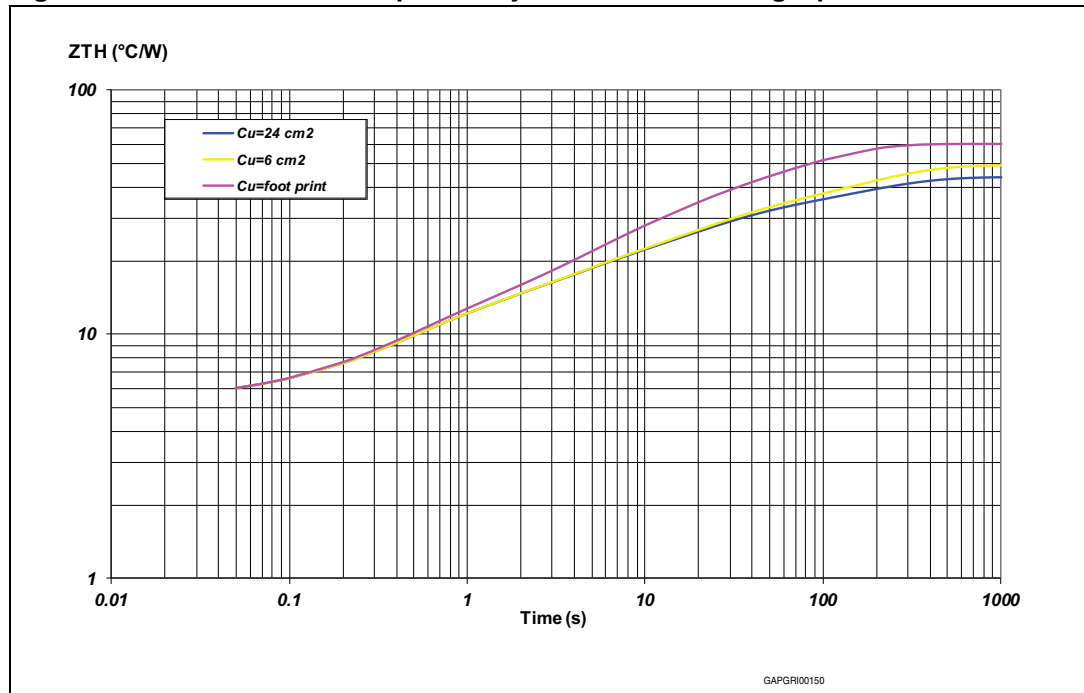
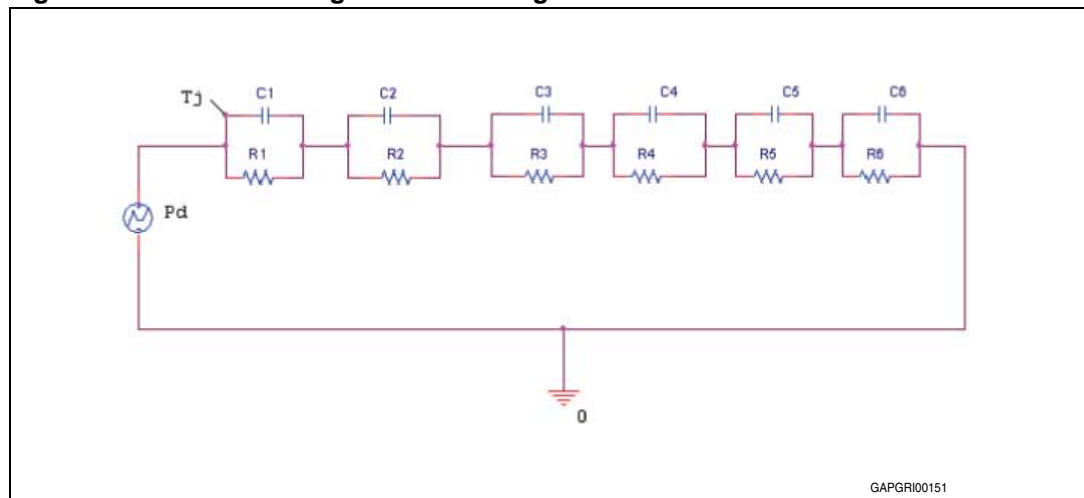


Figure 38. Thermal fitting model of a single channel HSD in SO-16L



Equation 5: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 15. Thermal parameter

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	1.2		
R2 (°C/W)	4.2		
R3 (°C/W)	5		
R4 (°C/W)	8	6	6
R5 (°C/W)	14	13	13
R6 (°C/W)	28	20	14.5
C1 (W.s/°C)	0.0008		
C2 (W.s/°C)	0.002		
C3 (W.s/°C)	0.1		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	1.5	1.5
C6 (W.s/°C)	3	9	12

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.2 Package mechanical data

Figure 39. SO-16L package dimensions

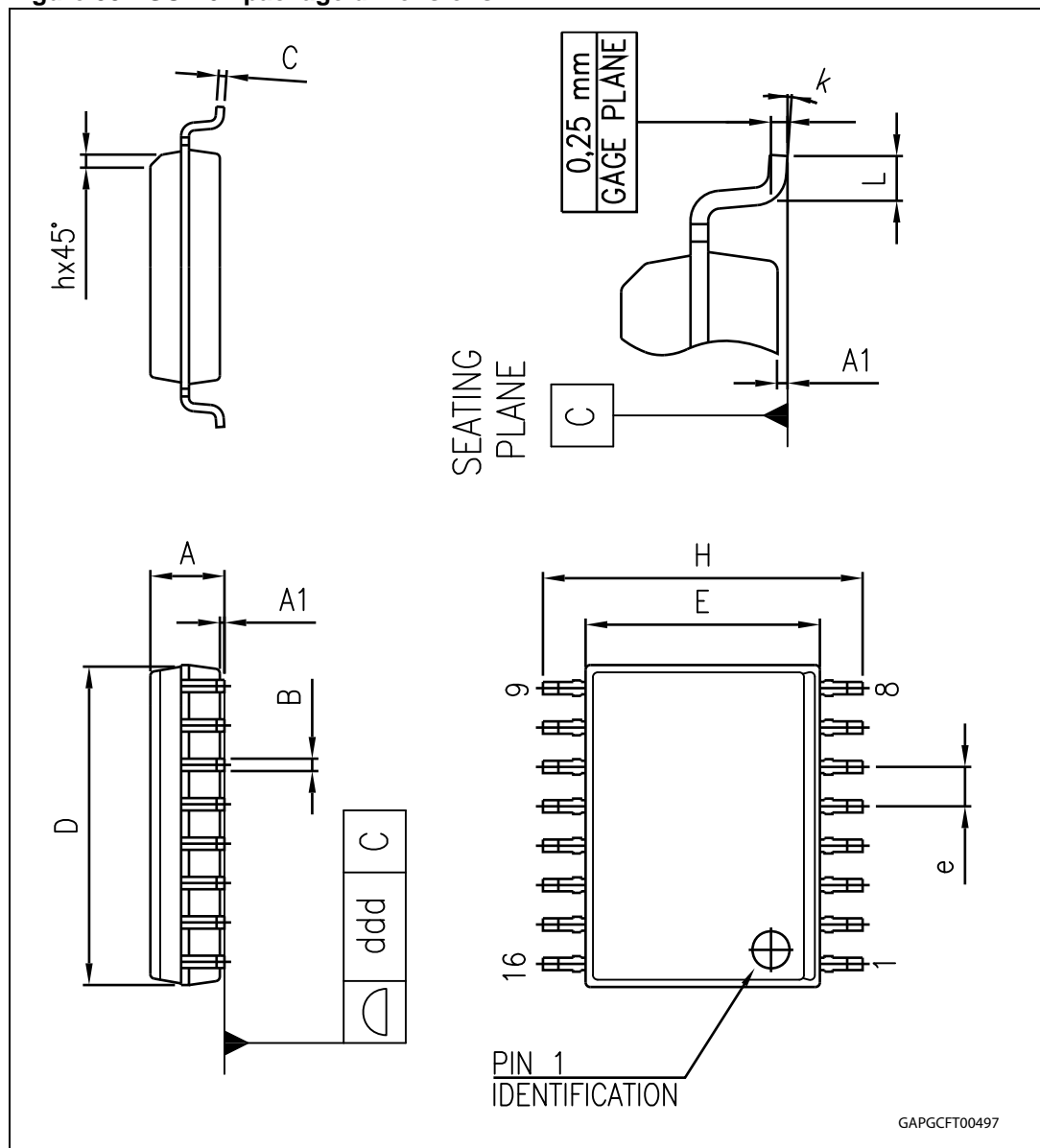




Table 16. SO-16L mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

### 5.3 Packing information

Figure 40. SO-16L tube shipment (no suffix)

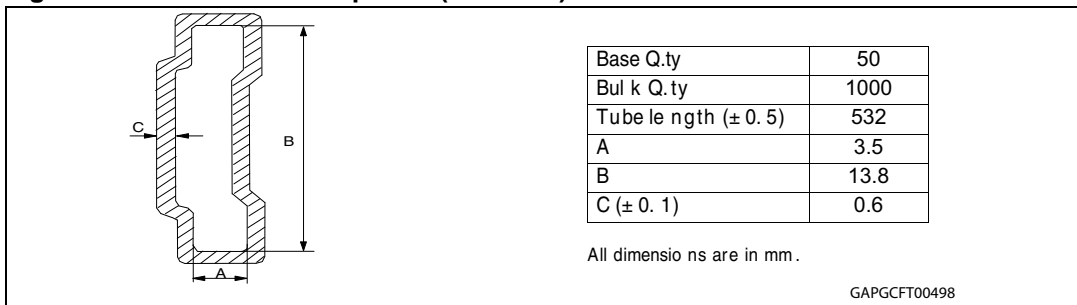
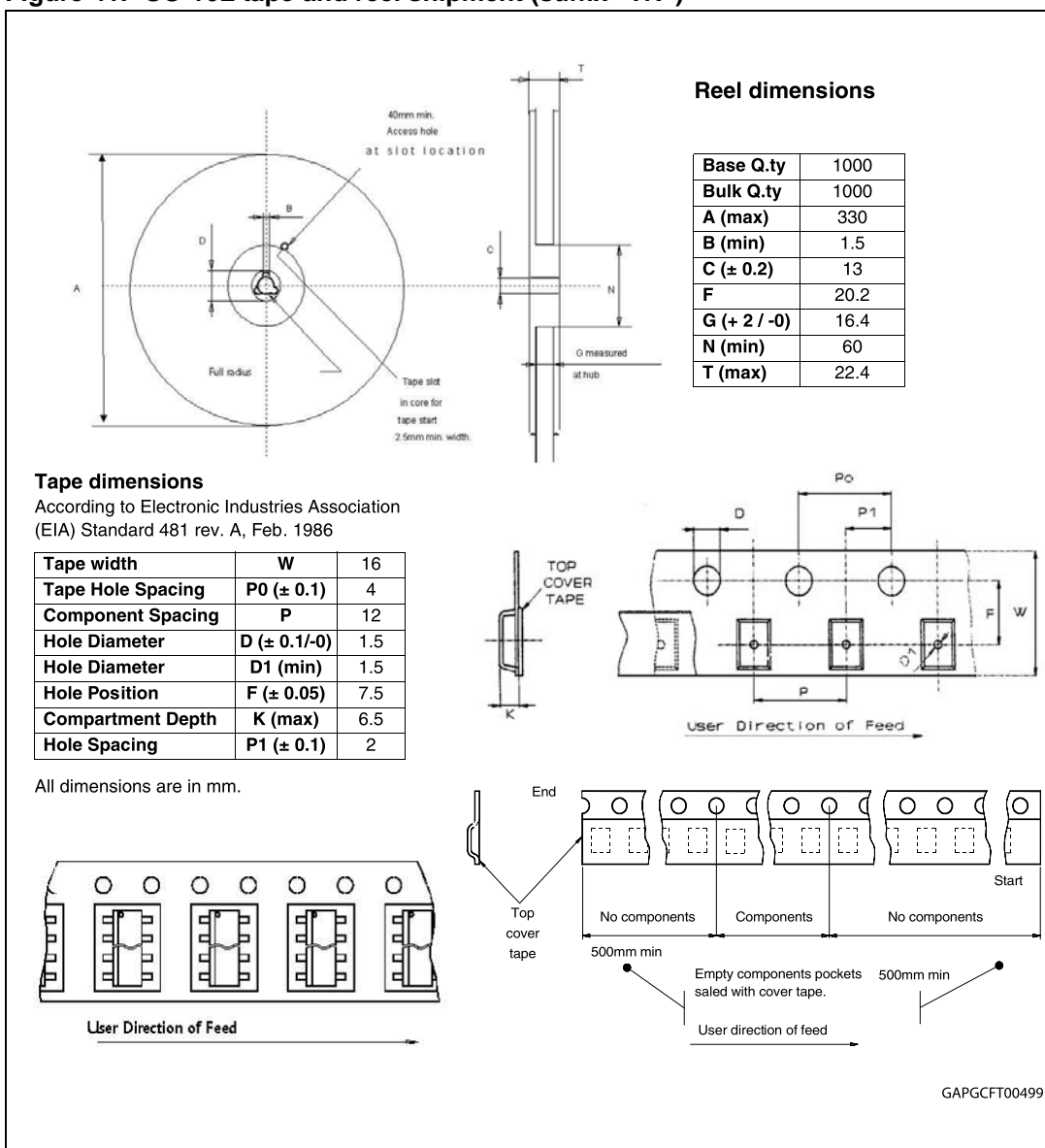


Figure 41. SO-16L tape and reel shipment (suffix "TR")



## 6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16L	VN5E160ASO-E	VN5E160ASOTR-E

## 7 Revision history

**Table 18. Document revision history**

Date	Revision	Changes
14-Dec-2011	1	Initial release.
03-May-2012	2	Update <a href="#">Table 5: Power section</a> Added <a href="#">Section 4: Package and PC board thermal data</a>
25-Jun-2012	3	<a href="#">Table 4: Thermal data:</a> – $R_{thj-pins}$ : removed row – $R_{thj-pcb}$ : added row
18-Sep-2012	4	Updated <a href="#">Table 4: Thermal data</a>
18-Sep-2013	5	Updated disclaimer.

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