PSMN1R4-40YLD

N-channel 40 V 1.4 mΩ logic level MOSFET in LFPAK56 using NextPower-S3 technology

5 May 2014 **Preliminary data sheet**

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in 150 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low Q_{RR}, Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I_{DSS} leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power-SO8) package, copper-clip, solder die attach and qualified to 150 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	40	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 2	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	199	W
T_j	junction temperature			-55	-	150	°C

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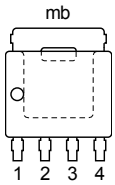
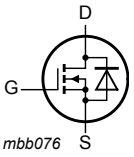
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.12	1.4	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.38	1.85	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 20 V; Fig. 10; Fig. 11		-	13	-	nC
$Q_{G(tot)}$	total gate charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 20 V; Fig. 10; Fig. 11		-	45	-	nC
Source-drain diode							
S	softness factor	I_S = 25 A; V_{GS} = 0 V; dI_S/dt = -100 A/µs; V_{DS} = 20 V; Fig. 14		-	0.85	-	

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-40YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	40	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	199	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	100	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1129	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	100	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1129	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = 74 A; R_{GS} = 50 Ω; unclamped; t_p = 0.23 ms; V_{GS} = 10 V; V_{sup} ≤ 40 V	[2]	-	446	mJ
		V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 25 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; unclamped; t_p = 2.52 ms	[2]	-	1641	mJ

[1] Continuous current is limited by package.
[2] Protected by 100% test

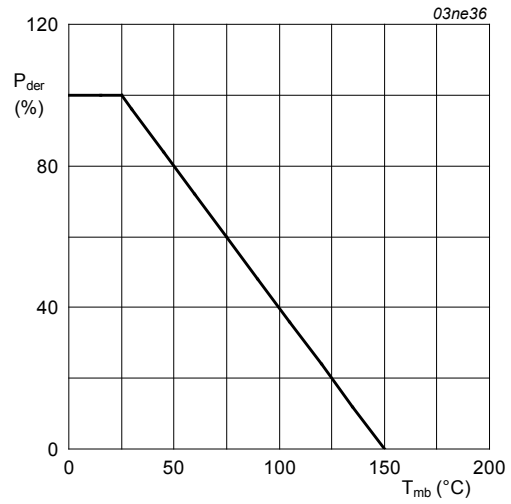
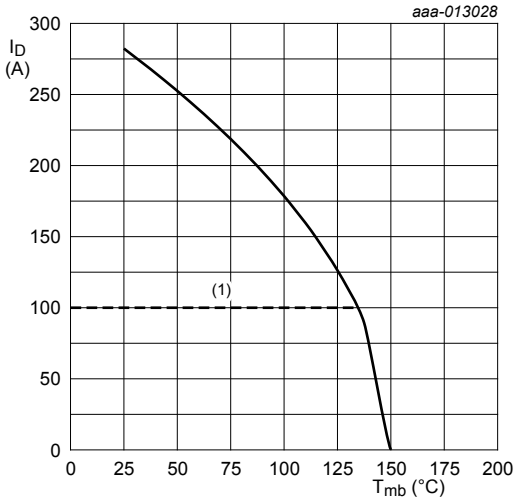


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P(tot)}{P_{tot(25°C)}} \times 100\,\%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

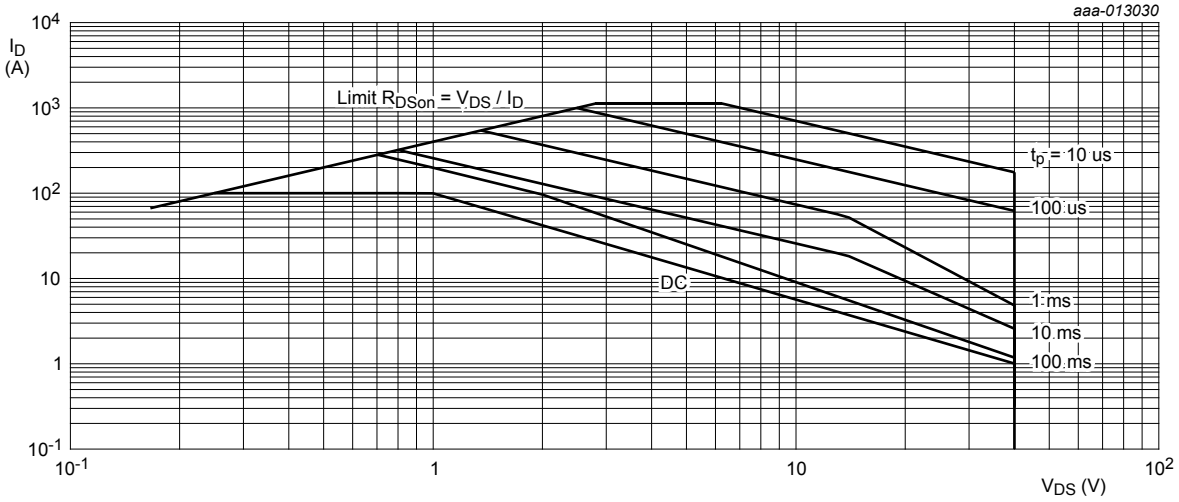


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25°C;\ I_{DM}\ is\ a\ single\ pulse$$

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.56	0.63	K/W

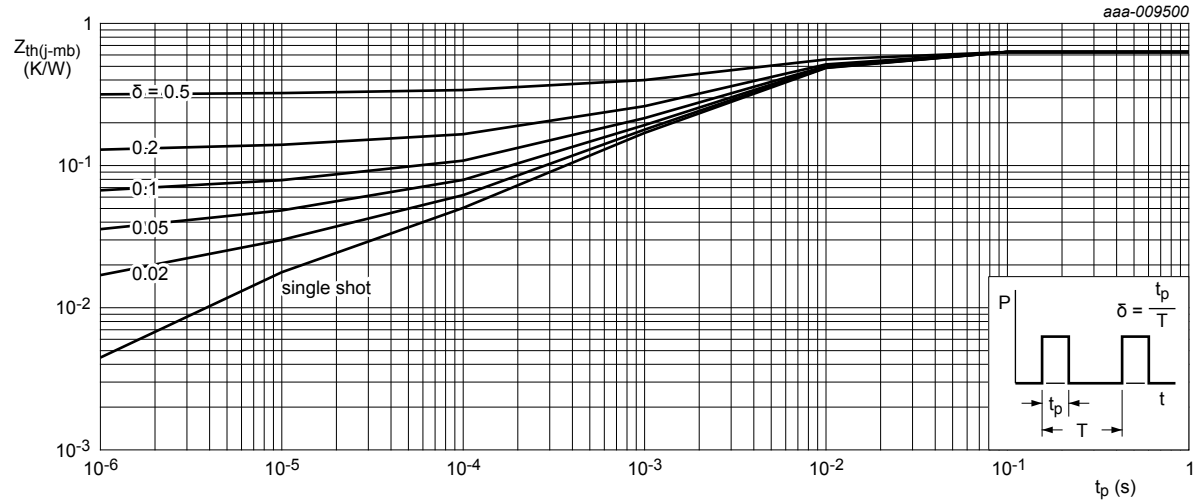


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

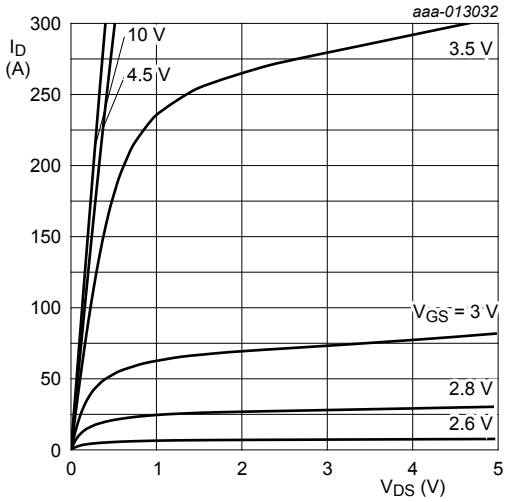
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C		1.05	1.7	2.2	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.12	1.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; Fig. 9; Fig. 8		-	-	2.4	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.38	1.85	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; Fig. 9; Fig. 8		-	-	3.13	mΩ
R_G	gate resistance	f = 1 MHz		-	1.1	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 10; Fig. 11		-	96	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 10; Fig. 11		-	45	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	85	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 10; Fig. 11		-	15	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	13	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 20 V; Fig. 10; Fig. 11		-	2.7	-	V
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 12		-	6661	-	pF
C_{oss}	output capacitance			-	1543	-	pF
C_{rss}	reverse transfer capacitance			-	299	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	39	-	ns
t_r	rise time			-	49	-	ns
$t_{d(off)}$	turn-off delay time			-	47	-	ns
t_f	fall time			-	30	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; T_j = 25 °C		-	50	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 13		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 14		-	47	-	ns
Q_r	recovered charge		[1]	-	61	-	nC
t_a	reverse recovery rise time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 14		-	25.4	-	ns
t_b	reverse recovery fall time			-	21.7	-	ns
S	softness factor			-	0.85	-	

[1] includes capacitive recovery



T_j = 25 °C

Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

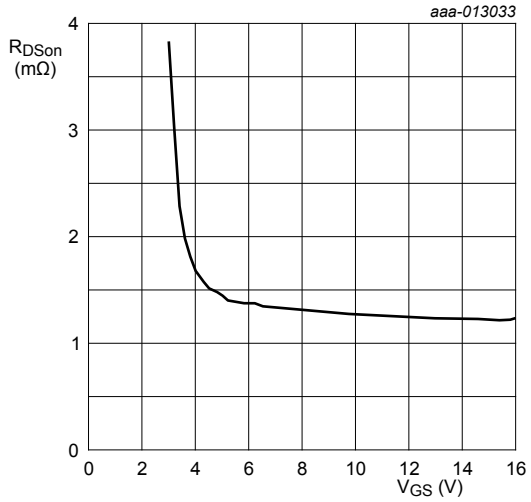


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 25A$

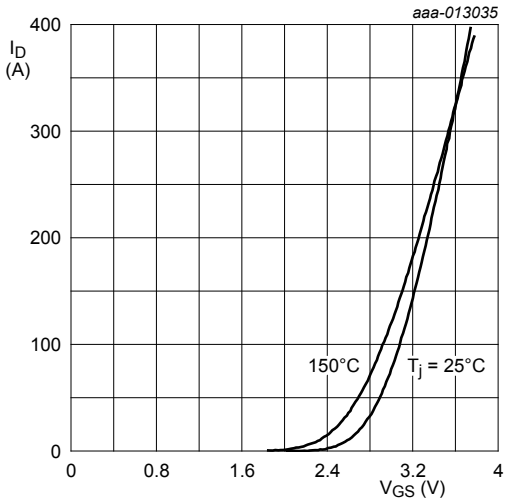
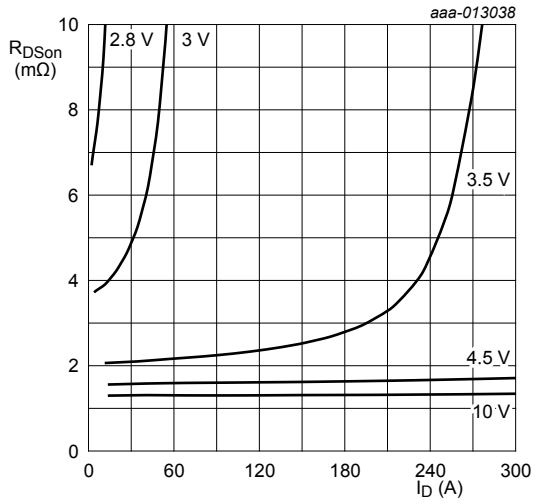


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$



T_j = 25 °C

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

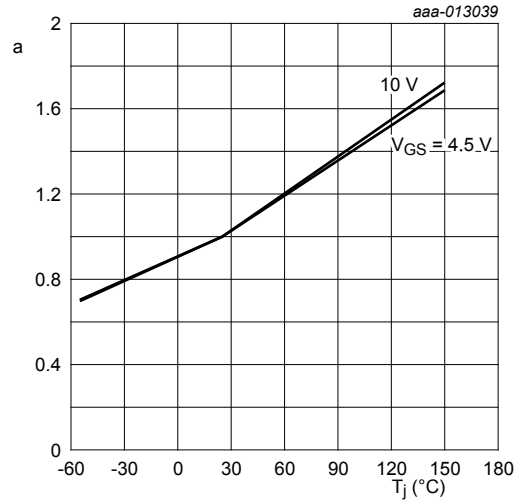


Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

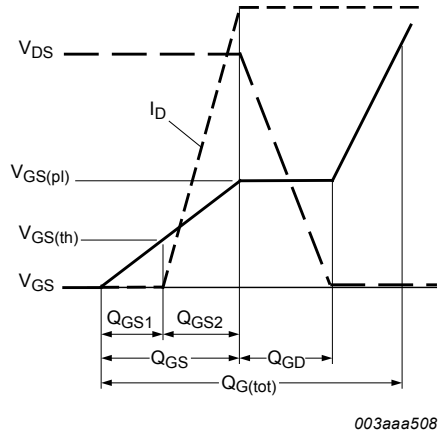


Fig. 10. Gate charge waveform definitions

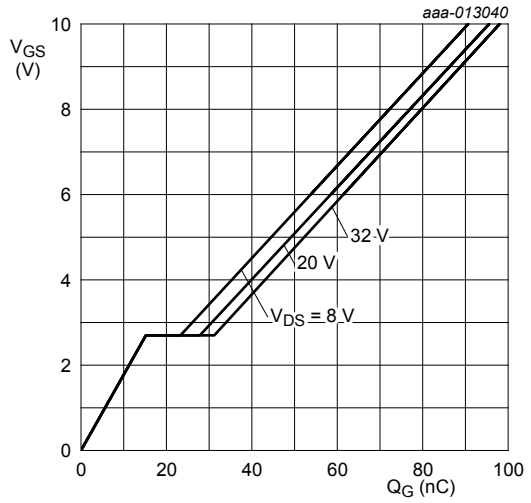


Fig. 11. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25°C;\ I_D = 25A$$

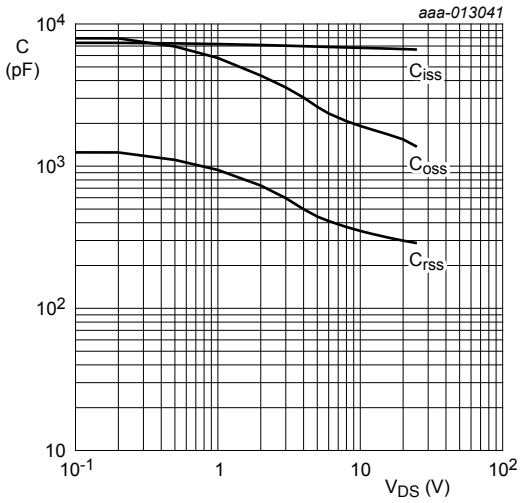


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V;\ f = 1MHz$$

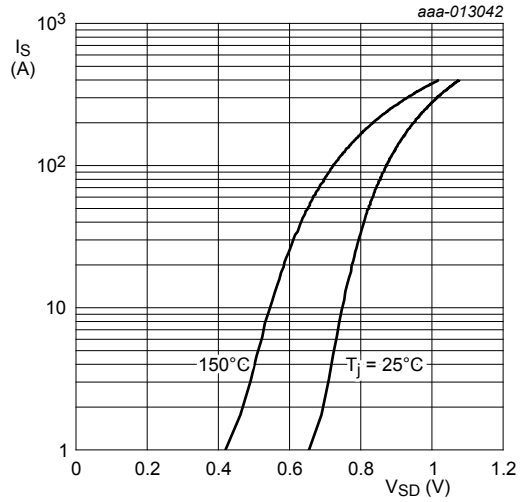


Fig. 13. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0V$$

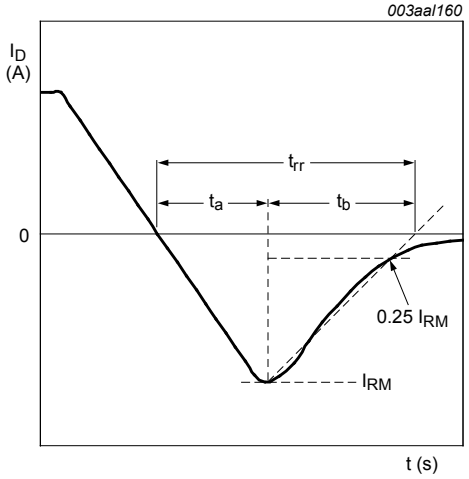
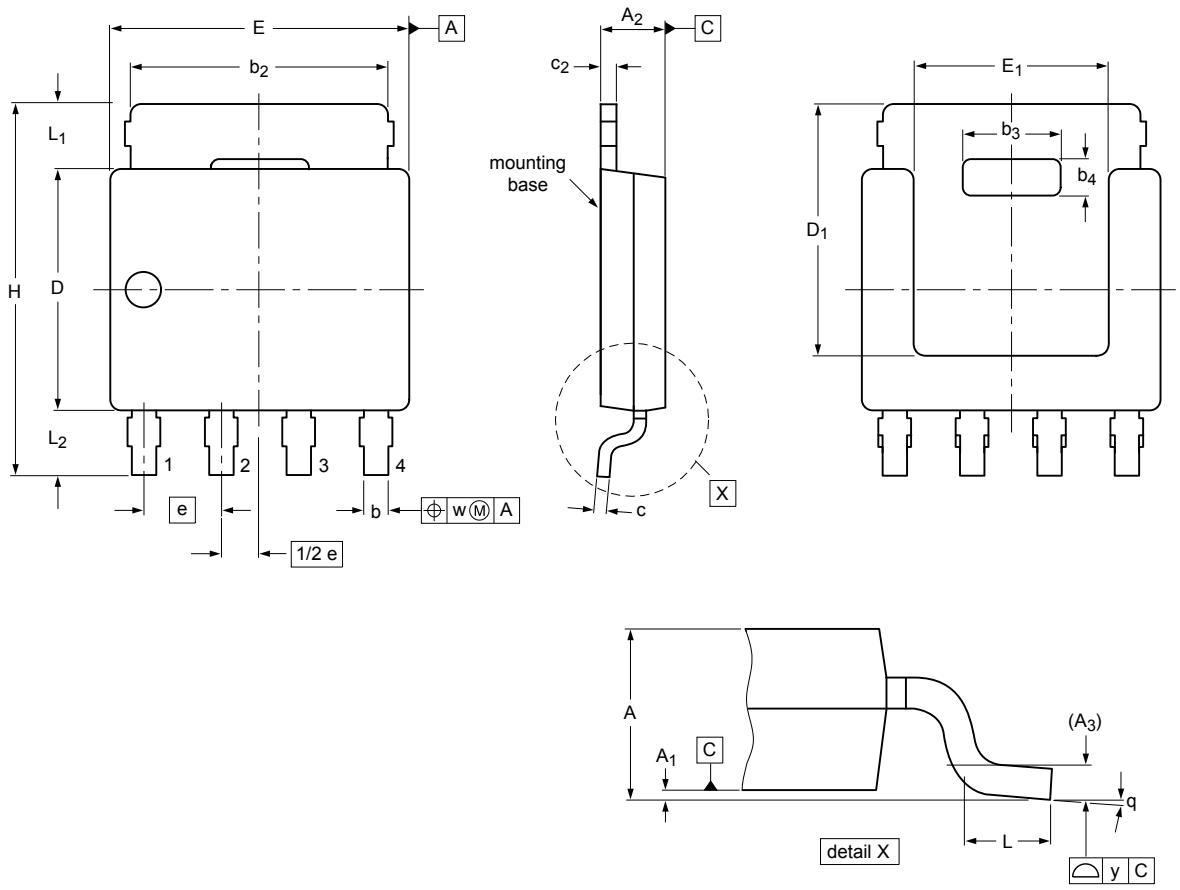


Fig. 14. Reverse recovery timing definition

10. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



θ
8°
0°

Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1{}^{(1)}$	$E^{(1)}$	$E_1{}^{(1)}$	e	H	L	L_1	L_2	w	y
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
	nom				0.25											1.27					0.25	0.1
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 15. Package outline LFPAK56; Power-SO8 (SOT669)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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12. Contents

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