AN1439
Application note

30 W AC-DC adapter with the L6565 quasi-resonant PWM controller

Introduction

This application note describes the evaluation board of the Quasi-resonant (QR) PWM controller L6565 (order code: STEVAL-ISC001V1 - previous code EVAL6565N) and presents the results of its bench evaluation. The board implements a 30 W, single-output (15 V/2 A), wide-range mains input, QR converter that can be used as a reference design for an AC-DC adapter, where good performance is to be achieved at low cost.

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1 Design specification

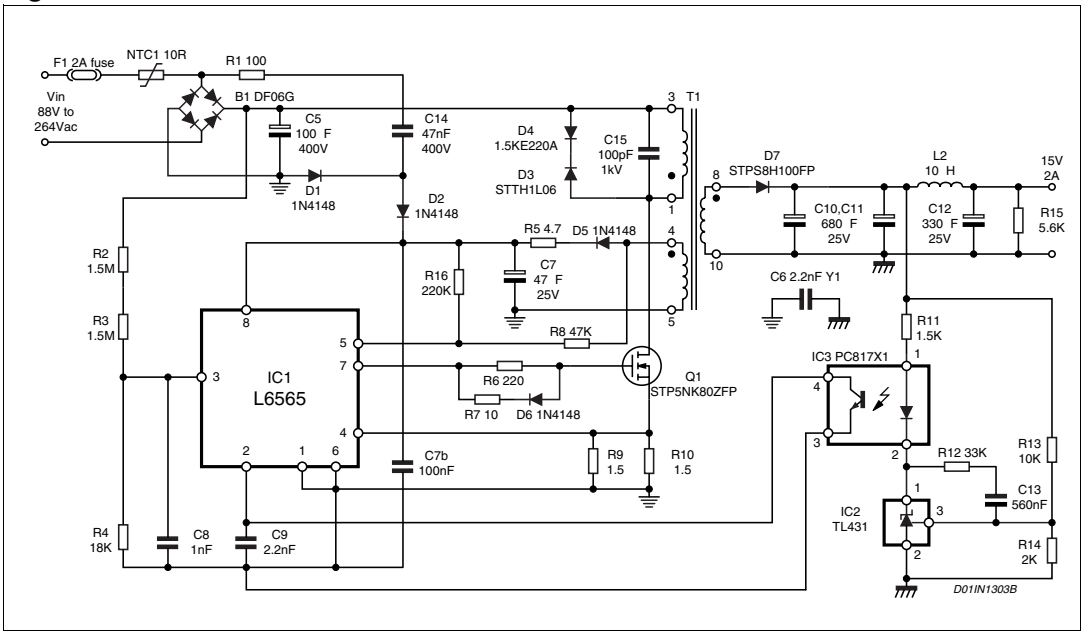
Table 1 summarizes the electrical specifications of the application, *Table 2* provides the BOM and *Table 3* lists the transformer's specifications. The electrical schematic is shown in *Figure 1* and the PCB layout in *Figure 2*.

Table 1. STEVAL-ISC001V1 evaluation board: electrical specifications

Input voltage range (V_{in})	88 to 264 V_{ac}
Mains frequency (f_L)	50/60 Hz
Maximum output power (P_{out})	30 W
Output	– V_{out}= 15 V ± 3%; – I_{out} = 0 to 2 A; – V_{ripple} < 4%
Minimum switching frequency (at 100 V_{DC} input voltage)	60 kHz
Target efficiency (at P_{out}= 30 W, V_{in}= 88÷264 V_{ac})	> 80%
Maximum no-load input power	< 0.75 W (1)

1. Compliant with European Code of Conduct on Efficiency of External Power Supplies, phase 2, 01.01.2003.

Figure 1. STEVAL-ISC001V1 evaluation board: electrical schematic



The electrical specification is typical of an AC-DC adapter for consumer equipment, usually developed as an external unit. As such, it falls within the scope of the European "Code of Conduct on Efficiency of External Power Supplies" and is required to be "efficient" under no-load conditions as specified in *Table 4*. The design target is to fulfill the phase 2 requirements, so as to be up-to-date until the year 2005, when phase 3 sets even more stringent limits. Some hints to upgrade the design according to phase 3 is given in the section *Evaluation board optimization for minimum no-load consumption on page 13*.

Table 2. STEVAL-ISC001V1 evaluation board: bill of material

Symbol	Value	Note
R1	100 Ω	5%
R2, R3	1.5 MΩ	
R4	18 kΩ	
R5	4.7 Ω	
R6	220 Ω	
R7	10 Ω	
R8	47 kΩ	
R9, R10	1.5 Ω	Metallic film
R11	1.5 kΩ	
R12	33 kΩ	
R13	10 kΩ	
R14	2 kΩ	
R15	5.6 kΩ	
R16	220 kΩ	
C5	100 µF	1 kV, Rubycon, MXR series or equivalent
C6	2.2 nF	Y1 class
C7	47 µF	25 V electrolytic
C7b	100 nF	Plastic film or ceramic
C8, C9	2.2 nF	Plastic film or ceramic
C10, C11	680 µF	25 V Rubycon, ZL series or equivalent
C12	330 µF	25 V Sanyo, CG series or equivalent
C13	560 nF	Plastic film or ceramic
C14	47 nF	400 V, polyester
C15	100 pF	1 kV, Y5P, Panasonic or equivalent
L2	10 µH	ELC08D100E, R=44 mΩ, Panasonic or equivalent
T1	558179	See spec in *Table 3*. Supplied by Albe s.r.l. (Tel. +39 363 61493)
B1	DF06G	1A / 600 V bridge, DIP4, GI or equivalent
D1, D2, D5, D6	1N4148	0.3 A / 75 V, glass case, Vishay or equivalent
D3	STTH1L06	1 A / 600 V Turboswitch, F126, ST
D4	1.5KE220A	220 V Transil, CB429, ST
D7	STPS8H100FP	8 A / 100 V Schottky, TO-220FPAC, ST
IC1	L6565	QR PWM controller, DIP8, ST (1)
IC2	TL431CZ	Shunt regulator, TO92, ST
IC3	PC817X1J000F	Optocoupler, Sharp or equivalent

Table 2. STEVAL-ISC001V1 evaluation board: bill of material (continued)

Symbol	Value	Note
Q1	STP5NK80ZFP	1.9 Ω/ 800 V, TO220FP, ST
NTC1	SSN550	NTC 10 Ω, Vishay or equivalent
F1	T2A250V	2 A, 250 V ELU
PCB	---	FR-4, Cu single layer 35 µm, 95.8 x 64.7 mm

1. If not otherwise specified, all resistors are 1%, ¼ W Q1 and D7 are both provided with a 40 °C/W heatsink SK95/25/SA from Fischer Elektronik.

Table 3. STEVAL-ISC001V1: transformer specification (part number 558179, supplied by Albe s.r.l.)

Core	E25/13/7, N67 material or 3C85 or equivalent				
Bobbin	Vertical mounting, 10 pins				
Air gap	≈ 1 mm for an inductance 1-3 of 740 µH				
Leakage inductance	< 20 µH (at 60 kHz) pins 1-3 with 4,5,7,8,9,10 shorted				
Windings Spec & build	**Pin start/end**	**Winding**	**Wire**	**Turns**	**Notes**
	1/2	Pri1	AWG26	40	Innermost winding
	7/9	Sec1	2xAWG23	8	Pins 7-8 will be shorted on the PCB
	8/10	Sec2	2xAWG23	8	Pins 9-10 will be shorted on the PCB
	2/3	Pri2	AWG26	40	Pin2 will be cut for safety
	4/5	Aux	AWG32	8	Evenly spaced

Figure 2. STEVAL-ISC001V1: PCB layout, silk + bottom layer (top view)

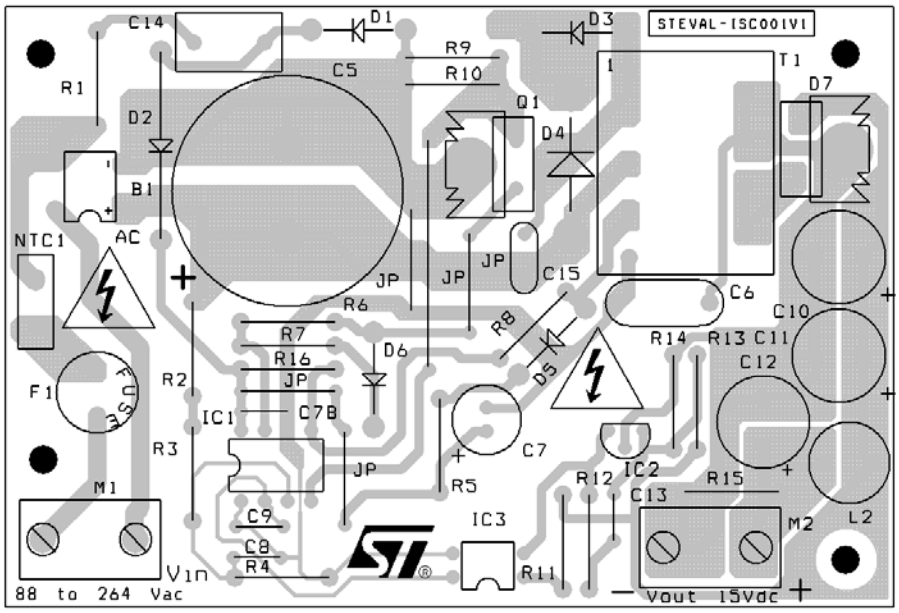


Table 4. Limits set by European code of conduct on efficiency of external power supplies

Rated input power	No-load power consumption		
	Phase 1 01.01.2001	Phase 2 01.01.2003	Phase 3 01.01.2005
≥0.3 W and < 15 W	1.0 W	0.75 W	0.30 W
≥15 W and < 50 W	1.0 W	0.75 W	0.50 W
Š50 W and < 75 W	1.0 W	0.75 W	0.75 W

1.1 Evaluation board functionality

The minimum switching frequency (60 kHz at V_{in} = 100 V_{DC}) has been chosen trading off the transformer's size against frequency-related losses. The reflected voltage has been chosen equal to 150 V, then ZVS is achieved only when the converter operates from the 110 V mains. This value seems to provide a good compromise between capacitive and switching losses at 220 V mains. To provide room for the leakage inductance spike, an 800 V Power MOSFET (STP5NK80ZFP) is used.

To get 150 V reflected voltage, the primary-to-secondary turn ratio is made 1:10, which originates relatively low reverse voltages at the secondary side and allows the use of a Schottky rectifier as the secondary diode (D7).

An STPS8H100FP has been selected. Two design choices have been done to meet the no-load consumption target. First, the converter is started up with a charge pump consisting of D1, D2, C14 and R1 instead of the usual dropping resistor. This circuit, usable thanks to the extremely low startup current of the L6565, provides a typical wakeup time going from 2.8 s at 88 V_{ac} to 0.75 s at 264 V_{ac}, while dissipating less than 50 mW at 264 V_{ac}, i.e. saving about 200 mW as compared to a startup circuit made with a dropping resistor that gives the same wakeup time. Second, the leakage inductance spikes are handled by a Transil clamp (D4, with the addition of D3 to prevent direct conduction during Power MOSFET's ON-time), instead of an RCD clamp, thus saving about 200 mW more. R2+R3 and R4 compensate for the power capability change vs. the input voltage (Voltage Feedforward). Their ratio has been found simply by fixing the high side one (using a high resistance value to keep the losses low) and varying the low side resistance until the converter loses output voltage regulation with the same load at 88 and 264 V_{ac}. A 1nF film capacitor bypasses any noise on pin #3 to ground.

To stay within ± 3% tolerance, the output voltage regulation is done with secondary feedback, using a typical arrangement TL431+optocoupler. R12, C13 and C9 (on the primary side) compensate the voltage loop for stability. Typically, the crossover frequency is 5 kHz with 70° phase margin. A 100 pF low-loss capacitor (C15) has been added across the primary winding to optimize the Power MOSFET's losses at maximum load by a small snubbing effect on the drain voltage rate of rise. The delay between transformer' s demagnetization and the Power MOSFET's turn-on is adjusted by means of R8. The final value of 47 kΩ has been experimentally determined so as to achieve the optimum turn-on point (after the addition of C15).

The converter is fully protected against short-circuit. Under this condition it operates at the frequency of the internal starter (2.5 kHz) and the reflected voltage on the auxiliary winding drops, hence the supply voltage of the L6565 cannot be maintained. This results in

intermittent operation ("hiccup" mode) with low power throughput (< 1 W at 264 V_{ac}). R10 prevents improper Power MOSFET's turn-on, due to signal bouncing on the pin, by pulling up the ZCD pin that would be completely floating otherwise. Additionally, thanks to the 2nd overcurrent level on the L6565's current sense pin, also a short-circuit directly across the secondary winding - or D7 failing short - causes an intermittent operation with an even lower level of power throughput.

Board evaluation: getting started

The AC voltage, generated by an AC source ranging from 88 V_{ac} to 264 V_{ac}, is applied to connector M1 (at the bottom left-hand corner). Should one want to use a high-voltage DC source, remember that the startup charge pump would not work and a dropping resistor would be needed to let the L6565 start.

The 15 VDC output (connector M2) is located close to the bottom right-hand corner and will be connected to the load. If an electronic load is going to be used in CC mode, make sure that the voltage which the load starts sinking current at is > 1 V or use CR mode if this cannot be set, otherwise the board may not start up at maximum load. This happens because V_{out} needs to build up a little in order for the ZCD signal to be large enough to trigger QR operation (refer to *2.: "L6565 Quasi-Resonant Controller" (AN1326)*.) Before that, the converter runs at the frequency of the internal starter, with a much lower power capability that may be easily exceeded if the load starts sinking the maximum current as V_{out} is just above zero. In this case V_{out} gets clamped at a low value, the ZCD signal cannot reach the minimum amplitude required, QR operation cannot take place and the system cannot start up.

Caution: **Like in any offline circuit, extreme caution must be used when working with the application board because it contains dangerous and lethal potentials. The application must be tested with an isolation transformer connected between the AC mains and the input of the board to avoid any risk of electrical shock**.

Board evaluation: bench results and significant waveforms

Table 5, *6*, and *7* summarize the results of some bench evaluations. A number of waveforms under different load and line conditions are shown for the user's reference.

Table 5. STEVAL-ISC001V1: typical performance

Parameter	Value	Unit
Regulated output voltage (at V_{in}= 220 V_{ac}, I_{out}= 2 A)	14.924	V
Minimum operating frequency (at V_{in}= 88 V_{ac}, I_{out}= 2 A)	60	kHz
Maximum operating frequency (at V_{in}= 264 V_{ac}, I_{out}= 1.1 A)	214	kHz
Line regulation (V_{in} = 88 to 264 V_{ac}, I_{out}= 2 A)	1	mV
Load regulation (V_{in}= 88 V_{ac}, I_{out}= 0 to 2 A)	55	mV
High-frequency output voltage ripple (at V_{in}= 88 V_{ac}, I_{out}= 2 A)	10	mV
Line-frequency output voltage ripple (at V_{in}= 88 V_{ac}, f_L = 60 Hz, I_{out}= 2 A)	< 5	mV
Maximum full-load efficiency (at V_{in} = 176 V_{ac}, I_{out} = 2)	85	%
Maximum no-load input power (at V_{in}= 264 V_{ac})	0.6	W

Table 6. STEVAL-ISC001V1: line/load regulation and efficiency

V_{ac} [V]		88	110	132	176	220	264
I_{out} [A]	2.0	V_{out} = 14.925 V η= 82.6 %	V_{out} = 14.924 V η= 84.0 %	V_{out} = 14.924 V η= 84.5 %	V_{out} = 14.924 V η= 85.0 %	V_{out} = 14.924 V η= 84.5 %	V_{out} = 14.924 V η= 83.1 %
	1.5	V_{out} = 14.938 V η= 83.3 %	V_{out} = 14.938 V η= 84.6 %	V_{out} = 14.938 V η= 84.9 %	V_{out} = 14.938 V η= 84.9 %	V_{out} = 14.938 V η= 83.6 %	V_{out} = 14.938 V η= 81.8 %
	1.0	V_{out} = 14.952 V η= 84.0 %	V_{out} = 14.952 V η= 85.0 %	V_{out}= 14.952 V η= 85.0 %	V_{out} = 14.952 V η= 84.0 %	V_{out} = 14.952 V η= 81.7 %	V_{out}= 14.952 V η= 78.7 %
	0.5	V_{out} = 14.966 V η= 83.1 %	V_{out} = 14.966 V η= 83.1 %	V_{out} = 14.966 V η= 83.1 %	V_{out} = 14.966 V η= 81.3 %	V_{out} = 14.966 V η= 77.1 %	V_{out} = 14.966 V η= 72.6 %
	0.2	V_{out} = 14.974 V η= 78.8 %	V_{out} = 14.974 V η= 78.8 %	V_{out} = 14.974 V η= 76.8 %	V_{out} = 14.974 V η= 73.0 %	V_{out} = 14.974 V η= 66.5 %	V_{out} = 14.974 V η= 58.7 %

Table 7. STEVAL-ISC001V1: light-load input power (at P_{out} = 0.5 W)

V_{ac} [V]	88	110	132	176	220	264
Pin [W]	0.9	1.0	1.1	1.2	1.5	1.6

Table 8. STEVAL-ISC001V1: no-load input power

V_{ac} [V]	88	110	132	176	220	264
Pin [W]	0.4	0.4	0.45	0.5	0.55	0.60

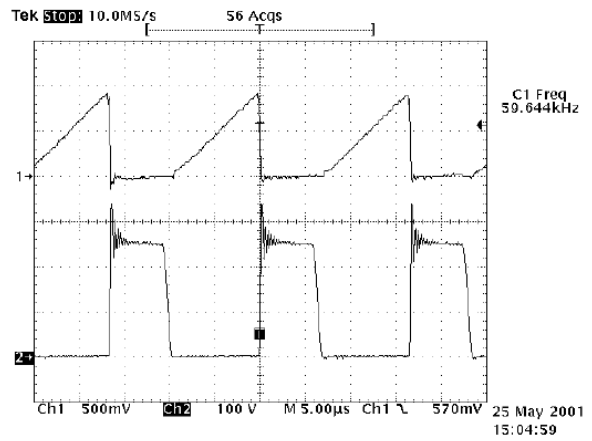
Table 9. STEVAL-ISC001V1: maximum power capability (measured at 0.95·V_{out})

V_{ac} [V]	88	110	132	176	220	264
Pinmax [W]	52.5	57.1	59.5	60.2	57.4	52.3

Table 10. STEVAL-ISC001V1: typical wakeup time

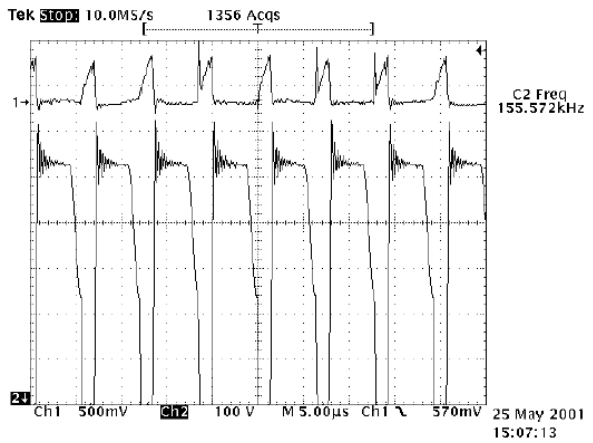
V_{ac} [V]	88	110	132	176	220	264
TWAKE [s]	2.8	2.1	1.65	1.17	0.9	0.75

Figure 3. STEVAL-ISC001V1: full load, V_{in} = 100 V_{DC}



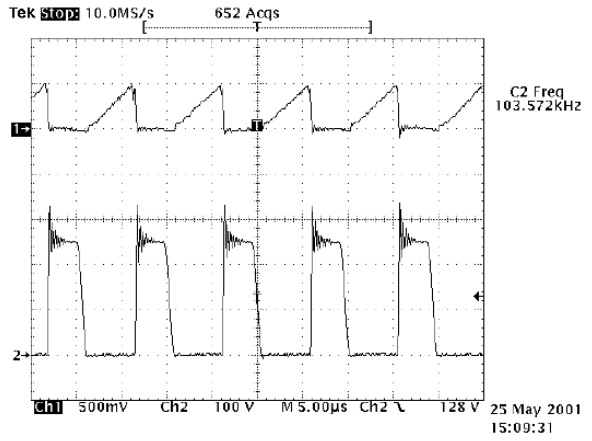
Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 4. STEVAL-ISC001V1: full load, V_{in} = 380 V_{DC}



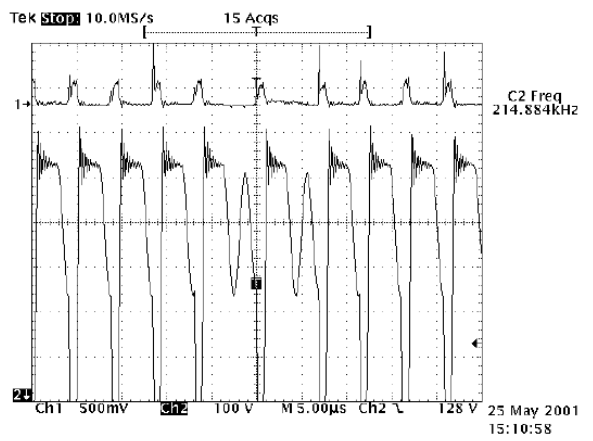
Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 5. STEVAL-ISC001V1: half load, V_{in} = 100 V_{DC}



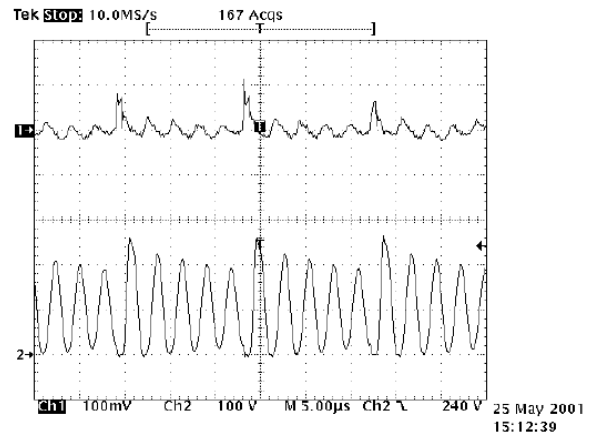
Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 6. STEVAL-ISC001V1: half load, V_{in} = 380 V_{DC} (note uneven skipping)



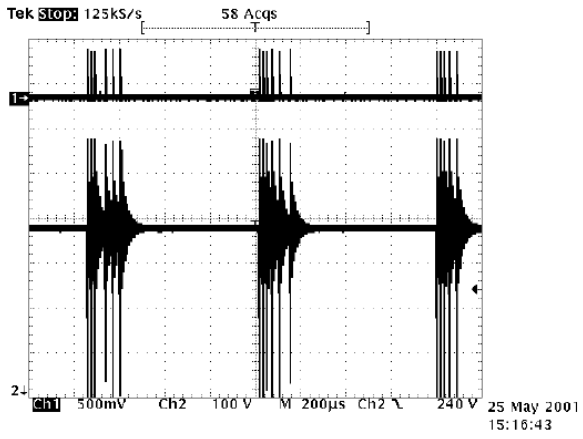
Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 7. STEVAL-ISC001V1: no load, V_{in} = 100 V_{DC}



Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 8. STEVAL-ISC001V1: no load, V_{in} = 380 V_{DC} (burst mode)



Ch2: Q1 drain voltage
Ch1: current sense pin

Figure 9. STEVAL-ISC001V1 full-load output ripple at V_{in} = 110 V_{ac}: high freq.

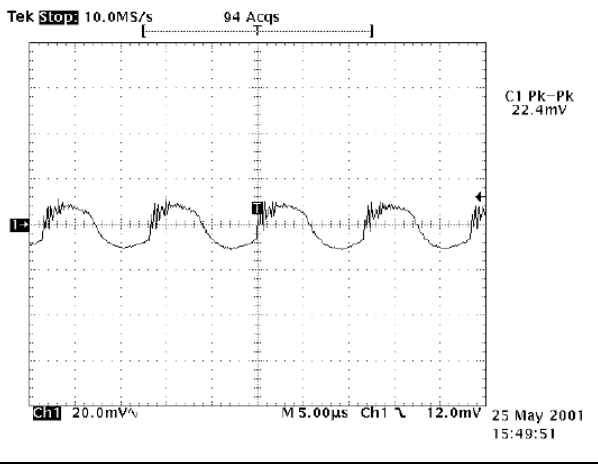


Figure 10. STEVAL-ISC001V1 full-load output ripple at V_{in} = 110 V_{ac}: line freq.

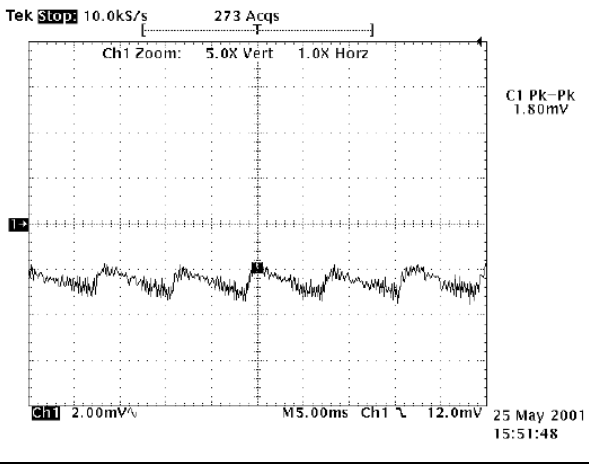
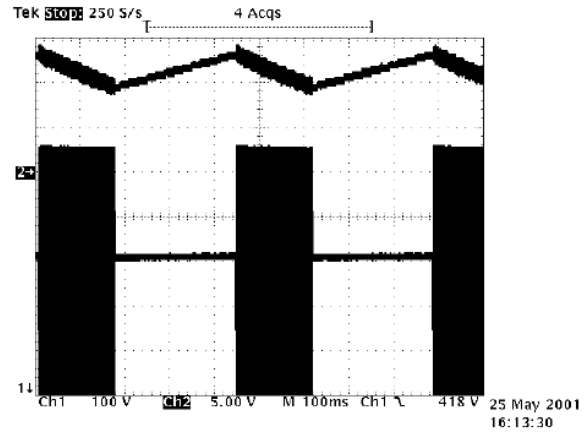
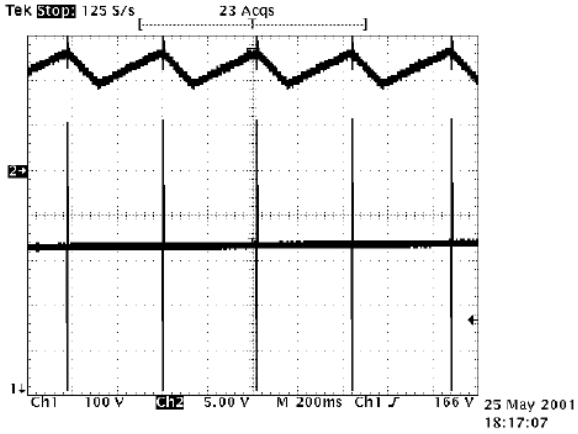


Figure 11. STEVAL-ISC001V1 behavior upon short-circuit on the output. V_{in}=220 V_{ac}



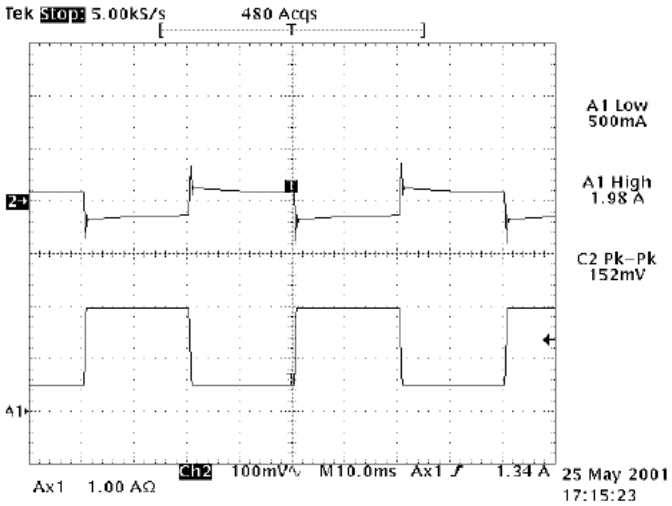
Ch1: Q1 drain voltage
Ch2: L6565 supply voltage

Figure 12. STEVAL-ISC001V1 behavior upon short-circuit on D7. V_{in}=220 V_{ac}



Ch1: Q1 drain voltage
Ch2: L6565 supply voltage

Figure 13. STEVAL-ISC001V1: load transient (at V_{in} = 220 V_{ac}: I_{out} = 0.5 to 2.5 A)



Ch2: Output voltage
Ch2: Load current

Evaluation board optimization for minimum no-load consumption

Additional optimization steps need to be taken in order for the STEVAL-ISC001V1 to fulfill the limits set by the 3rd phase of the European code of conduct on efficiency of external power supplies, which has been active from 01.01.2005. According to this standard, the no-load consumption must be less than 0.5 W at rated input voltage (220 V_{ac} for European mains, the 110 V_{ac} of the US mains is not a concern). To have some margin, it is a common design target to fulfill the specification even at maximum input voltage (264 V_{ac}).

The optimization steps are basically three:

1. Eliminate C15. This slightly hurts efficiency at heavy and moderate load but saves about 100 mW of no-load input consumption at maximum mains.
2. Replace the startup charge pump with a more efficient high-voltage active startup circuit, like the one shown in *Figure 15*. This saves about 40 mW input consumption.
3. The feedback network topology at the primary side should be changed as shown in *Figure 15*. The feedback topology used in the STEVAL-ISC001V1 is such that under no-load conditions the optocoupler draws about 3 mA out of pin COMP, which adds up to the quiescent current of the IC. This additional load causes the V_{cc} voltage to drop so that a small dummy load (R15) is required at the secondary side. With the circuit in *Figure 15*, the operating current of optocoupler is reduced to 1 mA and also the dummy load can be reduced, just the 10 kΩ resistor is used to provide adequate bias current to the TL431. The input consumption is reduced by about 100 mW.

Figure 14. High-voltage active startup circuit

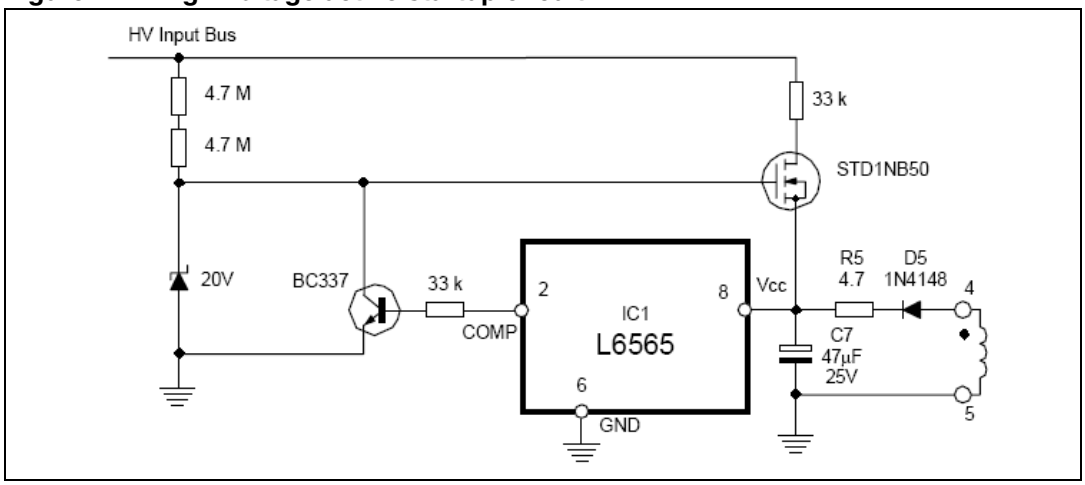


Figure 15. Low-consumption feedback network

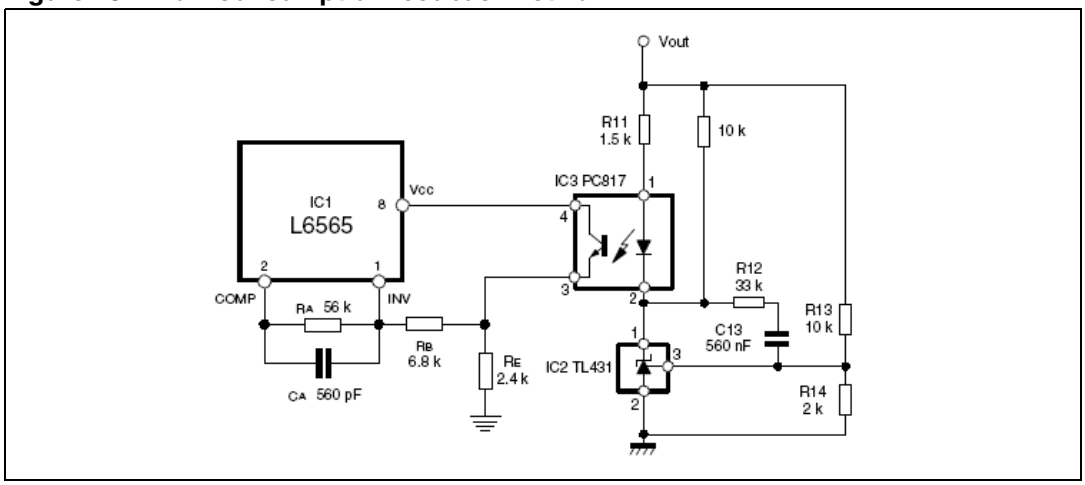


Table 11. STEVAL-ISC001V1 modified as per optimization steps 1 to 3: no-load input power measurements

V_{ac} [V]	88	110	132	176	220	264
Pin [W]	0.3	0.3	0.3	0.35	0.4	0.4

To gain more design margin the following tips could be considered:

a) Increase R2, R3 and R4: by using 4.7 MΩ for R2 and R3 and 56 kΩ for R4, the input consumption is reduced by 30 mW.

b) Reduce the parasitic capacitance of the drain node by using a smaller or lower voltage rating Power MOSFET. The price to pay might be more dissipation at full load and a larger heatsink. For example the 600V -rated Power MOSFET with the closest $R_{DS(on)}$ to that of the STP5NK80ZFP, the STP4NK80ZFP, has a C_{oss} which is only 66%, which allows saving about 15 mW. The full-load losses are essentially the same.

c) Another way to reduce the drain parasitic capacitance is to minimize the parasitic capacitance of the primary winding. To achieve a low capacitance, split the primary winding (this goes in favor of a low leakage inductance too) and wind first the half whose end is to be connected to the drain of the Power MOSFET. In case of multiple layer winding, which exhibits higher capacitance, it is useful to embed one layer of isolation in between. This, however, tends to increase leakage inductance and therefore should be done with care. Slotted bobbins are also very effective to this end but they tend to increase leakage inductance too.

2 References

1. "L6565 Quasi-Resonant SMPS Controller" datasheet
2. "L6565 Quasi-Resonant Controller" (AN1326).

3 Revision history

Table 12. Document revision history

Date	Revision	Changes
28-10-2005	5	First Issue in EDOCS dms
10/02/2006	6	– Obsolete parts replaced with newest ones. – Changed C14 and D4 values. – Updated *Table 10*.
12-Mar-2008	7	– *Figure 1*, *2* modified – EVAL6565N replaced by STEVAL-ISC001V1

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