A/D MCU

General Description

The MCU provides cost effective for ADC application。 It designs by LSI high technology with low power process。

Features

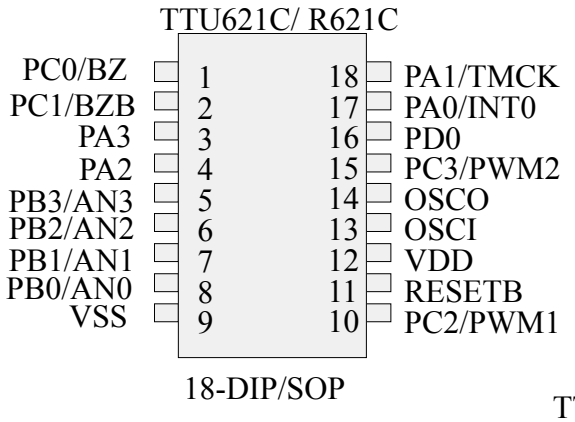
- ✧ Use 4-bit CPU core
- ✧ Operating Voltage：
  - (TTU621C/TTU622C)Mask type：2.2v-5.5v (fsys=4Mhz)，3.3v-5.5v (fsys=8Mhz)
  - (TTR621C/TTR622C)OTP type：2.2v-5.5v (fsys=4Mhz)，3.3v-5.5v (fsys=8Mhz)
- ✧ Oscillator type （Mask Option）
  - Resonator oscillator 1M-8Mhz(external capacitor)
  - Built-in RC oscillator external resistor，internal capacitor (400K-4Mhz)
  - External clock input(OSCH)
  - (TTU622C/TTR622C)External 32768Hz crystal oscillator
  - Internal RC oscillator 16Khz
- ✧ (TTU621C/TTR621C)user ROM 2K*16，RAM 128*4，(TTU622C/TTR622C)user ROM 4K*16，RAM 256*4
- ✧ Built-in (TTU621C/TTR621C) 2 stacks，(TTU622C/TTR622C) 4 stacks
- ✧ Built-in a time base with internal interrupt
- ✧ Built-in watch dog timer
- ✧ Built-in Programming frequency divider function for buzzer function
- ✧ Stop function and sleep function feature to reduce power consumption
- ✧ (TTU621C/TTR621C)Built-in 1 set 8-bit Timer/counter with auto-reload
- ✧ (TTU622C/TTR622C)Built-in 2 set 8-bit Timer/counter with auto-reload (share with 16-bit Timer/counter)
- ✧ (TTU621C/TTR621C)Built-in 1 set 8-bit PWM
- ✧ (TTU622C/TTR622C)Built-in 2 set 8-bit PWM
- ✧ Low voltage reset function
- ✧ (TTU621C/TTR621C)Built-in 8 bits ADC 4 channels (with internal interrupt function，conversion time is 72us @4Mhz) (8-bit resolution and 7-bit accuracy)
- ✧ (TTU622C/TTR622C)Built-in 8 bits ADC 8 channels (with internal interrupt function，conversion time is 64us @4Mhz) (8-bit resolution and 7-bit accuracy)
- ✧ (TTU621C/TTR621C)13 I/O ports，(TTU622C/TTR622C)23 I/O ports
- ✧ Provide external reset pin and internal reset pin
- ✧ Provide (TTU621C/TTR621C)18-pin DIP/SOP，(TTU622C/TTR622C) 24/28-pin SDIP/SOP

Application

- Electric appliances controller
- Consumer products
- Toy controller

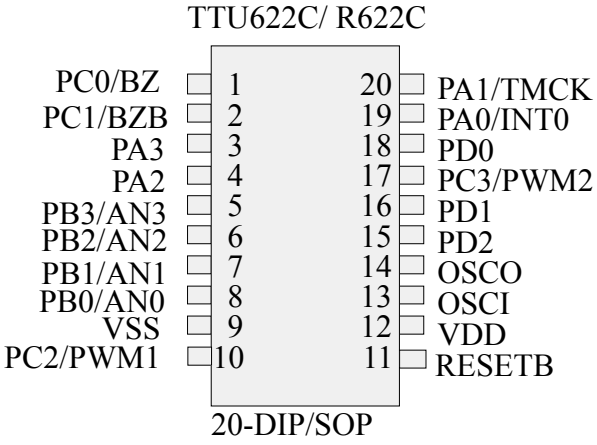
.Pin Assignment

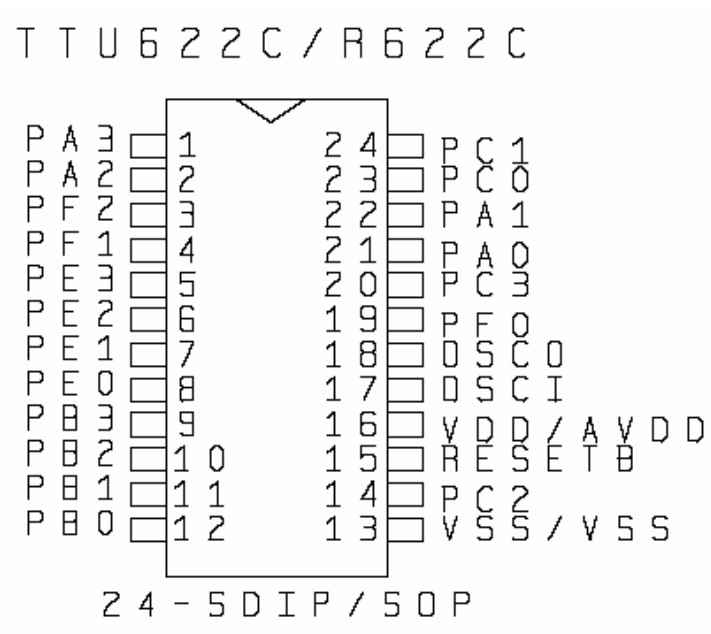
(TTU621C/TTR621C)

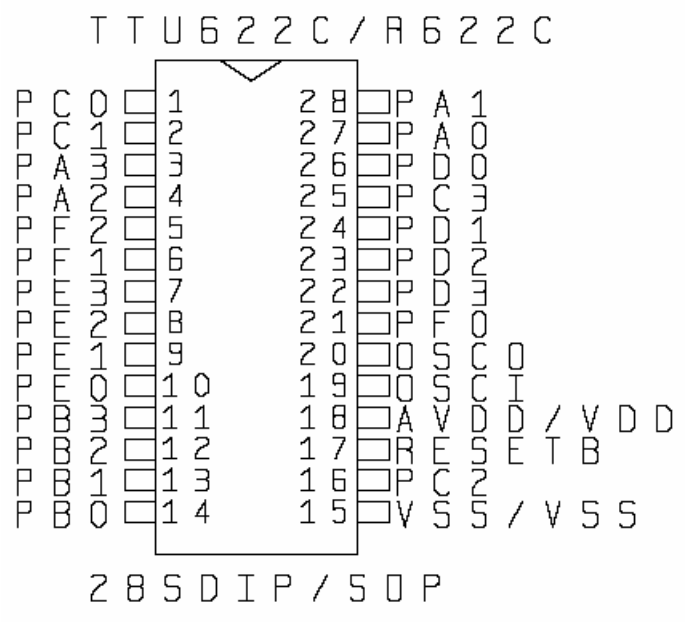


TTU621-F1

(TTU622C/TTR622C)






TTU622C/R622C
PC0 1
PC1 2
PA3 3
PA2 4
PF2 5
PF1 6
PE3 7
PE2 8
PE1 9
PE0 10
PB3 11
PB2 12
PB1 13
PB0 14
28 PA1
27 PA0
26 PD0
25 PC3
24 PD1
23 PD2
22 PD3
21 PF0
20 OSCO
19 OSCI
18 AVDD/VDD
17 RESETB
16 PC2
15 VSS/VSS
28SDIP/SOP

.Pin Description

(TTU621C/TTR621C)

Name	I/O	Description	pins
PA0/INT0	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, there can be selected as external interrupt input function	1
PA1/ TMCK	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, there can be selected as external wake-up function or external clock input for Timer/Counter1 circuit	1
PA2-PA3	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, there can be selected as external wake-up function	2
PD0	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, there can be selected as external wake-up function	1
RSTB	I	External reset pin, low active	1
VSS	P	Digital ground pin	1
VSS	P	Analog ground pin	1
PB0/AN0 PB1/AN1 PB2/AN2 PB3/AN3	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, with wake up function selected by software programming(falling edge trigger)。There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically。	4
PC0/BZ PC1/BZB	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, with wake up function selected by software programming(falling edge trigger)。Ther can be selected as buzzer function select by software programming。	2
PC2/PWMA1 PC3/PWMA2	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @3v selected by software, with wake up function selected by software programming (falling edge trigger)。Ther can be selected as PWM function select by software programming。	2
VDD	P	Analog power pin	1
VDD	P	Digital power pin	1
OSCI	I	Crystal type: crystal input RC type: RC oscillator input External clock input	1
OSCO	O	Crystal type: crystal output RC type: Oscillator frequency divided by 2 is available on OSCO to synchronize other logic or used for testing purpose.	1
		Total Pin	20

Note – Please notice input pin pull low/high or output pin driving current capacity in this table。

(TTU622C/TTR622C)

Name	I/O	Description	pins
PA0/INT0	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, there can be selected as external interrupt input function	1
PA1/ TMCK	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, it can be selected as external wake-up function or external clock input for Timer/Counter1 circuit	1
PA2/RTCI PA3/RTCO	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, there can be selected as external wake-up function。Ther can be selected as 32768Hz crystal oscillator function programed by mask option	2
RSTB/ VPP	I	External reset pin, hysteresis input, without pull high, low active	1
VSS	P	Digital ground pin	1
VSS	P	Analog ground pin	1
PB0/AN0 PB1/AN1 PB2/AN2 PB3/AN3	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger)。There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically。	4
PE0/AN4 PE1/AN5 PE2/AN6 PE3/AN7	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger)。There can be selected as an A/D input, the I/O function and pull-high resistor are disabled automatically。	4
VDD	P	Analog power pin	1
VDD	P	Digital power pin	1
PC0/BZ PC1/BZB	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, with wake up function selected by software programming(falling edge trigger)。Ther can be selected as buzzer function select by software programming。	2
PC2/PWMA1 PC3/PWMA2	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger)。Ther can be selected as PWM function select by software programming。	2
PF0/PWMB1 PF1/PWMB2	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, with wake up function selected by software programming (falling edge trigger)。Ther can be selected as PWM function select by software programming。	2
PF2	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, there can be selected as external wake-up function	1
OSCI	I	Crystal type: crystal input RC type: RC oscillator input External clock input	1
OSCO	O	Crystal type: crystal output RC type: Oscillator frequency divided by 2 is available on OSCO to synchronize other logic or used for testing purpose.	1
PD0-PD3	I/O	General purpose I/O port, hysteresis input, pull high 100Kohm @5v selected by software, there can be selected as external wake-up function	4
		Total Pin	30

Note – Please notice input pin pull low/high or output pin driving current capacity in this table。

.AC / DC Characteristics

.Absolutely max. ratings

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃- +95℃	℃
Storage Temperature	Tsto	-50℃- +125℃	℃
Supply Voltage	VDD	6.0	V
Voltage to input terminal	Vin	Vss-0.3 to Vdd+0.3	V

.D.C. Characteristics

(Condition : Ta= 25 ± 3 ℃, RH ≦ 65 %, VDD = + 3V, VSS=0V)

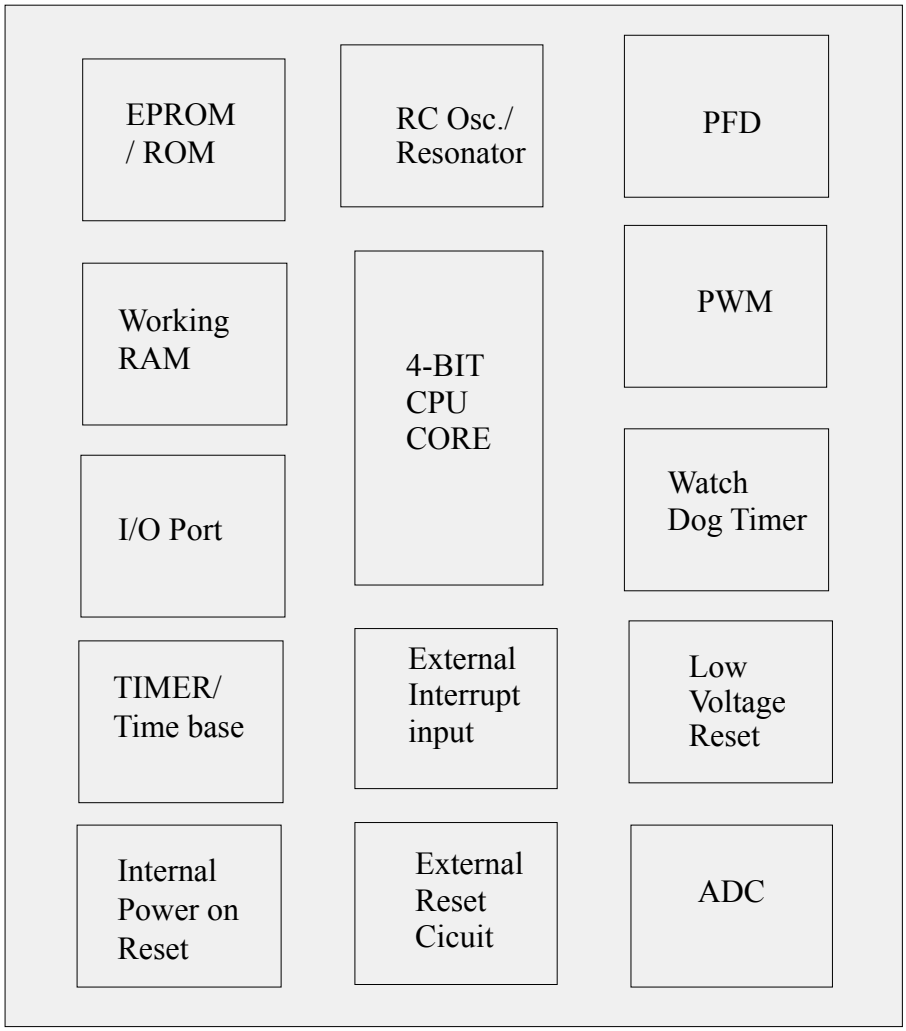
Item	Symbol	Condition	min。	typ。	Max。	unit
Operating voltage	VDD1	(TTU621C/TTU622C)Fsys=4Mhz	2.2	3.0	5.5	V
Operating voltage	VDD1	(TTR621C/TTR622C)Fsys=4Mhz	2.0	3.0	5.5	V
Operating voltage	VDD2	Fsys=8Mhz	3.0	5.0	5.5	V
Power consumption current	I_{OPR1}	System clock at 8Mhz resonator, No load, @5.0V, ADC off		4.0	8.0	mA
Power consumption current	I_{OPR2}	System clock at 4Mhz resonator, No load, @5.0V, ADC off		2.5	5.0	mA
Power consumption current	I_{OPR3}	System clock at 4Mhz RC oscillator, No load, @5.0V, ADC off		2.5	5.0	mA
Power consumption current	I_{OPR4}	System clock at 32Khz crystal oscillator, No load, @3.0V, ADC off		20	40	uA
ADC power consumption	I_{AD1}	Additional power consumption when ADC use(ADC clock is 1Mhz and VDD=3V)		0.5	1	mA
ADC power consumption	I_{AD2}	Additional power consumption when ADC use(ADC clock is 1Mhz and VDD=5V)		1.5	3	mA
Halt current	Ist2	System halt, No load @3.0V, WDT disable			1	uA
Input low voltage for input and I/O port	V_{IL1}		0		0.3VDD	V
Input high voltage for input and I/O port	V_{IH1}		0.7VDD		VDD	V
Input low voltage for RESB pin	V_{IL2}		0		0.4VDD	V
Input high voltage for RESB pin	V_{IH2}		0.9VDD		VDD	V
I/O port sink current	I_{OL1}	V_{OL}=0.1VDD, @5.0V	4	8	16	mA
I/O port source current	I_{OH1}	V_{OH}=0.9VDD, @5.0V	2	4	8	mA
Pull high resistance	R_{UP}	@5V	100	150	200	Kohm
Resonator oscillator sustain voltage	V_{SU}		2.3			V

LVR current	I_{LVR}	@ 3.0V		70	100	uA
A/D input voltage	V_{ADI}	(Vref=VDD)	0		VDD	V
A/D conversion error	E_{ADC}	When VDD from 2.7V-5.5V		±0.5	±1	LSB

.A.C. Characteristics

Item	Symbol	Condition	min。	typ。	Max。	unit
System clock1	f_{SYS1}	Resonator oscillator @3.0v		4		MHz
System clock2	f_{SYS2}	RC oscillator @3.0v，external resistor		4		MHz
Watch dog clock	f_{WDT}	(internal oscillator circuit)	8	16	32	Khz
External reset low pulse width	t_{RES}		1			us
ADC conversion time	t_{ADC}	At 4Mhz system clock，ADC clock is 1MHZ		64		us

.Block Diagram



SU621C-1

.Function Description

1 Map of memory and I/Os

(TTU621C/TTR621C)

000H	(DP1)
001H	A
002H	TB1
003H	TB2
004H	TB3
005H	DPL
006H	DPM
007H	DPH
008H	PS
009H	INTF
00AH	INTC
00BH	PA0&CTL
00CH	PAC
00DH	PA
00EH	PBC
00FH	PB
010H	PCC
011H	PC
012H	PDC
013H	PD
014H	Reserved
015H	
016H	TBC/BZC
017H	TMR1L
018H	TMR1H
019H	TMR1C
01AH	PWM1DL
01BH	PWM1DH
01CH	ADL
01DH	ADH
01EH	ADCTL0
01FH	ADCTL1
020H	RAM
09FH	
0A0H	Reserved
11FH	
120H	PWMC
121H	AD-SEL0
12AH	PWMCK
FFFH	Reserved

Data memory map

000	Reset vector
001	INTB vector
002	On-chip program memory
7FF	
800	Reserved
FFF	

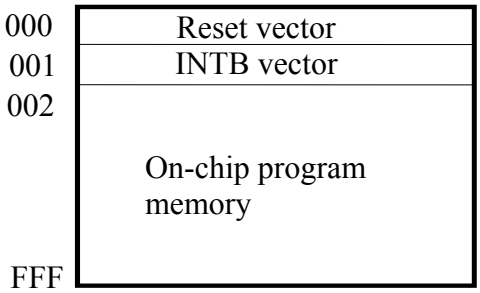
Progrom memory map

SU621C-G1

(TTU622C/TTR622C)

000H	(DP1)
001H	A
002H	TB1
003H	TB2
004H	TB3
005H	DPL
006H	DPM
007H	DPH
008H	PS
009H	INTF
00AH	INTC
00BH	PA0&CTL
00CH	PAC
00DH	PA
00EH	PBC
00FH	PB
010H	PCC
011H	PC
012H	PDC
013H	PD
014H	PEC
015H	PE
016H	TBC/BZC
017H	TMR1L
018H	TMR1H
019H	TMR1C
01AH	PWM1DL
01BH	PWM1DH
01CH	ADL
01DH	ADH
01EH	ADCTL0
01FH	ADCTL1
020H	RAM
11FH	
120H	PWMC
121H	AD-SEL0
122H	AD-SEL1
123H	PFC
124H	PF
125H	PWM2DL
126H	PWM2DH
127H	TMR2L
128H	TMR2H
129H	TMR2C
12AH	PWMCK
FFFH	Reserved

Data memory map



Progrom memory map

SU622C-G1

2I/O MAP TABLE

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	X	H/L	SLEEP	STOP	u100
		X	R/W	R/W	R/W	
009H	INTF	PA0F	TMR1F	TMR2F	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	PA0IE	TMR1IE	TMR2IE	TBIE	0000
		R/W	R/W	R/W	R/W	
00BH	PA0&CTL	RF1	RF0	LVREN	LVRC	0010
		R/W	R/W	R/W	R/W	
00CH	PAC	PAC3	PAC2	PAC1	PAC0	1111
		R/W	R/W	R/W	R/W	
00DH	PA	PA3	PA2	PA1	PA0	1111
		R/W	R/W	R/W	R/W	
00EH	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
010H	PCC	PCC3	PCC2	PCC1	PCC0	1111
		R/W	R/W	R/W	R/W	
011H	PC	PC3	PC2	PC1	PC0	1111
		R/W	R/W	R/W	R/W	
012H	PDC	PDC3	PDC2	PDC1	PDC0	1111
		R/W	R/W	R/W	R/W	
013H	PD	PD3	PD2	PD1	PD0	1111
		R/W	R/W	R/W	R/W	
014H	PEC	PEC3	PEC2	PEC1	PEC0	1111
		R/W	R/W	R/W	R/W	
015H	PE	PE3	PE2	PE1	PE0	1111
		R/W	R/W	R/W	R/W	
016H	TBC/BZC	BZEN	TB2	TB1	TB0	0000
		R/W	R/W	R/W	R/W	
017H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
018H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
019H	TMR1C	TM1LD	T1CK1	T1CK0	TM1EN	0000
		R/W	R/W	R/W	R/W	
01AH	PWMADL	DTY13	DTY12	DTY11	DTY10	0000
		R/W	R/W	R/W	R/W	
01BH	PWMADH	DTY17	DTY16	DTY15	DTY14	0000
		R/W	R/W	R/W	R/W	
01CH	ADL	AD3	AD2	AD1	AD0	0000

		R	R	R	R	
01DH	ADH	AD7	AD6	AD5	AD4	0000
		R	R	R	R	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	
120H	PWMC	PWMA2EN	PWMA1EN	PWMA2DC	PWMA1DC	0000
		R/W	R/W	R/W	R/W	
121H	AD-SEL0	AN3/PB3	AN2/PB2	AN1/PB1	AN0/PB0	0000
		R/W	R/W	R/W	R/W	
122H	AD-SEL1	AN7/PE3	AN6/PE2	AN5/PE1	AN4/PE0	0000
		R/W	R/W	R/W	R/W	
123H	PFC	X	PFC2	PFC1	PFC0	u111
		X	R/W	R/W	R/W	
124H	PF	X	PF2	PF1	PF0	u111
		X	R/W	R/W	R/W	
125H	PWMBDL	DTY23	DTY22	DTY21	DTY20	0000
		R/W	R/W	R/W	R/W	
126H	PWMBDH	DTY27	DTY26	DTY25	DTY24	0000
		R/W	R/W	R/W	R/W	
127H	TMR2L	TMR2_3	TMR2_2	TMR2_1	TMR2_0	0000
		R/W	R/W	R/W	R/W	
128H	TMR2H	TMR2_7	TMR2_6	TMR2_5	TMR2_4	0000
		R/W	R/W	R/W	R/W	
129H	TMR2C	TM2LD	T2CK1	T2CK0	TM2EN	0000
		R/W	R/W	R/W	R/W	
12AH	PWMCK	CK2_S1	CK2_S0	CK1_S1	CK1_S0	0000
		R/W	R/W	R/W	R/W	

3 SYSTEM CONTROL REGISTER

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	X	H/L	SLEEP	STOP	1100
		X	R/W	R/W	R/W	

STOP：high active。(All oscillator circuit is not active。)
SLEEP：high active。

Operating mode / Function status	SLEEP(high active)	STOP(high active)
Oscillator	Operating	Stopped
CPU internal status	Retain the status	
Memory，Flag，Register，I/O	Retain the status	
Program counter	Hold the executed address	
Timer/Counter/ Time base timer	Operated	Stopped & Retain
Watch-dog enable	Retain the status	
Release Condition(and clear STOP or SLEEP flag)	PA0-INT/ PA&PB & PC&PD &PE&PF port Wake-up / ADC-INT/ TMR1-INT/ TMR2-INT/ TB-INT	PA0-INT/ PA&PB &PC&PD &PE&PF port Wake-up

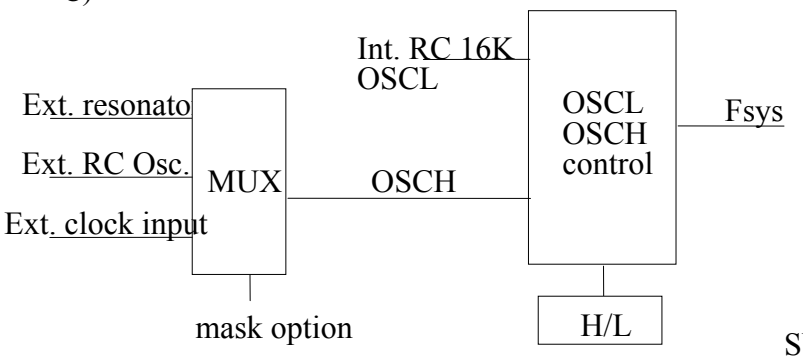
4 SYSTEM CLOCK CONTROL REGISTER

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	X	H/L	SLEEP	STOP	u100
		X	R/W	R/W	R/W	

H/L：Oscillator speed control register。

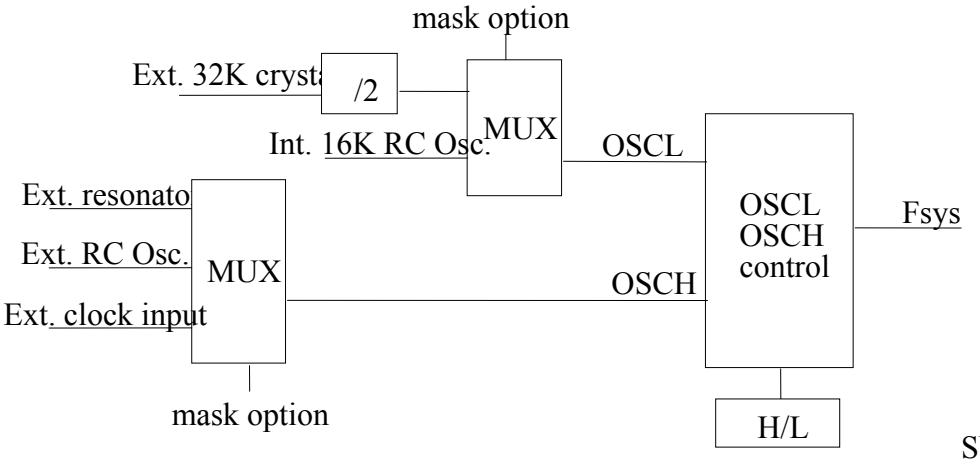
FLAG	FUNCTION
H/L	Low：oscillator low speed mode (OSCL) High：oscillator high speed mode (OSCH)

(TTU621C/TTR621C)



SU621C-J

(TTU622C/TTR622C)



SU622C-J

* 如果選 RTC(Ext. 32K crystal) 時，Int. 16KRC Osc. 要 Off。
* OSCL is always on except STOP=high。
* 如果進入 SLEEP MODE 時，若是 H/L 停在 low speed mode，此時 OSCH 要 off。
* 在 External RC oscillator mode 時，OSCO pin 會輸出 RC Osc. 頻率除以二的 clock 輸出。

*** RTC oscillation stable time needs 0.5sec ~2 sec that depends on operating voltage and IC process.**

Low Voltage Reset

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
00BH	PA0&CTL	RF1	RF0	LVREN	LVRC	0010
		R/W	R/W	R/W	R/W	

FLAG	FUNCTION
LVREN	Low：disable LVR function High：enable LVR function
LVRC	Low：select V+ level for LVR when LVREN=1 TTU622 : LVR 的偵測電壓爲 VDD < 2.4V ± 10% TTR622 : LVR 的偵測電壓爲 VDD < 2.2V ± 10% High：select V+ level for LVR when LVREN=1 LVR 的偵測電壓爲：VDD < 3.0V ± 10%

(TTU622C)

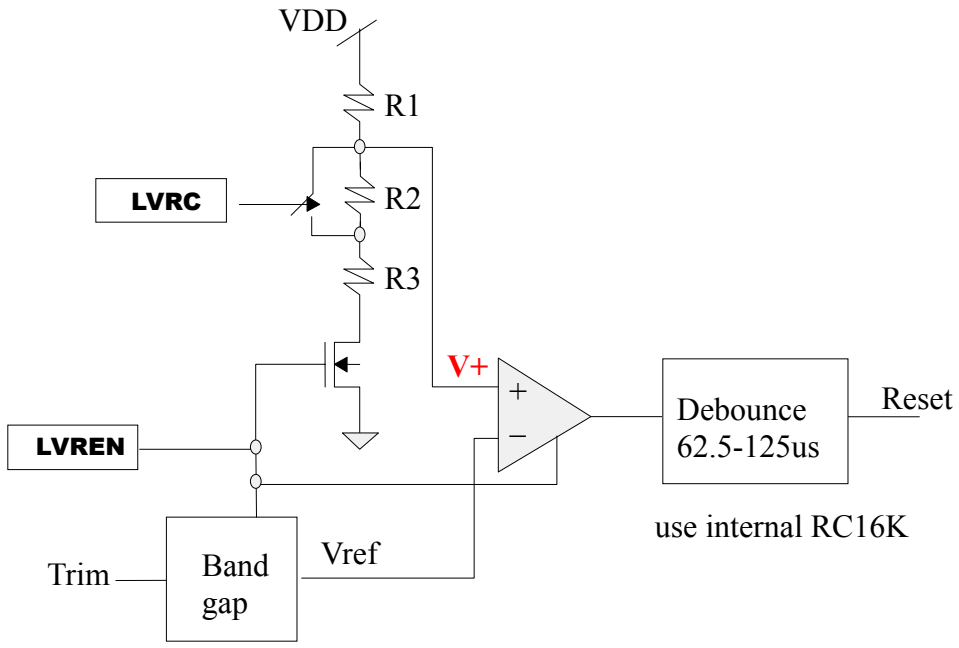
LVR 的偵測電壓爲：

- VDD < 2.4V ± 10%
- VDD < 3.0V ± 10%

(TTR622C)

LVR 的偵測電壓爲：

- VDD < 2.2V ± 10%
- VDD < 3.0V ± 10%



5 I/O REGISTER

A. Port A

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	PA0F	TMR1F	TMR2F	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	PA0IE	TMR1IE	TMR2IE	TBIE	0000
		R/W	R/W	R/W	R/W	
00BH	PA0&CTL	RF1	RF0	LVREN	LVRC	0010
		R/W	R/W	R/W	R/W	
00CH	PAC	PAC3	PAC2	PAC1	PAC0	1111
		R/W	R/W	R/W	R/W	
00DH	PA	PA3	PA2	PA1	PA0	1111
		R/W	R/W	R/W	R/W	

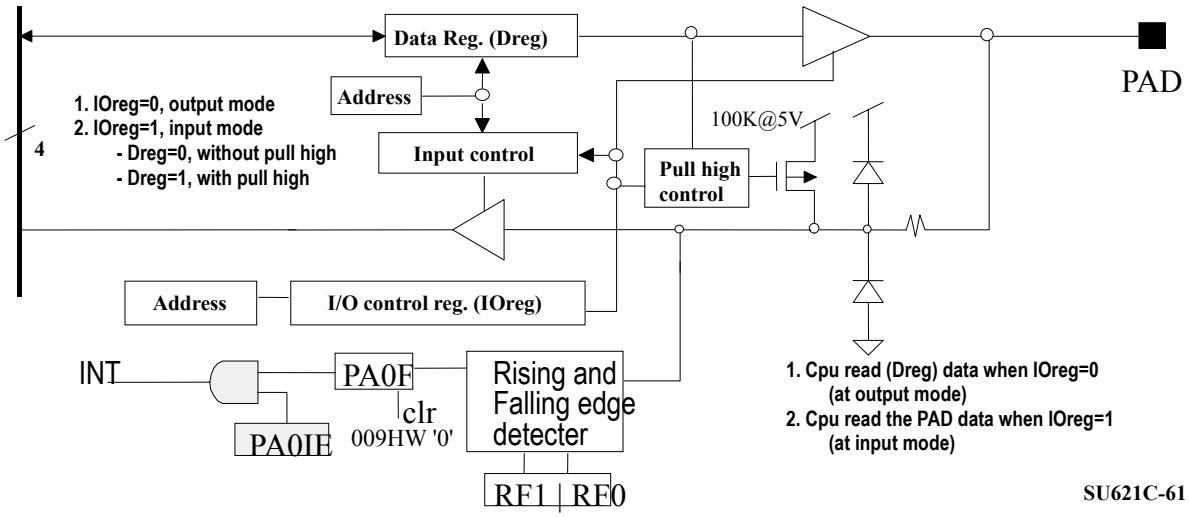
PAC：是控制 I/O mode，爲 high 時，是 input mode。

PA0 在 input mode 時，有 interrupt 功能(rising and falling edge trigger)，當系統進入 STOP or SLEEP mode 時，可以用此 PIN 來 wake up。

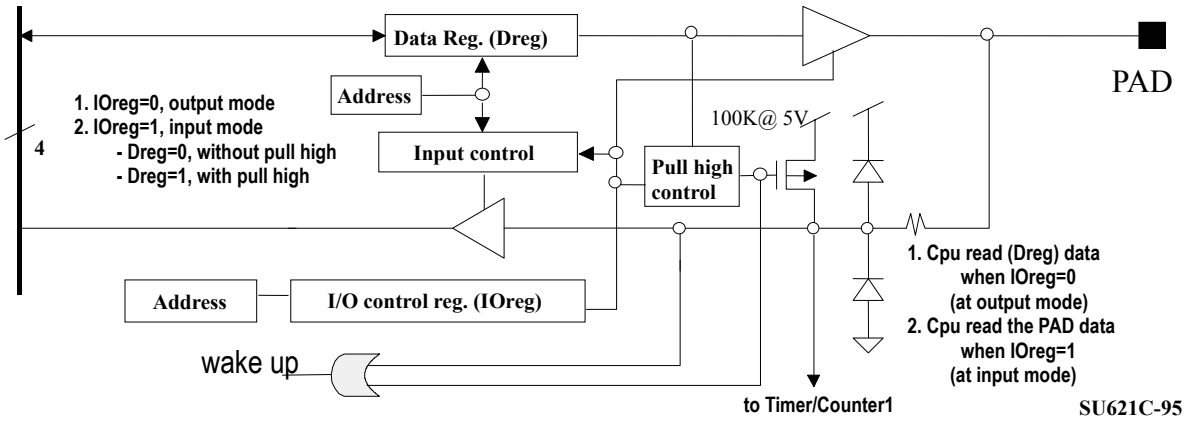
PA0F：此 flag 會被 write bit "0" 時 clear 爲 "0"，但是不會被 write bit "1" 時 set 爲 "1"。

RF0/RF1：控制 interrupt 的 trigger 方式。

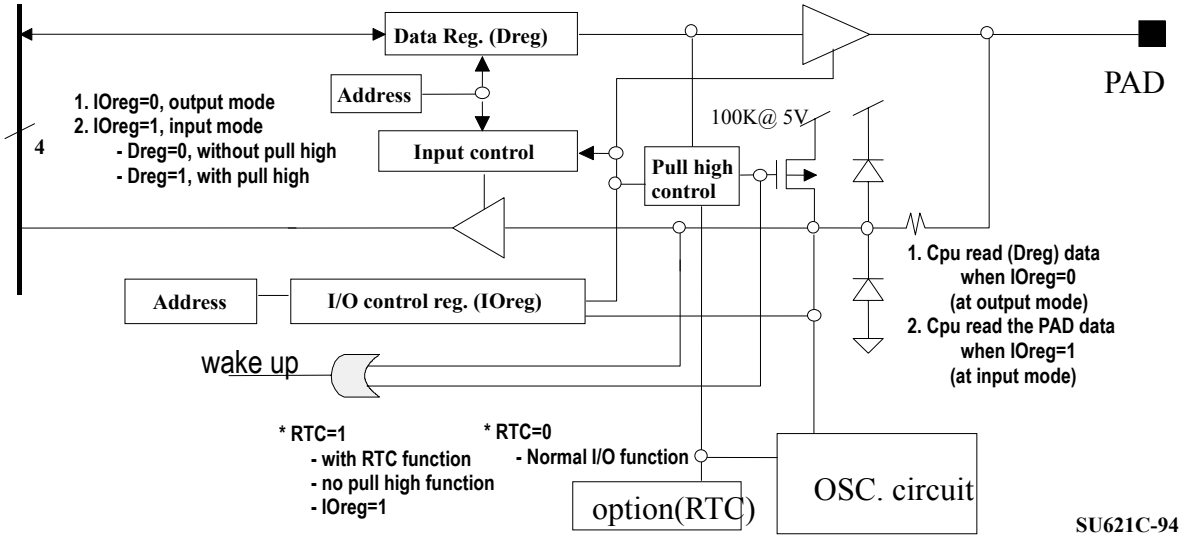
RF1	RF0	Trigger
0	0	falling edge
0	1	rising edge
1	0	falling & rising edge
1	1	falling & rising edge



PA1：爲 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。此 pin 亦可當作 Timer/Counter 的 clock input。



PA2/PA3：爲 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。也可以經由 mask option 來選擇爲是 32768Hz crystal oscillator pin。

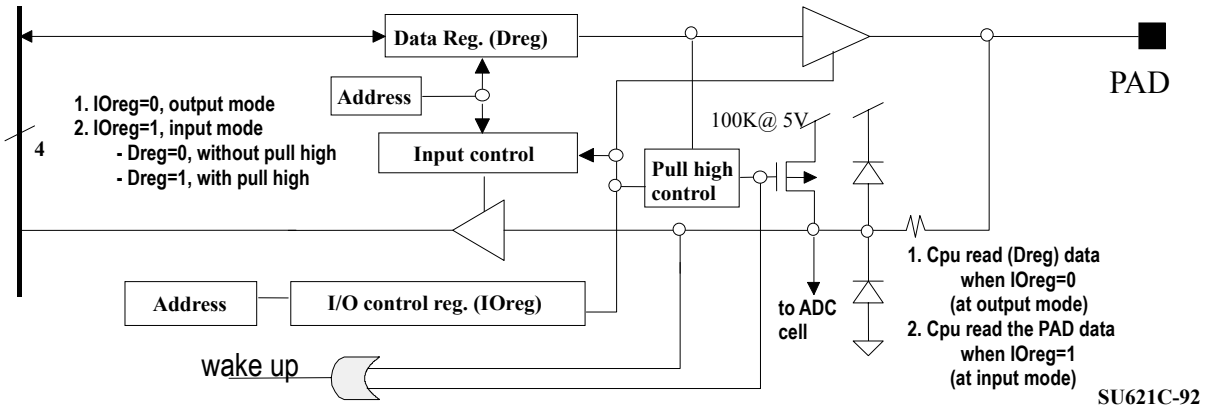


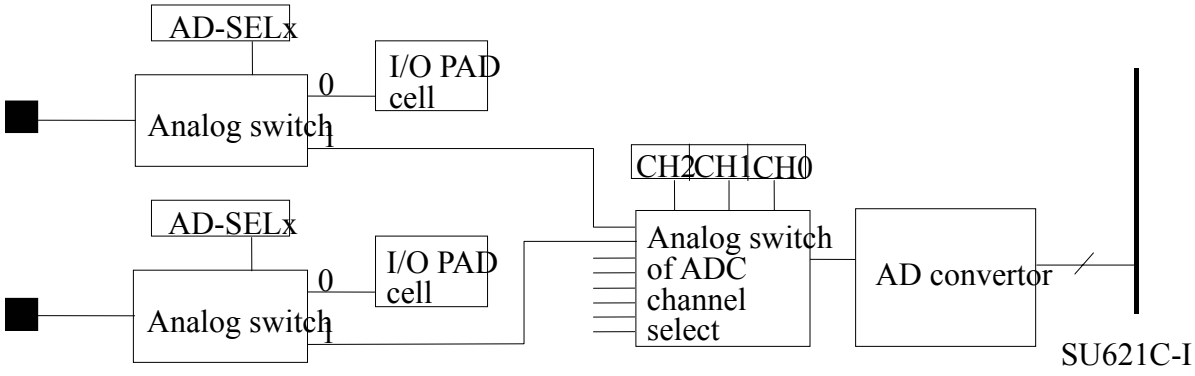
B. Port B & Port E

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
00EH	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
014H	PEC	PEC3	PEC2	PEC1	PEC0	1111
		R/W	R/W	R/W	R/W	
015H	PE	PE3	PE2	PE1	PE0	1111
		R/W	R/W	R/W	R/W	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	
121H	AD-SEL0	AN3/PB3	AN2/PB2	AN1/PB1	AN0/PB0	0000
		R/W	R/W	R/W	R/W	
122H	AD-SEL1	AN7/PE3	AN6/PE2	AN5/PE1	AN4/PE0	0000
		R/W	R/W	R/W	R/W	

PBC/ PEC：是控制 I/O mode，爲 high 時，是 input mode。

PB/ PE：爲 I/O port data，在 input mode 時(AD-SELx=0)，(Dreg)可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。





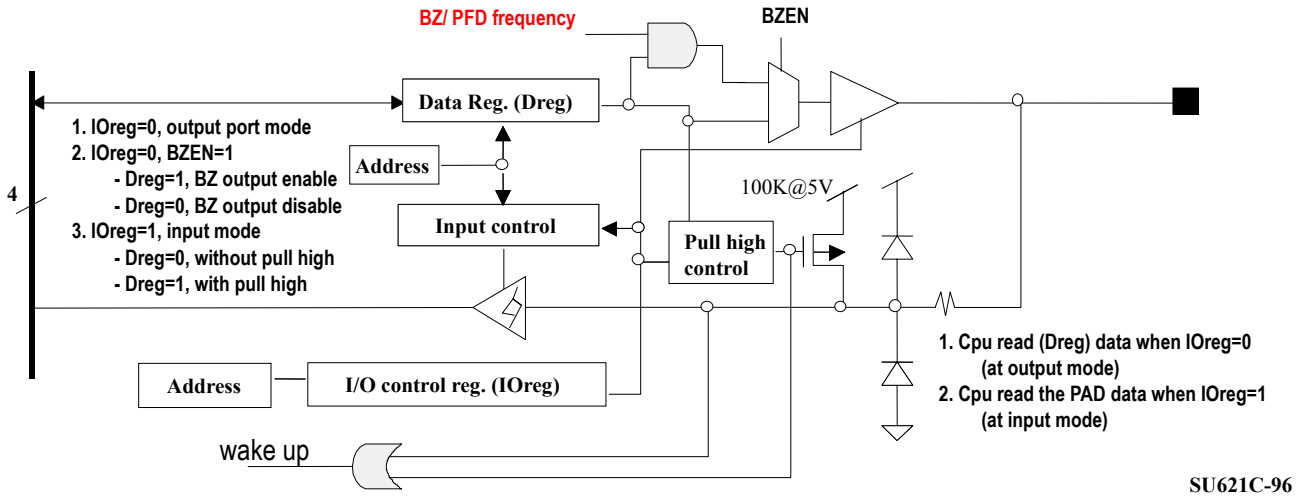
CH2	CH1	CH0	ADC channel selection
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

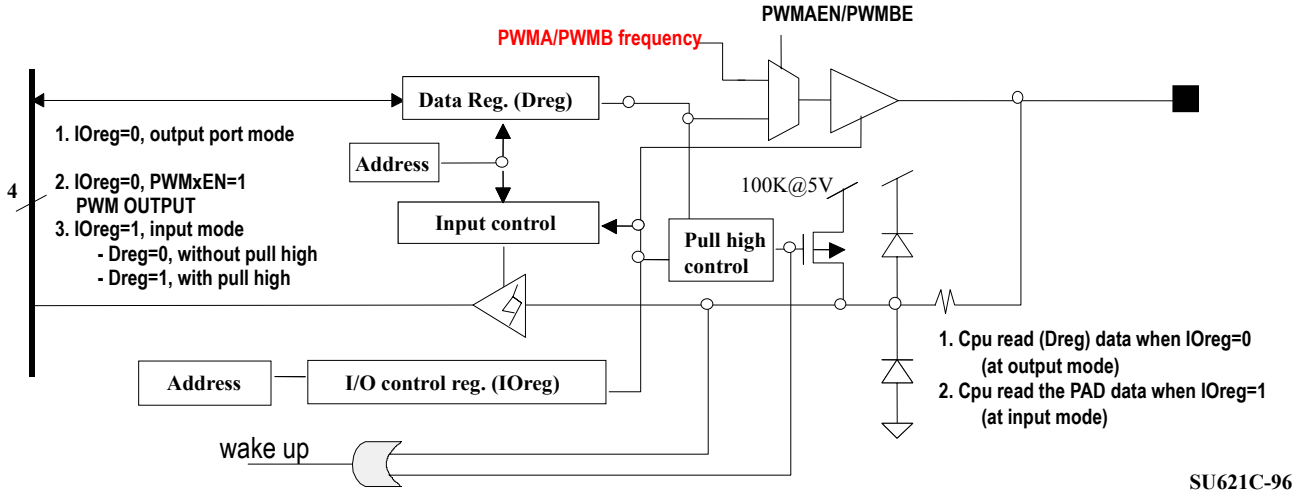
C. Port C/ Port F

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
010H	PCC	PCC3	PCC2	PCC1	PCC0	1111
		R/W	R/W	R/W	R/W	
011H	PC	PC3	PC2	PC1	PC0	1111
		R/W	R/W	R/W	R/W	
016H	TBC/BZC	BZEN	TB2	TB1	TB0	0000
		R/W	R/W	R/W	R/W	
120H	PWMC	PWMBEN	PWMAEN	PWMBDC	PWMADC	0000
		R/W	R/W	R/W	R/W	
123H	PF	X	PF2	PF1	PF0	u111
		X	R/W	R/W	R/W	
124H	PFC	X	PFC2	PFC1	PFC0	u111
		X	R/W	R/W	R/W	

PCC/ PFC：是控制 I/O mode，爲 high 時，是 input mode。

PC：爲 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function。在 output mode & BZEN=1 時，(Dreg) 可以控制是否有爲 Buzzer/ PFD 輸出（當 Dreg=1 時輸出頻率，當 Dreg=0 時輸出爲 low），如下圖。在 output mode & PWMxEN=1 時, 如果(IOreg=0)爲 PWM 輸出, 如果(IOreg=1)則爲 input mode。





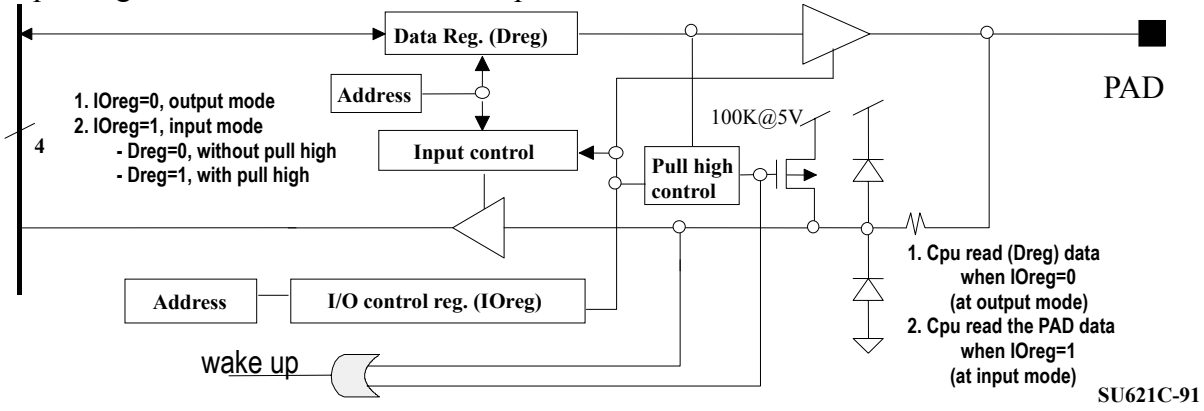
FLAG	FUNCTION
BZEN	LOW：PC0/PC1 without buzzer function HIGH：PC0/PC1 with buzzer function and enable buzzer frequency output through PC0 pad
PWMAEN	LOW：PC2/ PC3 without PWM function，I/O function only HIGH：PC2/ PC3 with PWM function or input function are controlled as below: - If (IOreg)=0 then enable PWMA frequency output through pad - If (IOreg)=1 then at input function mode
PWMBEN	LOW：PF0/ PF1 without PWM function，I/O function only HIGH：PF0/ PF1 with PWM function or input function are controlled as below: - If (IOreg)=0 then enable PWMB frequency output through pad - If (IOreg)=1 then at input function mode

D. Port D

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
012H	PDC	PDC3	PDC2	PDC1	PDC0	1111
		R/W	R/W	R/W	R/W	
013H	PD	PD3	PD2	PD1	PD0	1111
		R/W	R/W	R/W	R/W	

PDC：是控制 I/O mode，爲 high 時，是 input mode。

PD：爲 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，若此 pin 有 pull high function 時，就有 wake up function，如下圖。



6 A/D function description

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
01CH	ADL	AD3	AD2	AD1	AD0	0000
		R	R	R	R	
01DH	ADH	AD7	AD6	AD5	AD4	0000
		R	R	R	R	
01EH	ADCTL0	ADEN	CH2	CH1	CH0	0000
		R/W	R/W	R/W	R/W	
01FH	ADCTL1	ADIE	ADF	ADCK1	ADCK0	0000
		R/W	R/W	R/W	R/W	

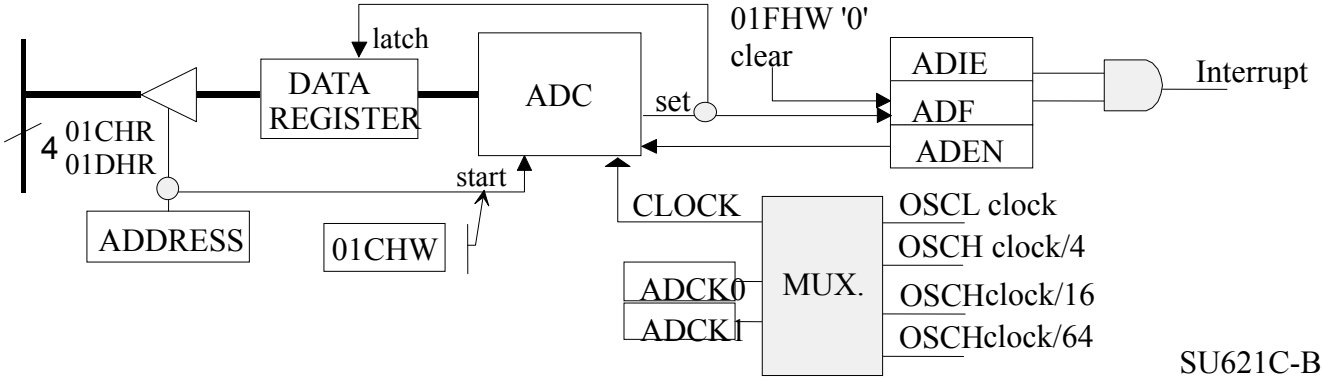
ADL/ADH：(AD0-AD7) 是 A/D 的 DATA。

如果對此 01CH PORT 做 WRITE 的動作時，要讓 ADC START CONVERSION。

如果對此 01DH PORT 做 WRITE 的動作時，要讓 CPU SLEEP & ADC START CONVERSION。

ADCTL0/ ADCTL1： 是 A/D 的 CONTROL REGISTER。

FLAG	FUNCTION
ADIE	LOW：Disable internal interrupt HIGH：Enable internal interrupt
ADF	LOW：Normal mode HIGH：A/D conversion complete flag。此 flag 會被 write bit "0" 時 clear 爲 "0"，但是不會被 write bit "1" 時 set 爲 "1"
ADEN	LOW：Disable A/D HIGH：Enable A/D
CH2 CH1 CH0	(CH2/CH1/CH0) 000：select AN0 input，001：select AN1 input，010：select AN2 input， 011：select AN3 input，100：select AN4 input，101：select AN5 input， 110：select AN6 input，111：select AN7 input。
ADCK1 ADCK0	(ADCK1/ ADCK0) 00：select OSCL clock，01：select OSCH clock/4， 10：select OSCH clock/16，11：select OSCH clock/64.



當 ADC 完成 conversion 後，才 latch "ADL" 和 "ADH" 的 data。

7 8-bit and 16-bit Timer/Counter function description

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	PA0F	TMR1F	TMR2F	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	PA0IE	TMR1IE	TMR2IE	TBIE	0000
		R/W	R/W	R/W	R/W	
017H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
018H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
019H	TMR1C	TM1LD	T1CK1	T1CK0	TM1EN	0000
		R/W	R/W	R/W	R/W	
127H	TMR2L	TMR2_3	TMR2_2	TMR2_1	TMR2_0	0000
		R/W	R/W	R/W	R/W	
128H	TMR2H	TMR2_7	TMR2_6	TMR2_5	TMR2_4	0000
		R/W	R/W	R/W	R/W	
129H	TMR2C	TM2LD	T2CK1	T2CK0	TM2EN	0000
		R/W	R/W	R/W	R/W	

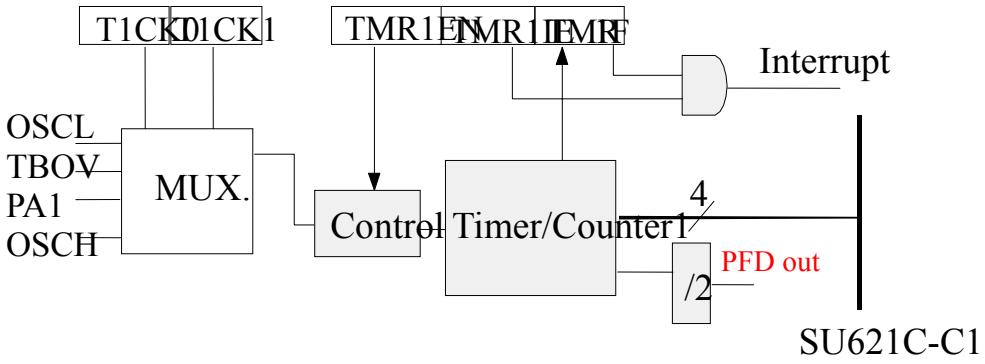
INTF：TMR1F/ TMR2F 是 Timer/Counter 的 overflow flag。（此 flag 會被 write bit "0" 時 clear 爲 "0"，但是不會被 write bit "1" 時 set 爲 "1"）

INTC：TMR1IE/TMR2IE 是控制 TMR1F/TMR2F 要不要產生 interrupt。

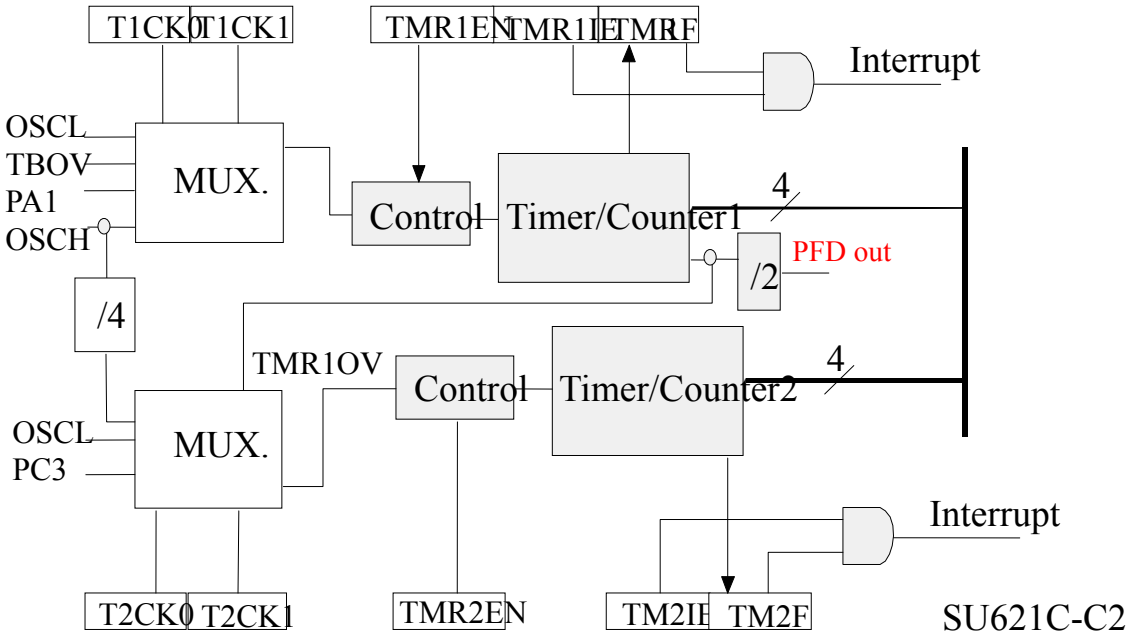
TMR1L/ TMR1H/ TMR2L/ TMR2H：Timer/Counter data，Timer/Counter 的 data 可以 R/W。Overflow 時會 set interrupt flag（TMR1F/TMR2F）

FLAG	FUNCTION
TM1EN	Low：stop Timer/Counter1 High：start Timer/Counter1
TM2EN	Low：stop Timer/Counter2 High：start Timer/Counter2
TM1LD	Low：without Auto-reload function(Timer/Counter1) High：with Auto-reload function(Timer/Counter1)
TM2LD	Low：without Auto-reload function(Timer/Counter2) High：with Auto-reload function(Timer/Counter2)
T1CK1/ T1CK0	(T1CK1/ T1CK0) 00： select OSCH clock 01： select time base timer clock(OSCL) 10： select PA1 external input clock 11： select time base timer overflow(TBOV)
T2CK1/ T2CK0	(T2CK1/ T2CK0) 00： select OSCH clock/4 01： select time base timer clock(OSCL) 10： select PC3 external input clock 11： select time base timer overflow(TMR1OV)

(TTU621C/TTR621C)



(TTU622C/TTR622C)



8 PWM CONTROL CIRCUIT

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
01AH	PWMADL	DTY13	DTY12	DTY11	DTY10	0000
		R/W	R/W	R/W	R/W	
01BH	PWMADH	DTY17	DTY16	DTY15	DTY14	0000
		R/W	R/W	R/W	R/W	
120H	PWMC	PWMBEN	PWMAEN	PWMBDC	PWMADC	0000
		R/W	R/W	R/W	R/W	
125H	PWMBDL	DTY23	DTY22	DTY21	DTY20	0000
		R/W	R/W	R/W	R/W	
126H	PWMBDH	DTY27	DTY26	DTY25	DTY24	0000
		R/W	R/W	R/W	R/W	
12AH	PWMCK	CK2_S1	CK2_S0	CK1_S1	CK1_S0	0000
		R/W	R/W	R/W	R/W	

PWMADL，PWMADH，PWMBDL，PWMBDH：控制 PWM 的 duty。(register option 2 modes)

FLAG	FUNCTION
PWMAEN	Low：disable PWMA output High：enable PWMA output
PWMBEN	Low：disable PWMB output High：enable PWMB output
PWMADC	Low：PWM circuit in 4 duty mode when PWMAEN is high state High：PWM circuit in 2 duty mode when PWMAEN is high state
PWMBDC	Low：PWM circuit in 4 duty mode when PWMBEN is high state High：PWM circuit in 2 duty mode when PWMBEN is high state
CK1_S1/ CK1_S0	Select PWMA input clock（CK1_S1/CK1_S0) 00 : external high frequency，01: external high frequency/4 10 : external high frequency/16，11: external high frequency/64
CK2_S1/ CK2_S0	Select PWMB input clock（CK2_S1/CK2_S0) 00 : external high frequency，01: external high frequency/4 10 : external high frequency/16，11: external high frequency/64

4 duty cycle mode：

DTY*7	DTY*6	DTY*5	DTY*4	DTY*3	DTY*2	DTY*1	DTY*0	4 Duty Cycles
0	0	0	0	0	0	0	0	0/64+0/64+0/64+0/64
0	0	0	0	0	0	0	1	1/64+0/64+0/64+0/64
0	0	0	0	0	0	1	0	1/64+1/64+0/64+0/64
0	0	0	0	0	0	1	1	1/64+1/64+1/64+0/64
0	0	0	0	0	1	0	0	1/64+1/64+1/64+1/64
…	…	…	…	…	…	…	…	…
0	1	0	0	0	0	0	1	17/64+16/64+16/64+16/64
0	1	0	0	0	0	1	0	17/64+17/64+16/64+16/64
0	1	0	0	0	0	1	1	17/64+17/64+17/64+16/64
0	1	0	0	0	1	0	0	17/64+17/64+17/64+17/64
…	…	…	…	…	…	…	…	…

1	0	0	0	0	0	0	1	33/64+32/64+32/64+32/64
1	0	0	0	0	0	1	0	33/64+33/64+32/64+32/64
1	0	0	0	0	0	1	1	33/64+33/64+33/64+32/64
1	0	0	0	0	1	0	0	33/64+33/64+33/64+33/64
…	…	…	…	…	…	…	…	…
1	1	0	0	0	0	0	1	49/64+48/64+48/64+48/64
1	1	0	0	0	0	1	0	49/64+49/64+48/64+48/64
1	1	0	0	0	0	1	1	49/64+49/64+49/64+48/64
1	1	0	0	0	1	0	0	49/64+49/64+49/64+49/64
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	0	63/64+63/64+63/64+63/64
1	1	1	1	1	1	0	1	64/64+63/64+63/64+63/64
1	1	1	1	1	1	1	0	64/64+64/64+63/64+63/64
1	1	1	1	1	1	1	1	64/64+64/64+64/64+63/64

2 duty cycle mode：

DTY*7	DTY*6	DTY*5	DTY*4	DTY*3	DTY*2	DTY*1	DTY*0	2 Duty Cycles
0	0	0	0	0	0	0	0	0/128+0/128
0	0	0	0	0	0	0	1	1/128+0/128
0	0	0	0	0	0	1	0	1/128+1/128
0	0	0	0	0	0	1	1	2/128+1/128
0	0	0	0	0	1	0	0	2/128+2/128
…	…	…	…	…	…	…	…	…
0	1	0	0	0	0	0	1	33/128+32/128
0	1	0	0	0	0	1	0	33/128+33/128
0	1	0	0	0	0	1	1	34/128+33/128
0	1	0	0	0	1	0	0	34/128+34/128
…	…	…	…	…	…	…	…	…
1	0	0	0	0	0	0	1	65/128+64/128
1	0	0	0	0	0	1	0	65/128+65/128
1	0	0	0	0	0	1	1	66/128+65/128
1	0	0	0	0	1	0	0	66/128+66/128
…	…	…	…	…	…	…	…	…
1	1	0	0	0	0	0	1	97/128+96/128
1	1	0	0	0	0	1	0	97/128+97/128
1	1	0	0	0	0	1	1	98/128+97/128
1	1	0	0	0	1	0	0	98/128+98/128
…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	0	126/128+126/128
1	1	1	1	1	1	0	1	127/128+126/128
1	1	1	1	1	1	1	0	127/128+127/128
1	1	1	1	1	1	1	1	128/128+127/128

9 Time Base Timer

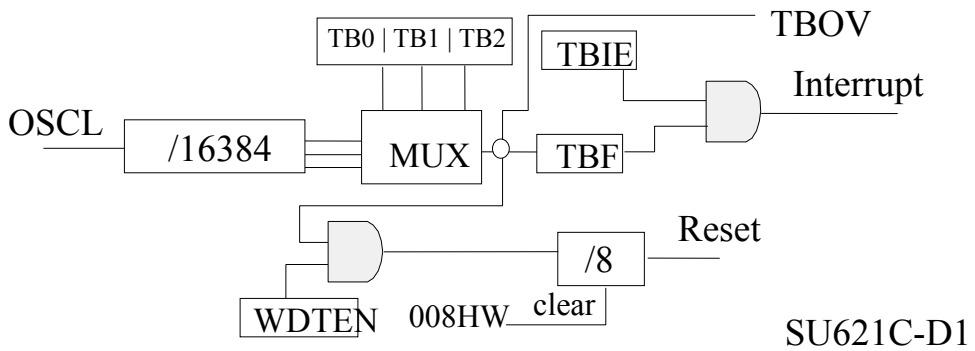
Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	PA0F	TMR1F	TMR2F	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	PA0IE	TMR1IE	TMR2IE	TBIE	0000
		R/W	R/W	R/W	R/W	
016H	TBC/BZC	BZEN	TB2	TB1	TB0	0000
		R/W	R/W	R/W	R/W	

TBF： Time base timer overflow flag。(此 flag 會被 write bit "0" 時 clear 爲 "0"，但是不會被 write bit "1" 時 set 爲 "1")

TBIE：Time base timer interrupt enable control register。

TB0/ TB1/ TB2：Time base timer input clock source select register。

TB2	TB1	TB0	O/P
0	0	0	128HZ
0	0	1	64HZ
0	1	0	32HZ
0	1	1	16HZ
1	0	0	8HZ
1	0	1	4HZ
1	1	0	2HZ
1	1	1	1HZ



注意：在 RTC mode，若有使用 Time base timer 功能，在 power on 後和每次在 Stop mode wake-up 起來之後，一定要先下 "read 008H（008HR）" 的動作，否則其頻率會不準確。

*** RTC oscillation stable time needs 0.5 sec ~2 sec that depends on operating voltage and IC process.**

10 Watch Dog Timer

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	X	H/L	SLEEP	STOP	u100
		X	R/W	R/W	R/W	

可以使用 008HW 來 clear WDT，如上圖。

RESET PLAN

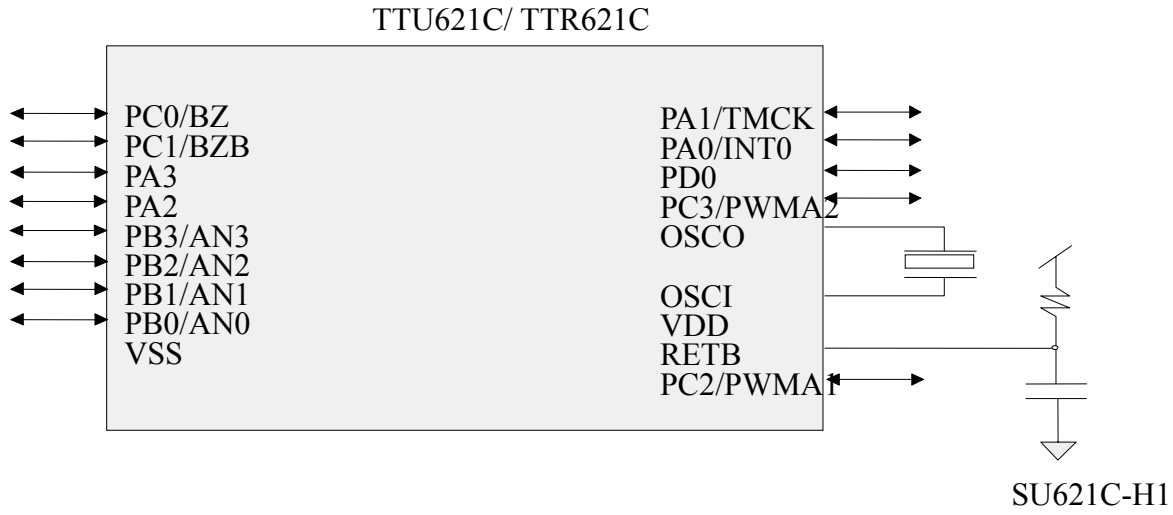
Reset 方式有 3 種：

A. INTERNAL RESET

B. EXTERNAL RESET（ACTIVE LOW）

C. LVR RESET（單邊 reset，high voltage to low voltage）

.Application Diagram



.Mask option table

Function	Option	U621C	R621C	U622C	R622C
Oscillator type	□ Resonator。 □ RC oscillator。	mask	mask	mask	mask
Time base clock selection	□ External 32K crystal oscillator。 □ Internal RC oscillator。	X	X	mask	mask
LVR control	□ LVR disable □ LVR enable	mask	mask	mask	mask
Buzzer frequency selection	□ 2KHZ。 □ 4KHZ。 □ 6KHZ。 □ PFD。	mask	mask	mask	mask

. RC oscillator Resistor vs. Frequency table

電阻（Ω）	電壓(V)	頻率(Hz)
51K	5	7.3M
56K	5	6.6M
62K	5	6.1M
68K	5	5.4M
75K	5	4.7M
82K	5	4.4M
91K	5	4.1M
100K	5	3.7M
120K	5	3.1M
150K	5	2.4M
160K	5	2.3M
180K	5	2.0M
200K	5	1.8M
220K	5	1.7M
240K	5	1.6M
300K	5	1.2M
510K	5	714K
1M	5	368K

. ORDER INFORMATION

(TTU621C/TTR621C)

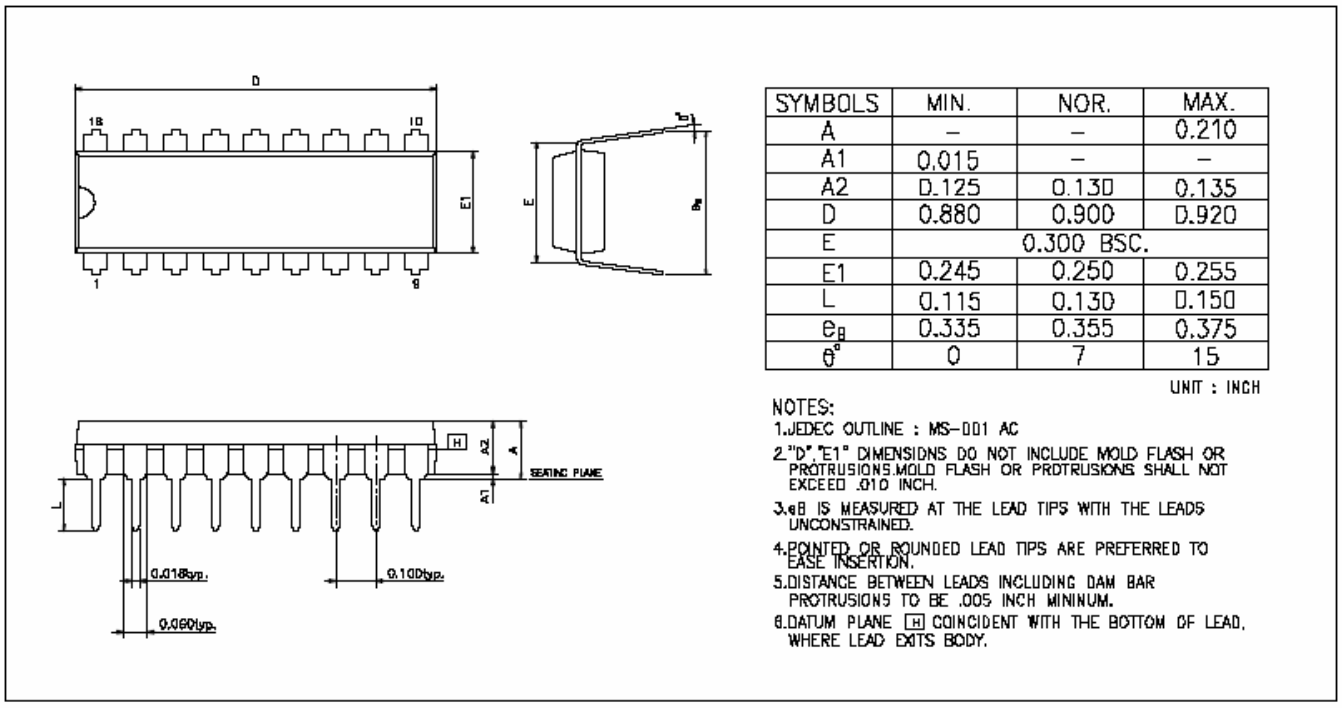
a. Package form : TTU621C
b. Chip form : TCU621C
c. Wafer base : TDU621C

(TTU622/TTR622)

a. Package form : TTU622C
b. Chip form : TCU622C
c. Wafer base : TDU622C

. Package Information

(18-DIP)

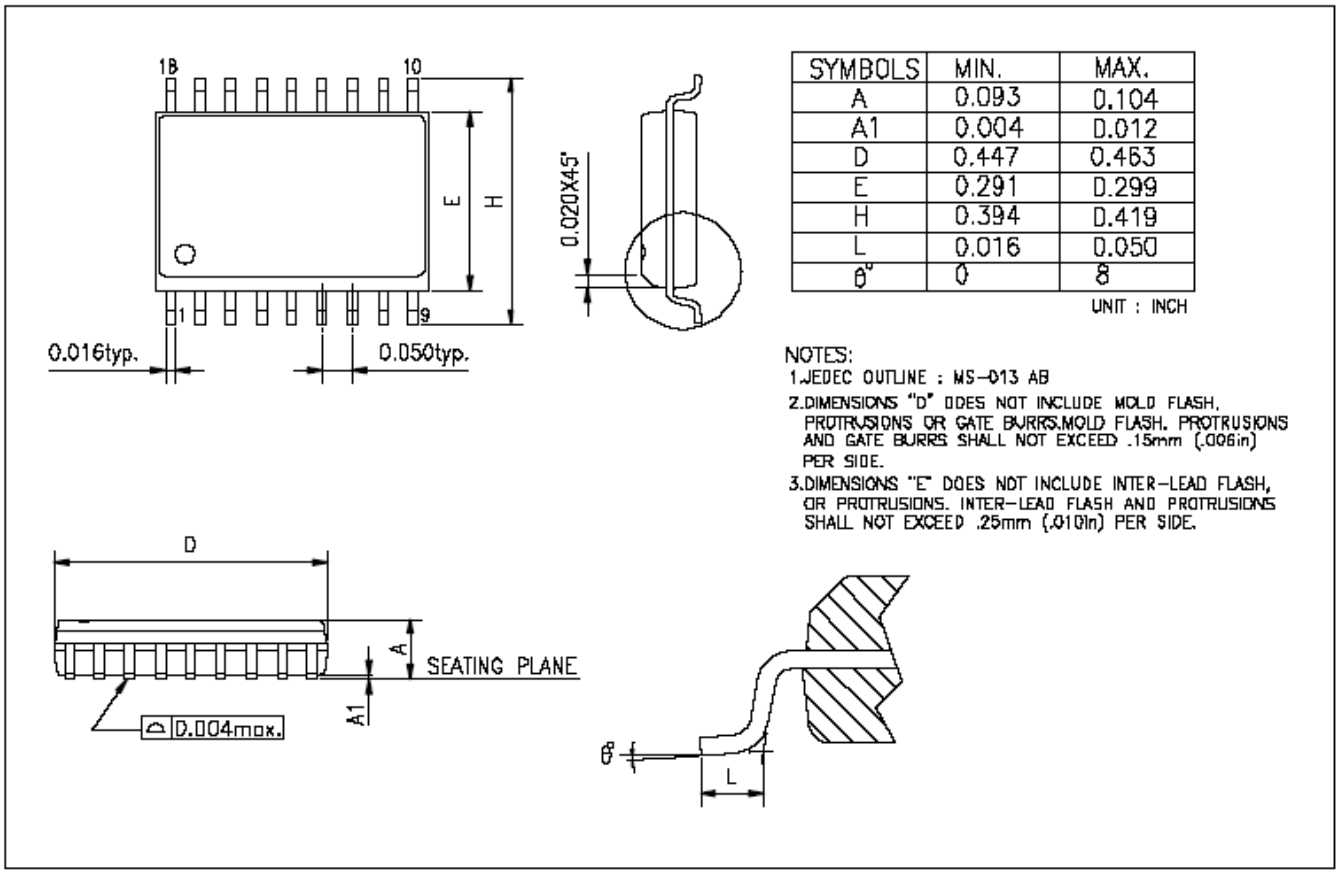


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.880	0.900	0.920
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-001 AC
2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

(18-SOP)

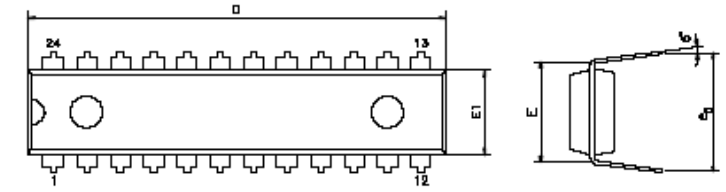


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

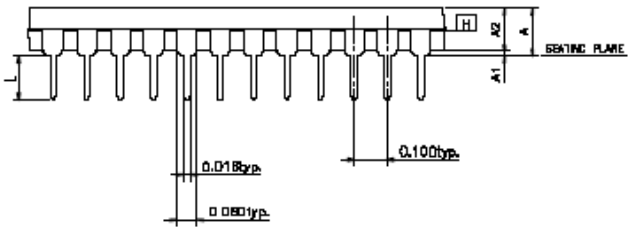
NOTES:
1. JEDEC OUTLINE : MS-013 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

(24-SKINNY DIP)



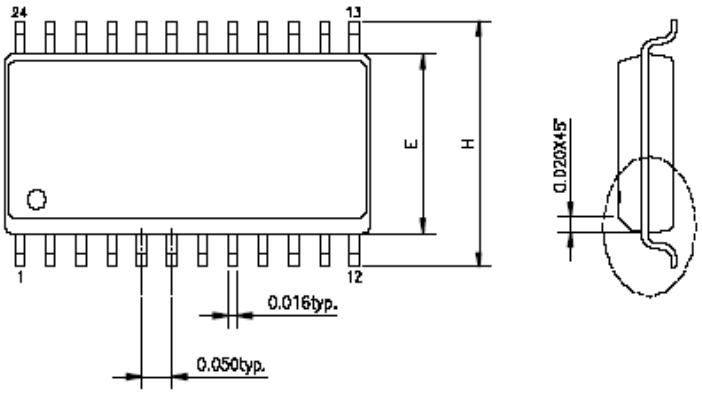
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E		0.300 BSC.	
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH



NOTES:
1. JEDEC OUTLINE : MS-001 AF
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

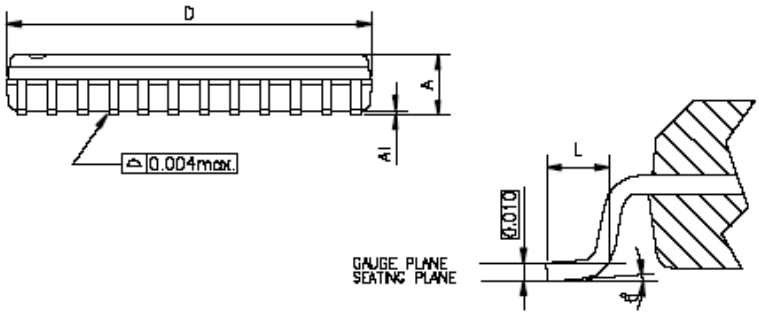
(24-SOP)



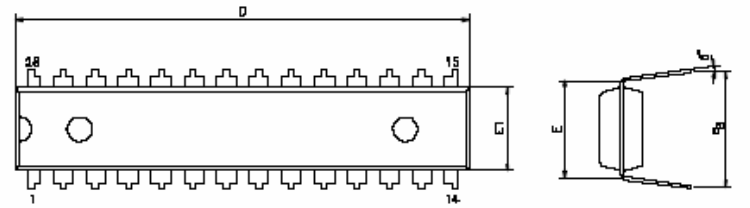
SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	–	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	–	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-013 AD
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.



(28-SKINNY DIP)

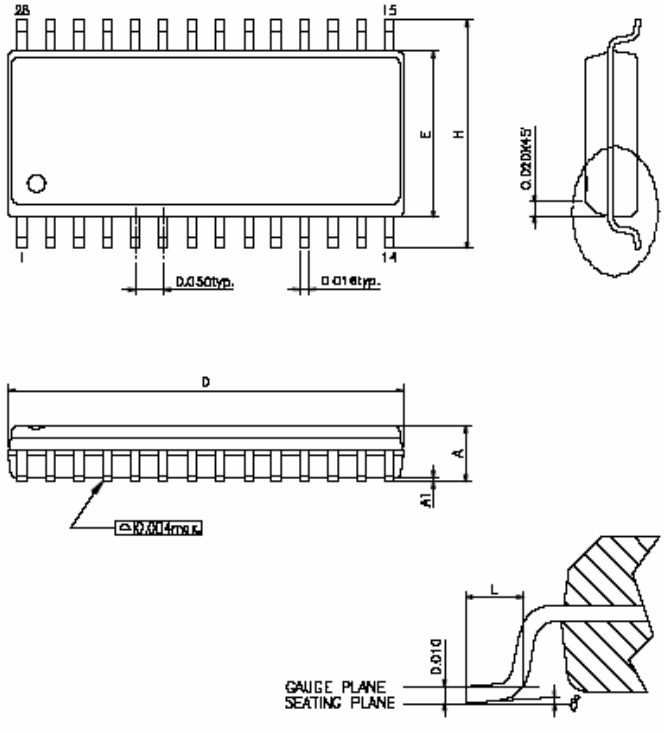


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E		0.310 BSC	
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
e_B	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-015 AH

(28-SOP)



SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.697	0.713
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AE
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

. Revise History

2005/9/26 p.15 & p.27 RTC OST 0.5 sec ~2 sec

2006/5/29 p10,p11,p12,p16,p17

P10,p11 : Map of memory and I/Os add PWMCK

p12,p16,p17: update PA0&CTL register initial state

p16 : update LVRC register function description and graph

2006/06/02 p.25, p.27

PWMAEN→PWMBEN

WDT/4→WDT/8

2006/07/05 p.3, p.7

Update operating voltage

Update pull high resistance

2006/10/05 p.29
Update RC oscillator Resistor vs. Frequency table

2006/11/30 p.8
Update A.C. Characteristics. Watch dog clock from 8K to 32KHz.

2007/5/28 p.20, p.21 : update PC PF graph and description
p.7 : Iopr1, Iopr2, Iopr3, Iol1, Ioh1 @3V→ 5V

2007/0702 p.7 : update D.C. Characteristics.
p.29 : update RC oscillator Resistor vs. Frequency table

2007/10/01 p.4 : add 20pin DIP/SOP package

2010/06/11 p.8: update Absolutely max. ratings , Operating Temperature +70℃→ +95℃