Elektronische Bauelemente

SSU90N04-02B

N-Ch Enhancement Mode Power MOSFET

162A, 40V, $R_{DS(ON)}$ 2.3mΩ

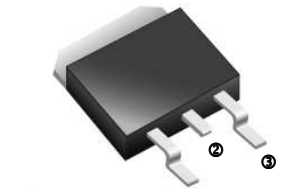
RoHS Compliant Product
A suffix of "-C" specifies halogen free

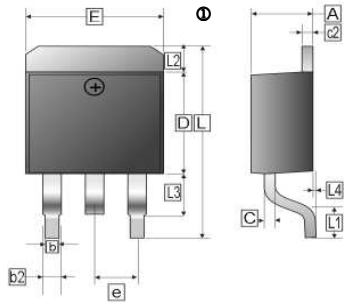
DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

TO-263



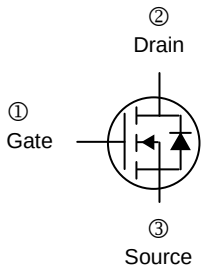


FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe DPAK saves board space.
- Fast switching speed.
- High performance trench technology.

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.00	4.85	c2	1.10	1.45
b	0.68	1.00	b2	1.34 REF	
L4	0.00	0.30	D	8.0	9.15
C	0.36	0.53	e	2.54 REF	
L3	1.50 REF		L	14.6	15.85
L1	2.29	2.79	L2	1.27 REF	
E	9.60	10.45			

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25℃	I_D	162	A
Pulsed Drain Current [2]		I_{DM}	360	A
Continuous Source Current (Diode Conduction) [1]	T_C=25℃	I_S	90	A
Total Power Dissipation	T_C=25℃	P_D	234	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	℃
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient [3]		$R_{\theta JA}$	43	℃ / W
Maximum Thermal Resistance Junction-Case		$R_{\theta JC}$	0.64	℃ / W

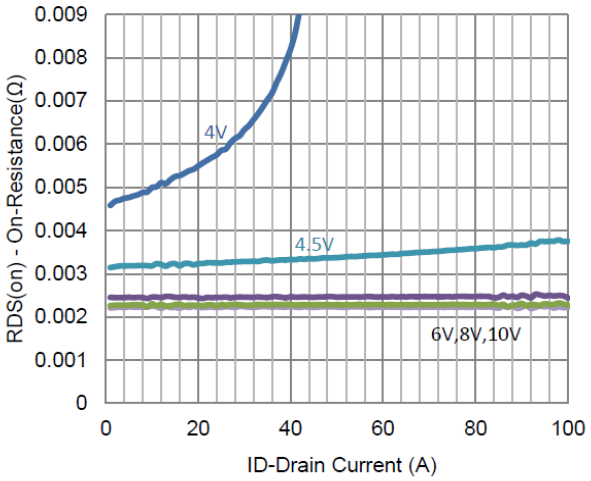
Note:
1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A
2. Pulse width limited by maximum junction temperature
3. Surface Mounted on 1" x 1" FR4 Board.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

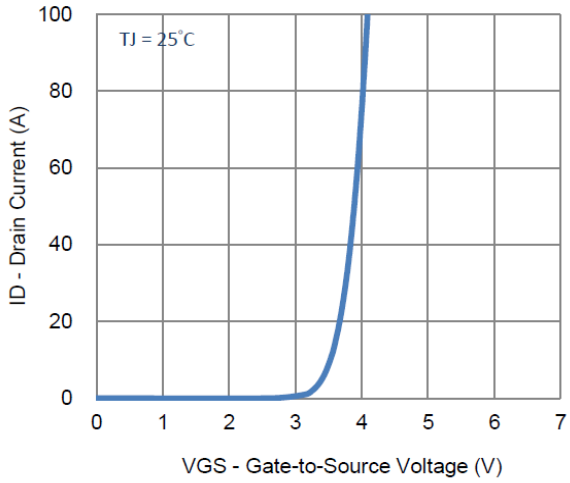
Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	V_{DS}= V_{GS}, I_D = 250 μA
Gate-Body Leakage	I_{GSS}	-	-	±100	nA	V_{DS} = 0V, V_{GS}= ±20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS}= 32V, V_{GS}= 0V
		-	-	25		V_{DS}= 32V, V_{GS}= 0V, T_J=55℃
On-State Drain Current [1]	$I_{D(on)}$	120	-	-	A	V_{DS} = 5V, V_{GS}= 10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	2.3	mΩ	V_{GS}= 10V, I_D= 45A
		-	-	3		V_{GS}= 5.5V, I_D= 44A
Forward Transconductance [1]	g_{fs}	-	35	-	S	V_{DS}=15V, I_D=20A
Diode Forward Voltage[1]	V_{SD}	-	0.82	-	V	I_S=45A, V_{GS}= 0 V
Dynamic [2]						
Input Capacitance	C_{iss}	-	24600	-	pF	V_{GS} =0 V_{DS}=15V f =1.0MHz
Output Capacitance	C_{oss}	-	1560	-		
Reverse Transfer Capacitance	C_{rss}	-	1470	-		
Total Gate Charge	Q_g	-	138	-	nC	V_{DS} = 20V V_{GS} = 5.5 V I_D = 20A
Gate-Source Charge	Q_{gs}	-	52	-		
Gate-Drain Charge	Q_{gd}	-	57	-		
Turn-on Delay Time	$T_{d(on)}$	-	54	-	nS	V_{DS}= 20V I_D= 20A V_{GEN} = 10 V R_L= 1 Ω R_{GEN}= 6 Ω
Rise Time	T_r	-	85	-		
Turn-off Delay Time	$T_{d(off)}$	-	254	-		
Fall Time	T_f	-	86	-		

Notes:
1. Pulse test：Pulse width≦300 μs, duty cycle≦2%.
2. Guaranteed by design, not subject to production testing.

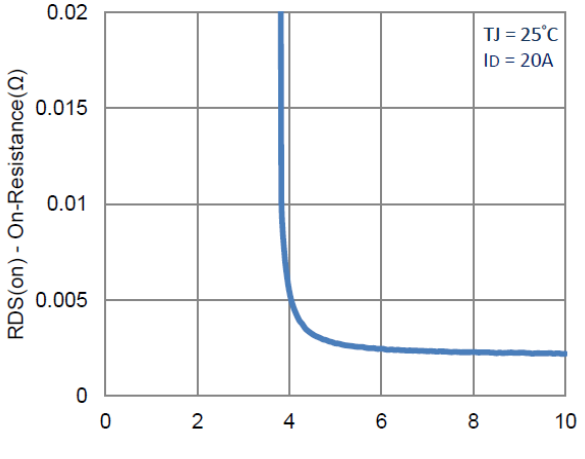
CHARACTERISTIC CURVE



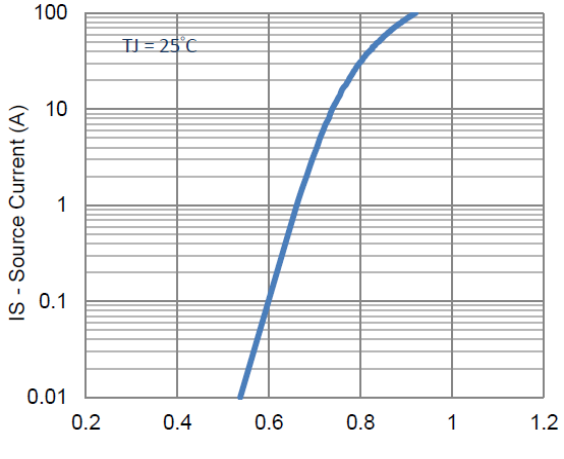
1. On-Resistance vs. Drain Current



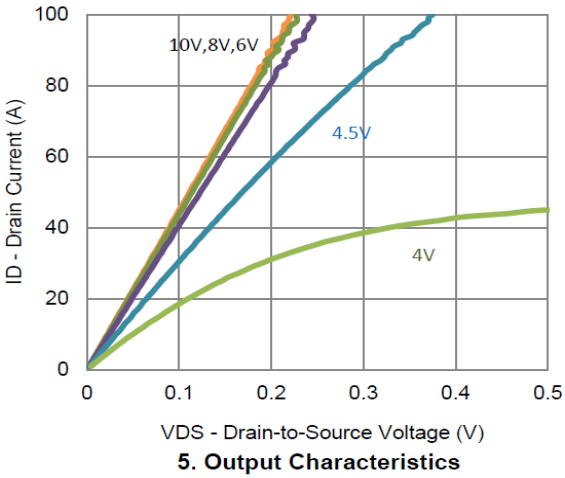
2. Transfer Characteristics



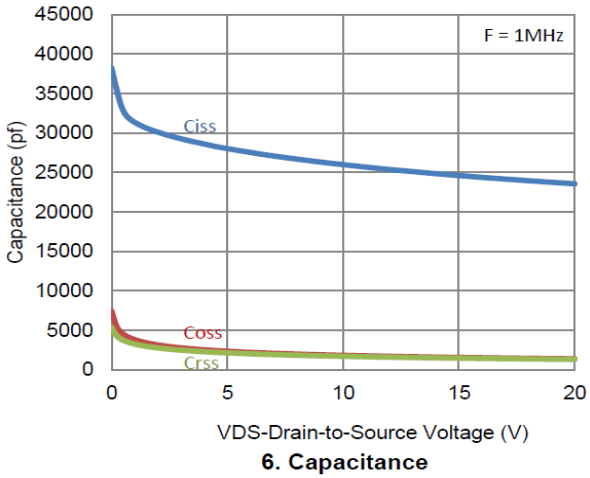
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

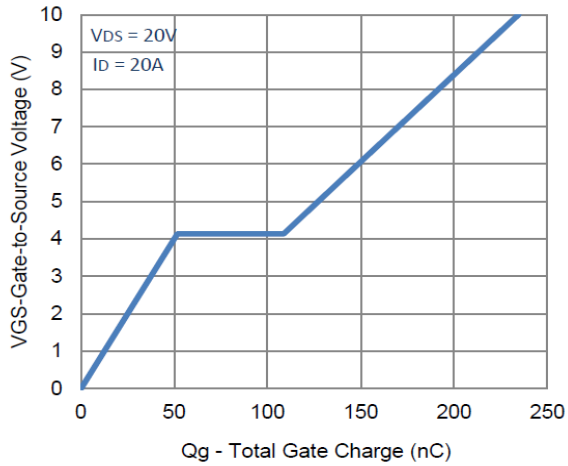


5. Output Characteristics

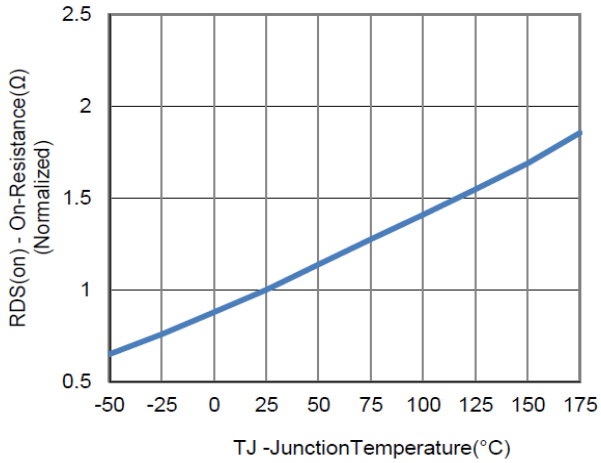


6. Capacitance

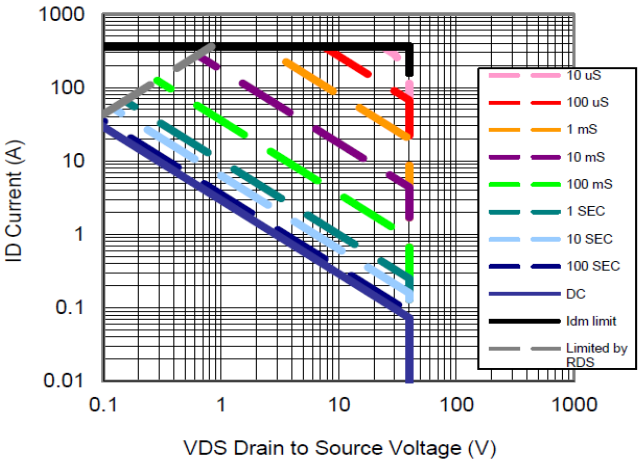
CHARACTERISTIC CURVE



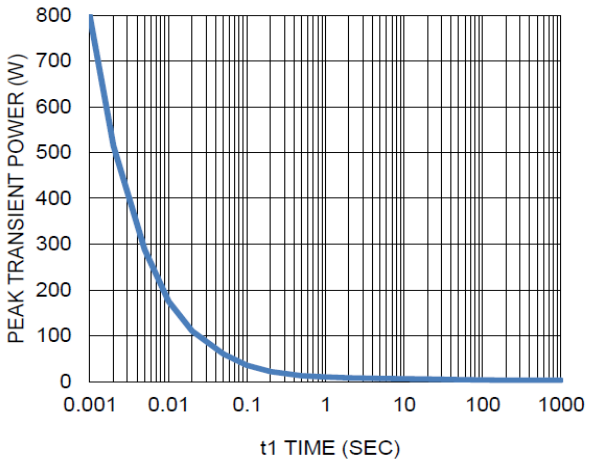
7. Gate Charge



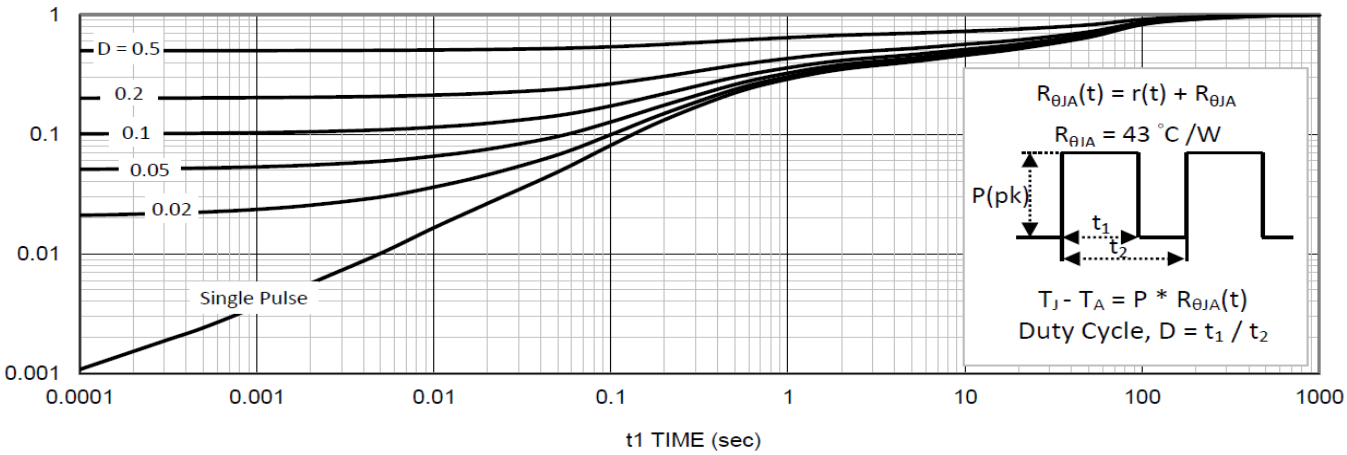
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area



10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient