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TN0973
Technical note

Safety application guide for SPC56EL54xx/SPC56EL60xx family reference manual addendum

Introduction

This document is an addendum of SPC56EL54xx/SPC56EL60xx Safety Application Guide.

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1 Purpose and scope

The purpose of this document is to communicate to ST customers who intend to integrate SPC56EL54xx/SPC56EL60xx in an ASIL-D Item some additional assumptions which shall be met at item level to preserve the SPC56EL54xx/SPC56EL60xx integrity. The assumptions described in this document shall be intended as additional assumptions with respect to those communicated in the SPC56EL54xx/SPC56EL60xx Safety Application Guide.

2 Considerations on SPC56EL54xx/SPC56EL60xx package and soldering procedures

2.1 Introduction

SPC56EL54xx/SPC56EL60xx package is composed by Ultra Low Alpha mold compound. Measurements report an alpha particle emissivity of 0.00383 ± 0.00056 cp/h/cm^2.

This value has been used in the SPC56EL54xx/SPC56EL60xx quantitative safety analyses (see SPC56EL54xx/SPC56EL60xx FMEDA).

In order to ensure that this value does not increase when soldering the device on a board, a risk analysis is made in the following chapter. The conclusions of this analysis report that some caution must take during soldering process in order to avoid package delamination, hence avoiding any contamination from the soldering material to the silicon contained in the plastic package.

2.2 Risk analysis

2.2.1 Risk item

Single Event Upset randomly induced by alpha particle emission from Package material

2.2.2 Cause

A possible cause of silicon contamination is the presence of potentially alpha-emissive soldering material, specifically induced by Pb impurities.

2.2.3 Risk evaluation

Assuming that no delamination is present on the package and given the low migration capability of Pb particles, the risk of having emissive material on the silicon surface is very low.

2.2.4 Item Assumption

We recommend our customers to avoid active soldering flux and to verify the integrity of packages after board mounting in order to eliminate the possibilit y of package delamination after device mounting on board, therefore eliminating the possibility of silicon contamination by soldering material.

3 Revision history

Table 1. Revision history

Date	Revision	Changes
14-Feb-2013	1	Initial release.
17-Sep-2013	2	Updated Disclaimer.

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