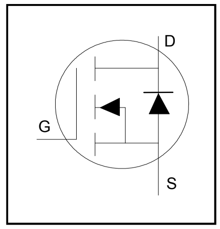
International
IOR Rectifier

AUTOMOTIVE GRADE

AUIRFR8401
AUIRFU8401

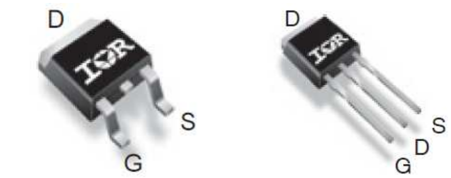
HEXFET® Power MOSFET

Features
- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		**40V**
$R_{DS(on)}$	typ.	**3.2mΩ**
	max	**4.25mΩ**
I_D (Silicon Limited)		**100A①**
I_D (Package Limited)		**100A**

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



D-Pak AUIRFR8401 | I-Pak AUIRFU8401

G	D	S
Gate	Drain	Source

Applications
- Electric Power Steering (EPS)
- Battery Switch
- Start /Stop Micro Hybrid
- Heavy Loads
- DC-DC Converter

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AIRFR8401	D-Pak	Tube	75	AUIRFR8401
		Tape and Reel	2000	AUIRFR8401TR
		Tape and Reel Left	3000	AUIRFR8401TRL
		Tape and Reel Right	3000	AUIRFR8401TRR
AUIRFU8401	I-Pak	Tube	75	AUIRFU8401

Absolute Maximum Ratings
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	100①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	71	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	100	
I_{DM}	Pulsed Drain Current ②	400	
P_D @T_C = 25°C	Maximum Power Dissipation ⑤	79	W
	Linear Derating Factor ⑤	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

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*Qualification standards can be found at http://www.irf.com/

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Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	67	mJ
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑩	94	
I_{AR}	Avalanche Current ②	See Fig 14, 15, 24a, 24b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	——	1.9	°C/W
$R_{\theta CS}$	Junction-to-Ambient (PCB Mounted)⑧	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.035	——	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.2	4.25	mΩ	V_{GS} = 10V, I_D = 60A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	——	3.9	V	$V_{DS} = V_{GS}$, I_D = 50μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	150	μA	V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Reverse Leakage	——	——	-100	nA	V_{GS} = -20V
R_G	Internal Gate Resistance	——	2.0	——	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	198	——	——	S	V_{DS} = 10V, I_D = 60A
Q_g	Total Gate Charge	——	42	63		I_D = 60A
Q_{gs}	Gate-to-Source Charge	——	12	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	14	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	28	——		
$t_{d(on)}$	Turn-On Delay Time	——	7.9	——	ns	V_{DD} = 20V
t_r	Rise Time	——	34	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	25	——		R_G = 2.7Ω
t_f	Fall Time	——	24	——		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	——	2200	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	340	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	205	——		f = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ⑦	——	410	——		V_{GS} = 0V, V_{DS} = 0V to 32V , See Fig. 11 ⑦
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥	——	495	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Package limit current is 100A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.037mH R_G = 50Ω, I_{AS} = 60A, V_{GS} =10V.

④ $I_{SD} \leq$ 60A, di/dt $\leq$ 918A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

⑤ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ R_θ is measured at T_J approximately 90°C.

⑩ This value determined from sample failure population, starting T_J = 25°C, L=0.037mH, R_G = 25Ω, I_{AS} = 60A, V_{GS} =10V.

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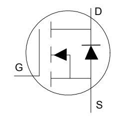
Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)①	—	—	100①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 60A, V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery dv/dt④	—	3.2	—	V/ns	T_J = 175°C, I_S =60A, V_{DS} = 40V④
t_{rr}	Reverse Recovery Time	—	28	—	ns	T_J = 25°C V_{DD} = 34V
		—	29	—		T_J = 125°C I_F = 60A,
Q_{rr}	Reverse Recovery Charge	—	28	—	nC	T_J = 25°C di/dt = 100A/μs ⑤
		—	31	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	1.6	—	A	T_J = 25°C

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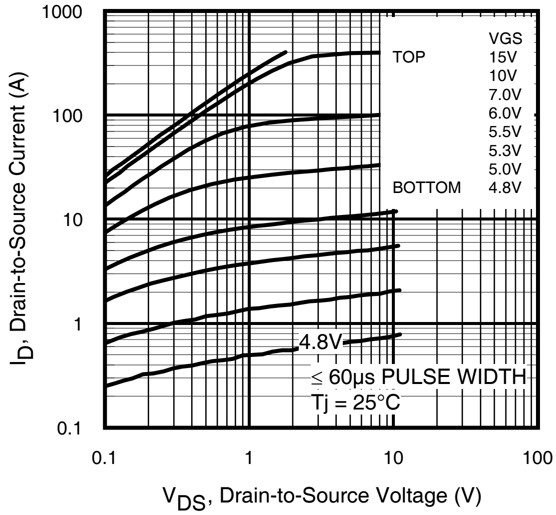

Fig 1. Typical Output Characteristics

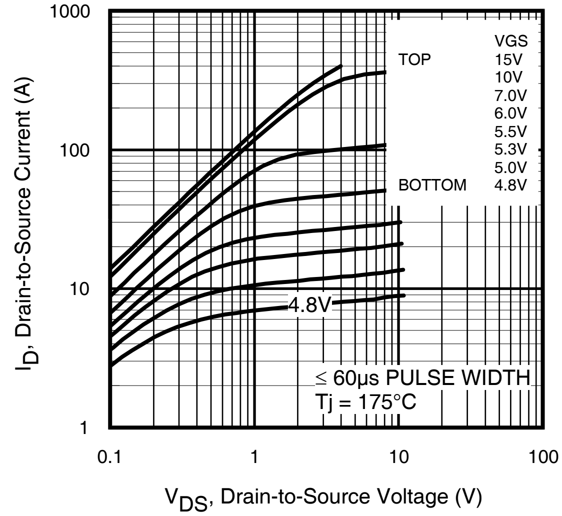

Fig 2. Typical Output Characteristics

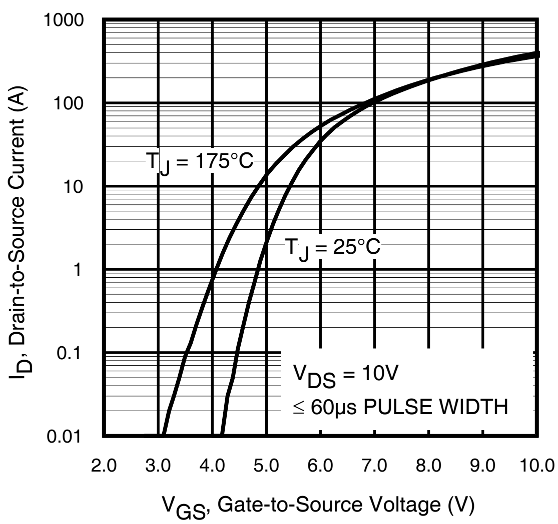

Fig 3. Typical Transfer Characteristics

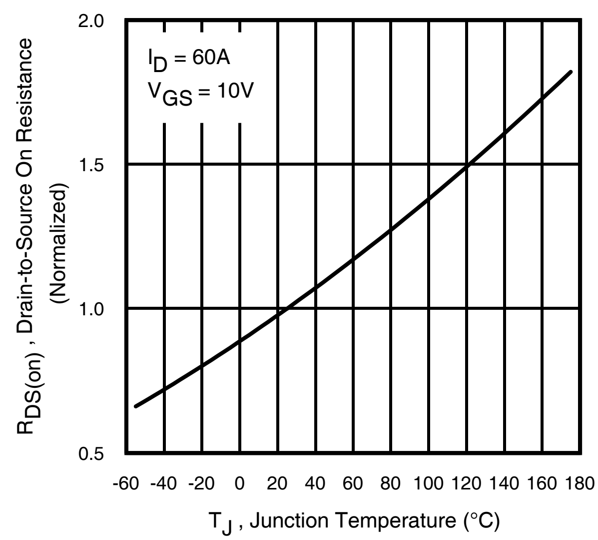

Fig 4. Normalized On-Resistance vs. Temperature

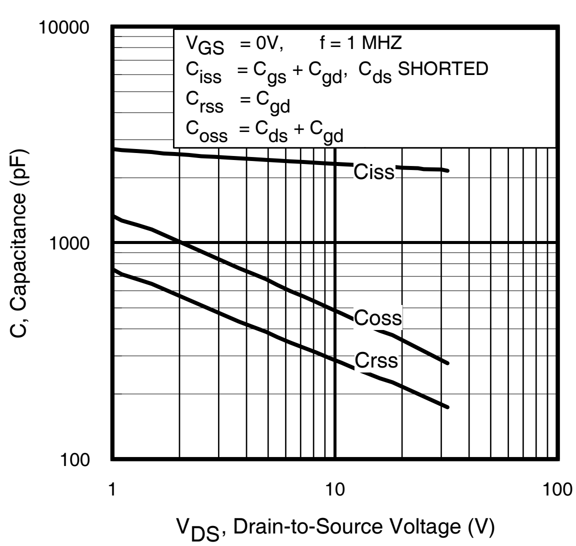

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

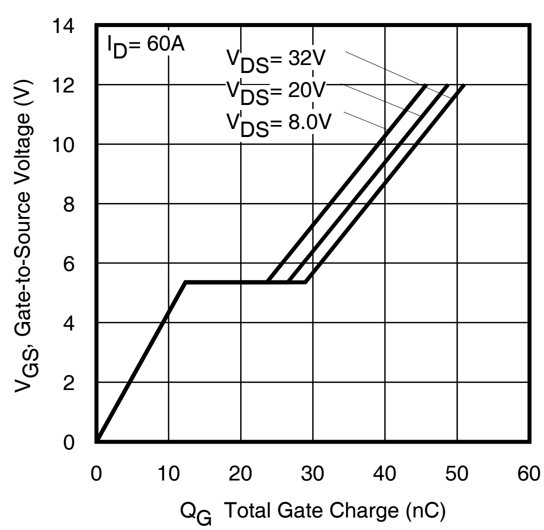

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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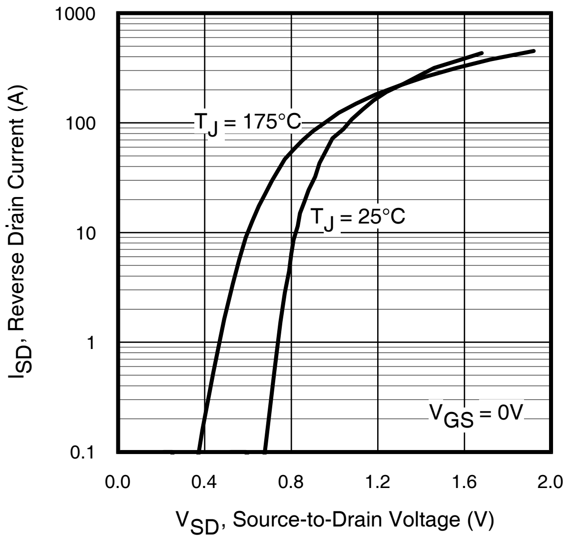

Fig 7. Typical Source-Drain Diode Forward Voltage

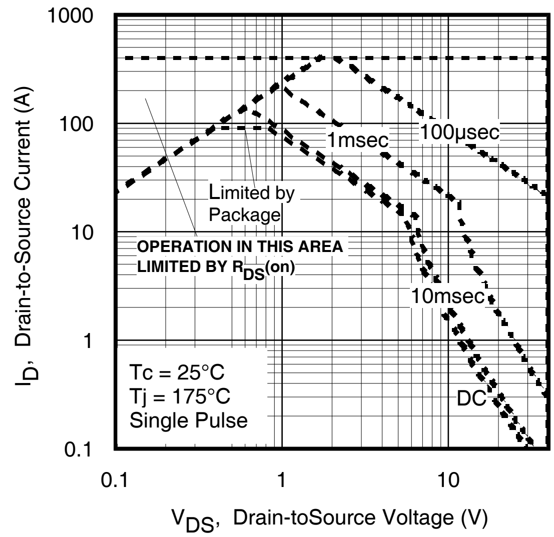

Fig 8. Maximum Safe Operating Area

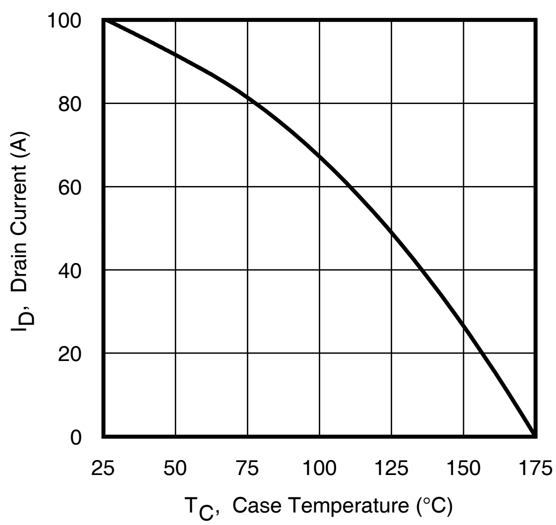

Fig 9. Maximum Drain Current vs. Case Temperature

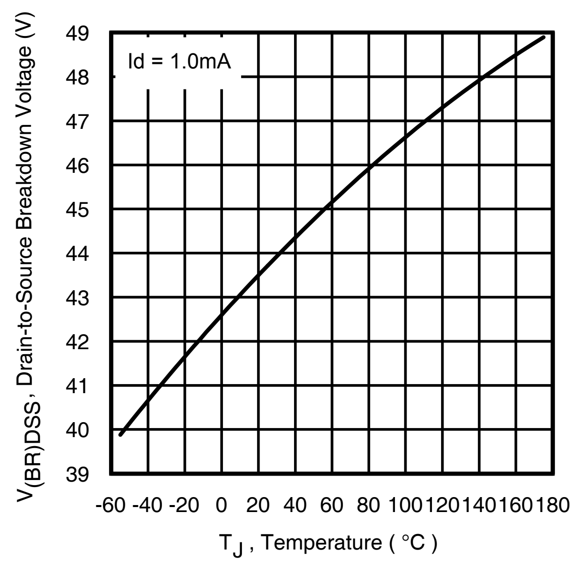

Fig 10. Drain-to-Source Breakdown Voltage

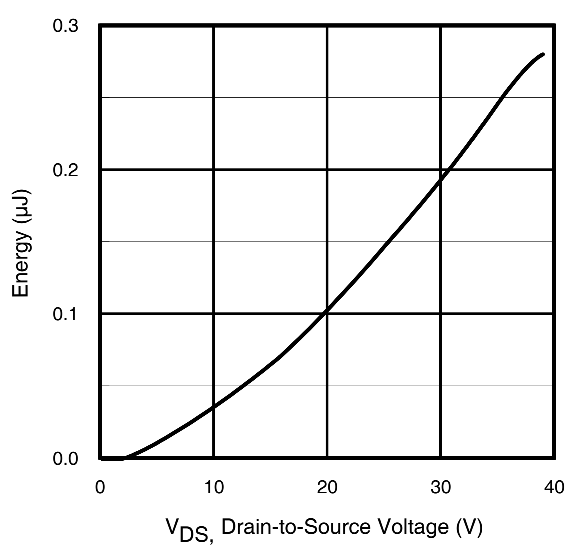

Fig 11. Typical Coss Stored Energy

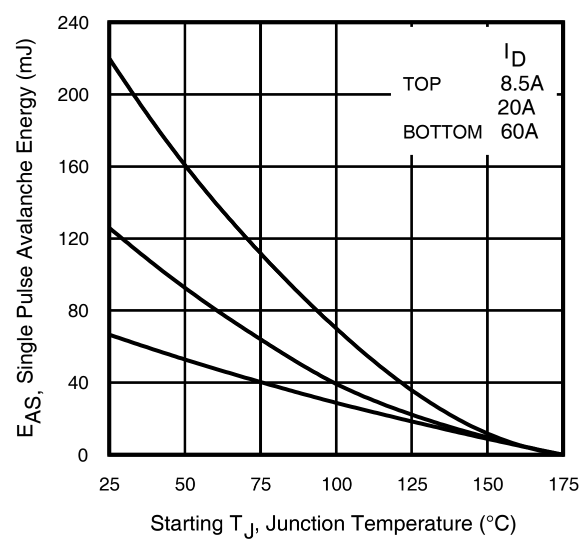

Fig 12. Maximum Avalanche Energy vs. Drain Current

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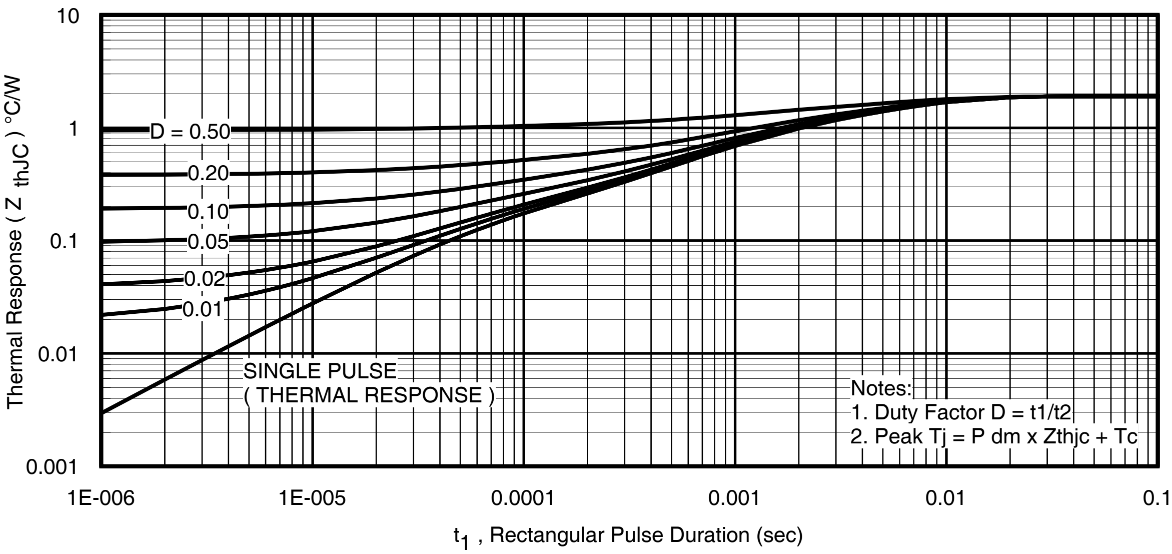

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

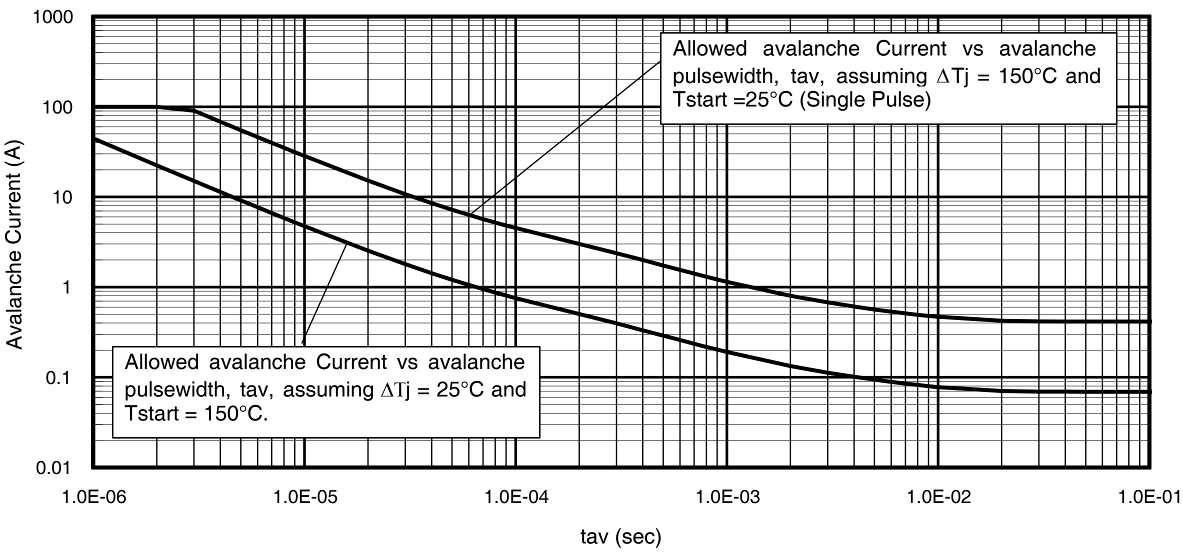

Fig 14. Typical Avalanche Current vs.Pulsewidth

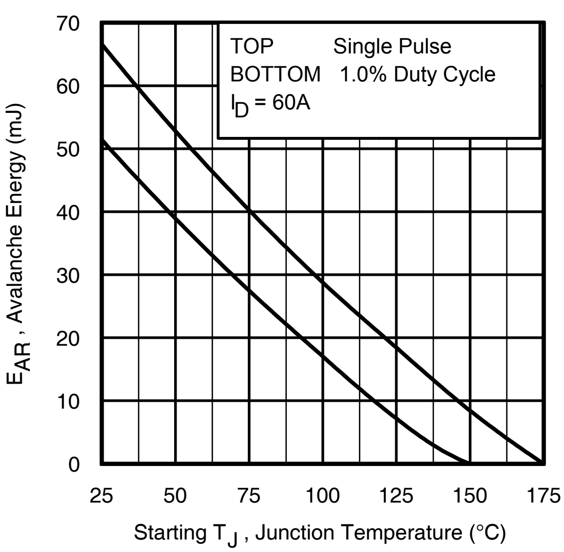

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asTjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. PD (ave) = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. Iav = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f

$Z_{thJC}(D, t_{av})$= Transient thermal resistance, see Figures 14)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot Iav) = \Delta T / Z_{thJC}$$
$$Iav = 2\Delta T / [1.3 \cdot BV \cdot Zth]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

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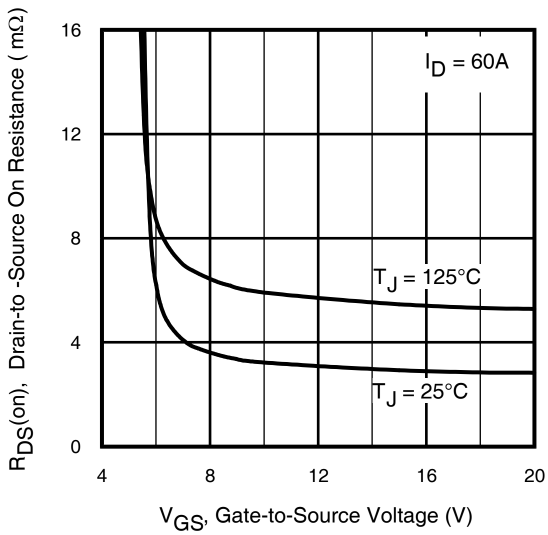

Fig 16. Typical On-Resistance vs. Gate Voltage

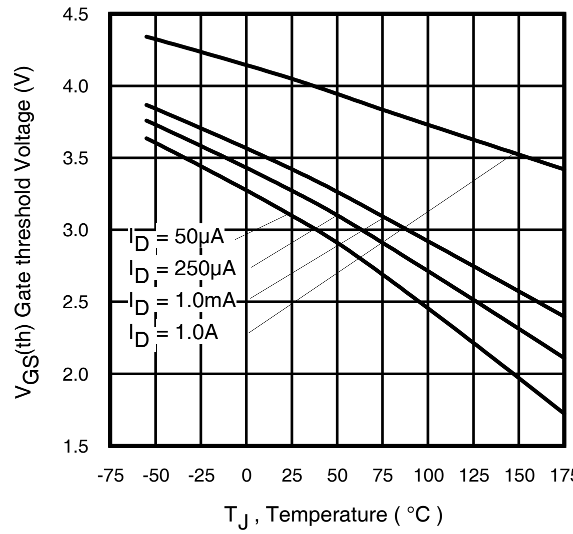

Fig 17. Threshold Voltage vs. Temperature

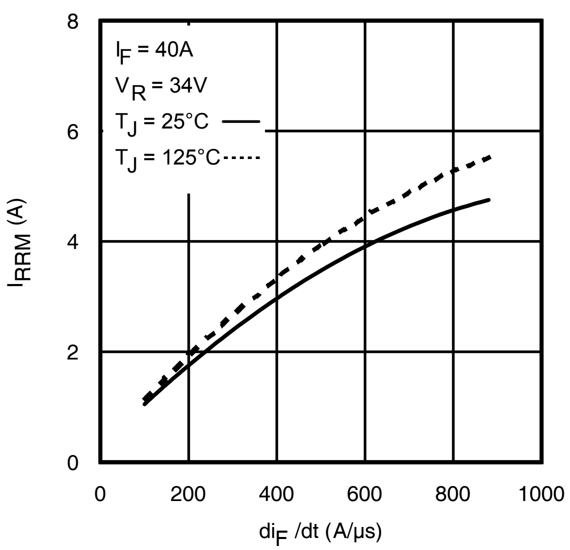

Fig. 18 - Typical Recovery Current vs. dif/dt

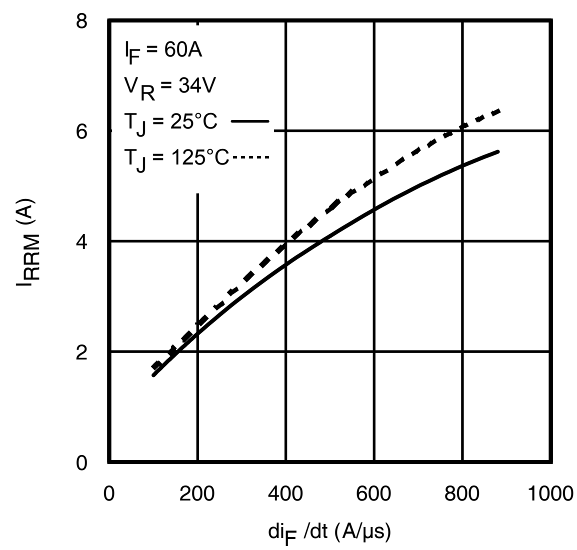

Fig. 19 - Typical Recovery Current vs. dif/dt

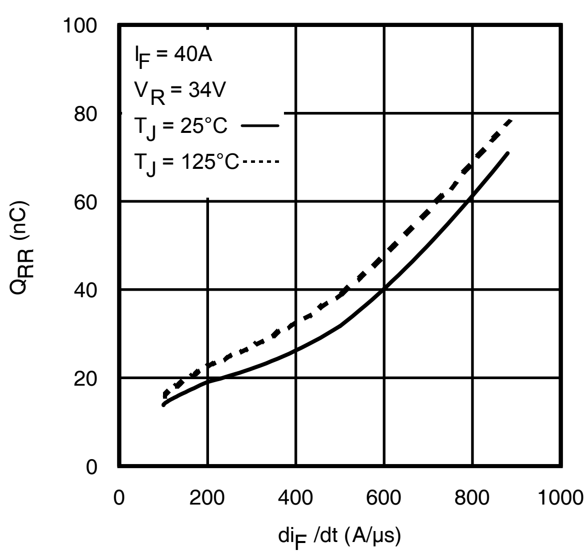

Fig. 20 - Typical Stored Charge vs. dif/dt

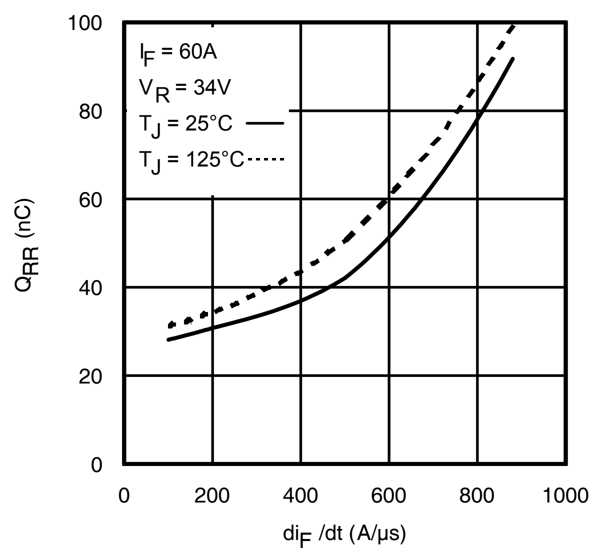

Fig. 21 - Typical Stored Charge vs. dif/dt

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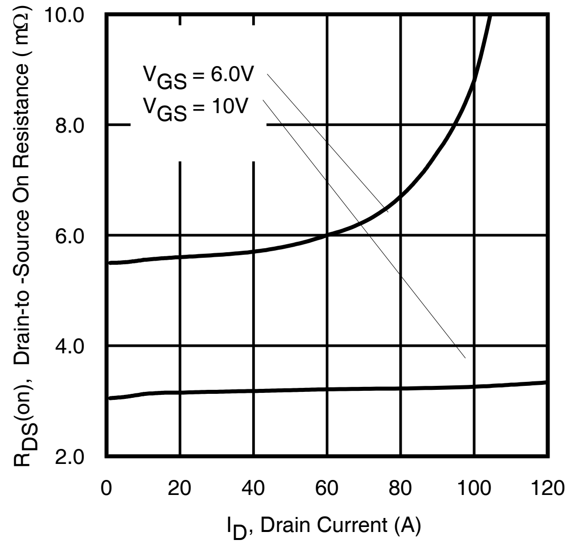

Fig 22. Typical On-Resistance vs. Drain Current

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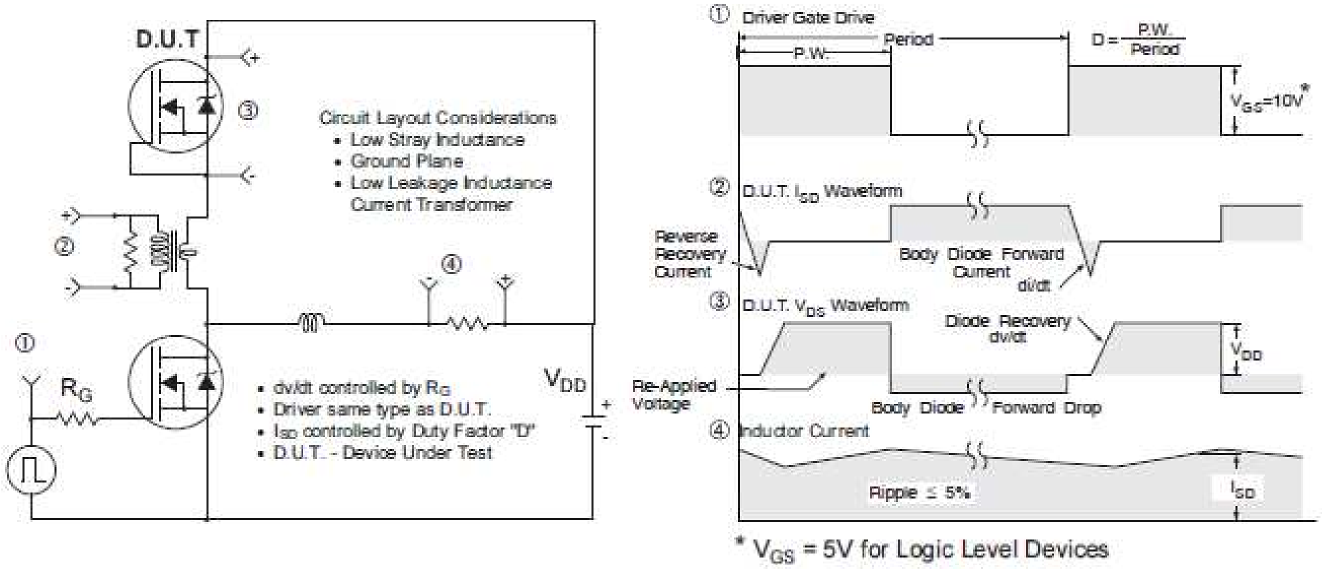

Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

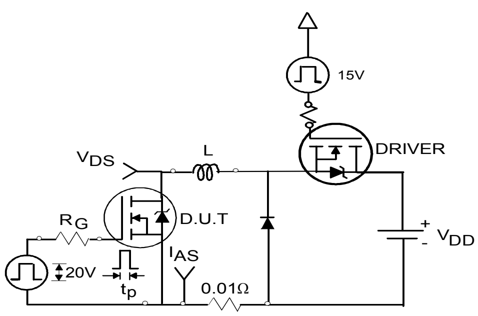

Fig 24a. Unclamped Inductive Test Circuit

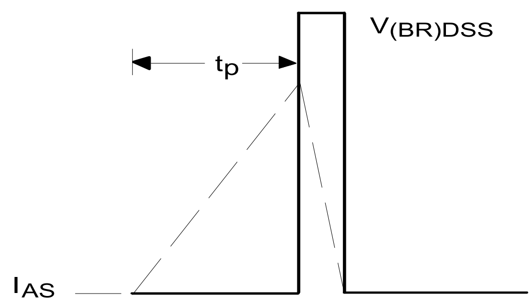

Fig 24b. Unclamped Inductive Waveforms

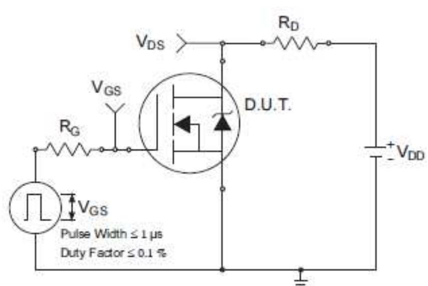

Fig 25a. Switching Time Test Circuit

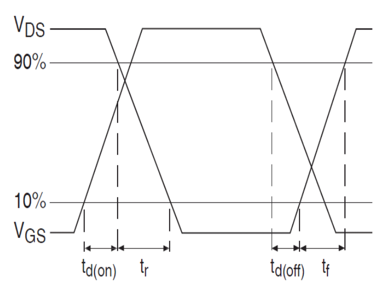

Fig 25b. Switching Time Waveforms

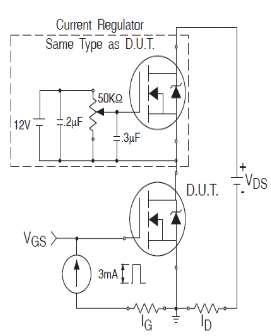

Fig 26a. Gate Charge Test Circuit

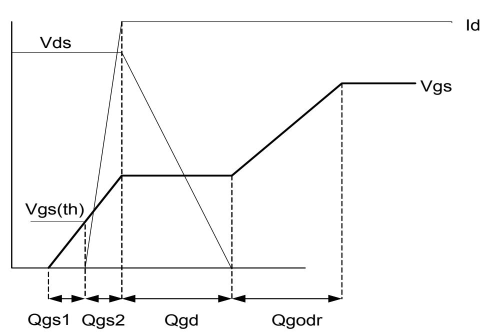

Fig 26b. Gate Charge Waveform

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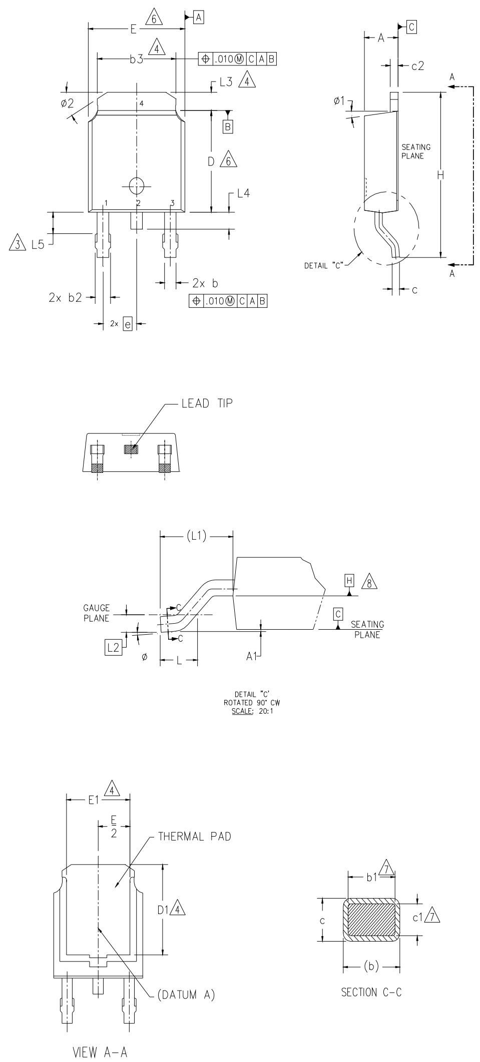
D-Pak (TO-252AA) Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

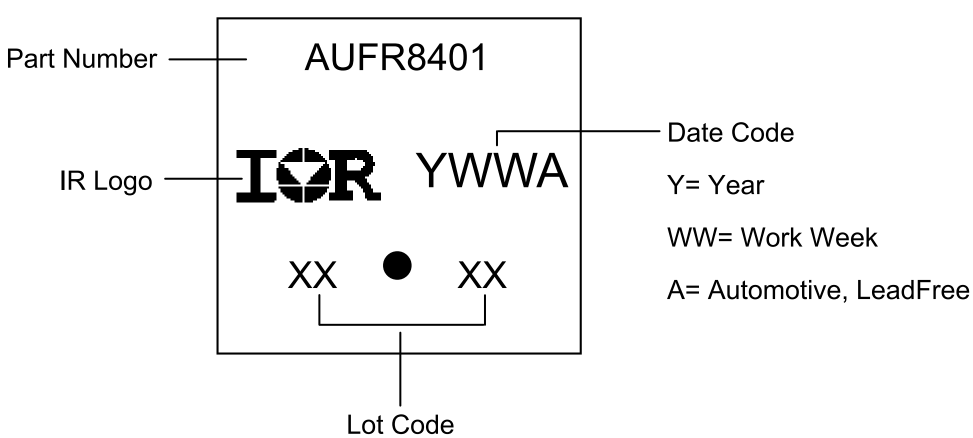
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT & CoPAK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) **Part Marking Information**



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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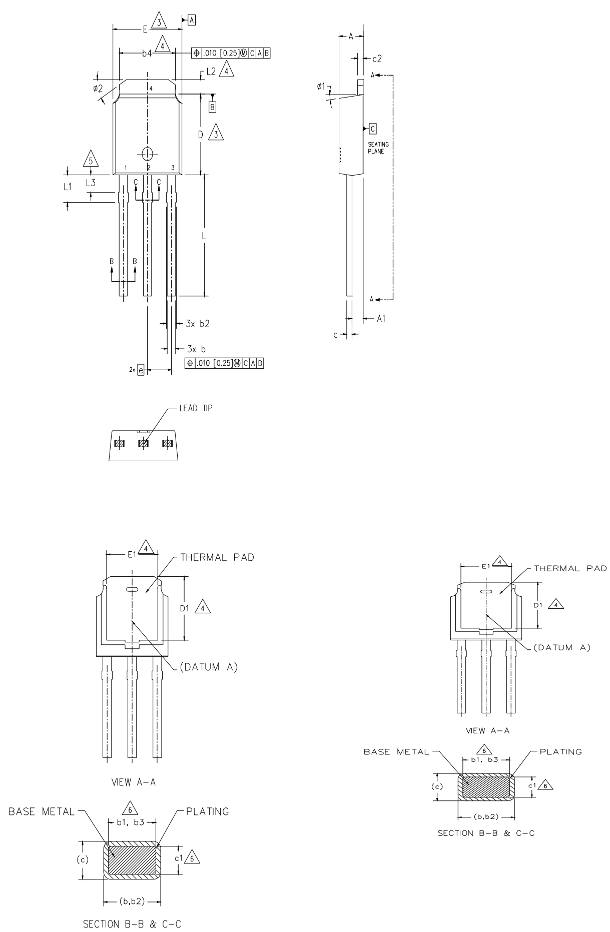
I-Pak (TO-251AA) Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

5.- LEAD DIMENSION UNCONTROLLED IN L3.

6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).

8.- CONTROLLING DIMENSION : INCHES.

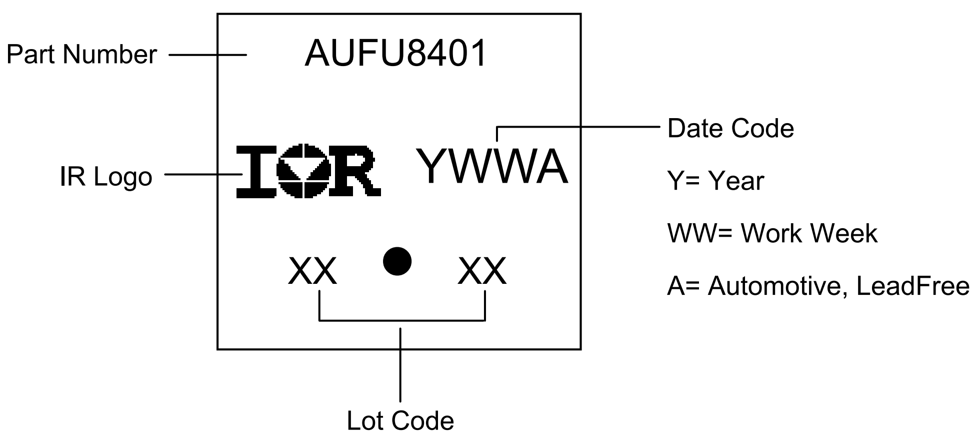
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

I-Pak (TO-251AA) **Part Marking Information**



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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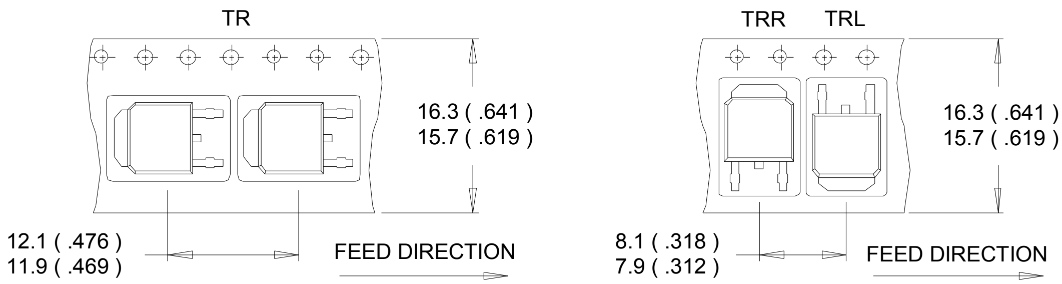
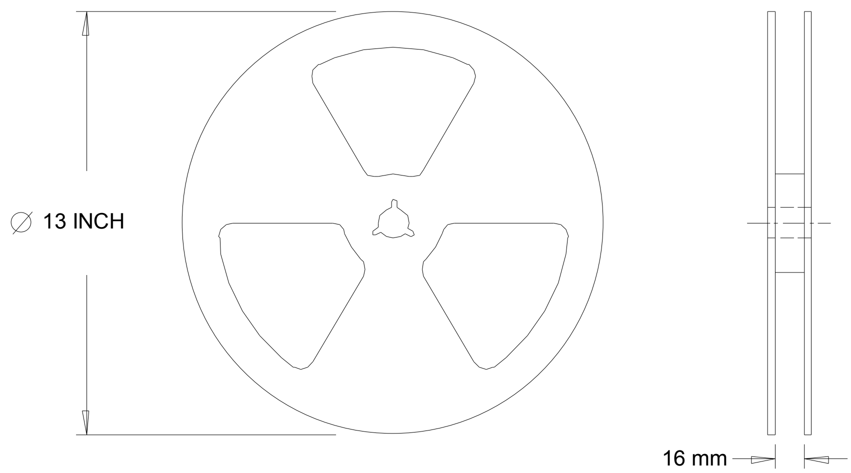
D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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Qualification Information†

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		3L-D-PAK	MSL1
		I-PAK	N/A
ESD	Machine Model	Class M2 (+/- 200)†† AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000)†† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000)†† AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Highest passing voltage.

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