2GB – 2x128Mx72 DDR2 SDRAM UNBUFFERED, ECC w/PLL

FEATURES

- 200-pin, dual in-line memory module (SO-DIMM)
- Support ECC error detection and correction
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- Package option
  - 200 Pin SO-DIMM
  - PCB – 30.00mm (1.181") Max

DESCRIPTION

The WV3HG2128M72EEU is a 2x128Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eighteen 128Mx8 bit stacked BGA with 8 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-6400*	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	400MHz	333MHz	266MHz	200MHz
CL-t_{RCD}-t_{RP}	6-6-6	5-5-5	4-4-4	3-3-3

PIN CONFIGURATION

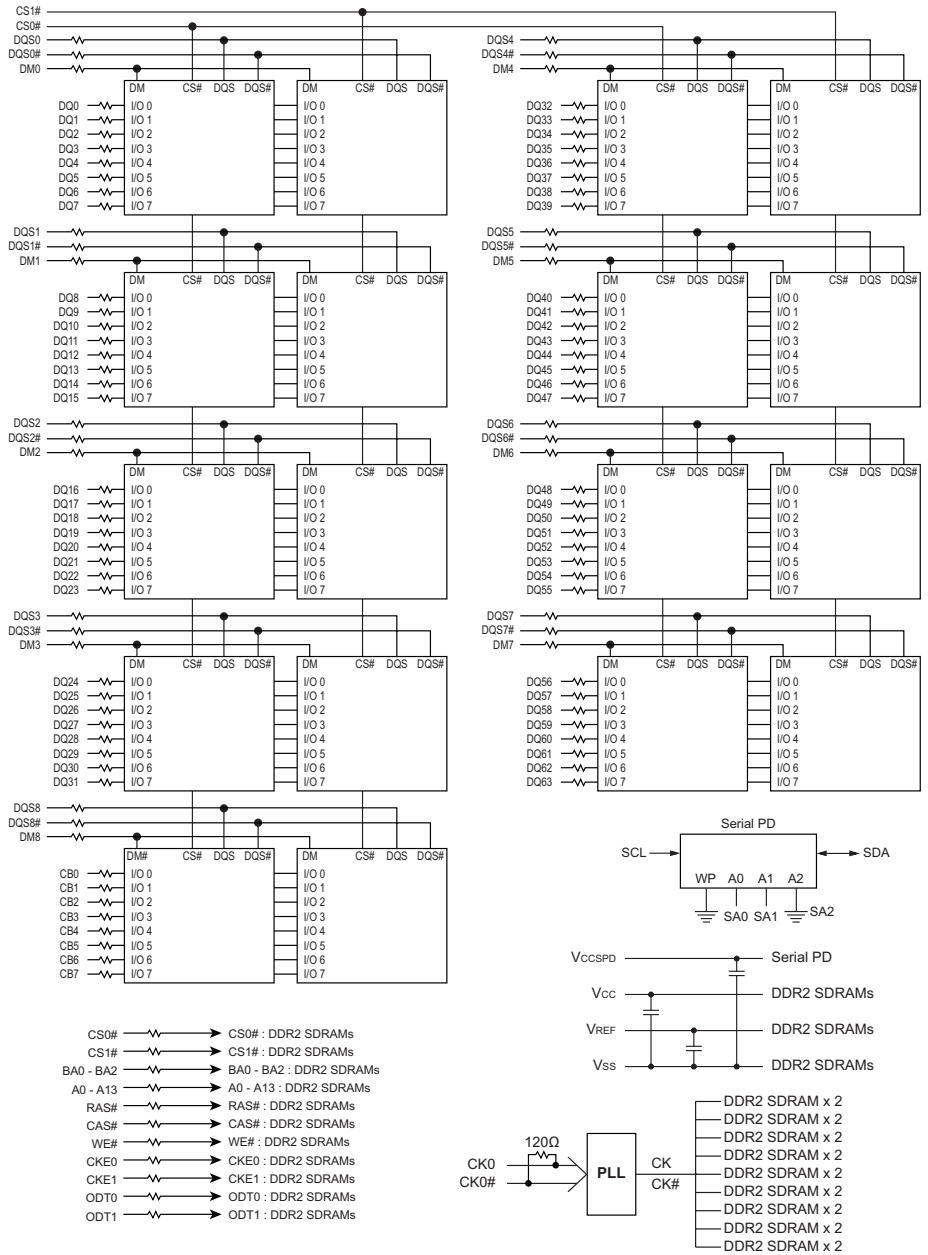
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	51	DQ18	101	V_{CC}	151	V_{SS}
2	V_{SS}	52	V_{SS}	102	A6	152	V_{SS}
3	DQ0	53	DQ19	103	A5	153	DQS5#
4	DQ4	54	DQ28	104	A4	154	DM5
5	V_{SS}	55	V_{SS}	105	A3	155	DQS5
6	DQ5	56	DQ29	106	V_{CC}	156	V_{SS}
7	DQ1	57	DQ24	107	A2	157	V_{SS}
8	V_{SS}	58	V_{SS}	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	V_{CC}	159	DQ42
10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	V_{SS}	111	A10/AP	161	DQ43
12	V_{SS}	62	V_{SS}	112	BA1	162	V_{SS}
13	V_{SS}	63	DQS3#	113	BA0	163	V_{SS}
14	DQ6	64	DQ30	114	V_{CC}	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48
16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	V_{SS}	117	V_{CC}	167	DQ49
18	V_{SS}	68	V_{SS}	118	CS0#	168	V_{SS}
19	V_{SS}	69	DQ26	119	CAS#	169	V_{SS}
20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	CS1#	171	DQS6#
22	DQ13	72	CB5	122	A13	172	V_{SS}
23	DQ9	73	V_{SS}	123	V_{CC}	173	DQS6
24	V_{SS}	74	V_{SS}	124	V_{CC}	174	DQ54
25	V_{SS}	75	CB0	125	ODT1	175	V_{SS}
26	DM1	76	DM8	126	CK	176	DQ55
27	DQS1#	77	CB1	127	NC/CS3#	177	DQ50
28	V_{SS}	78	V_{SS}	128	CK#	178	V_{SS}
29	DQS1	79	V_{SS}	129	DQ32	179	DQ51
30	DQ14	80	CB6	130	V_{SS}	180	DQ60
31	V_{SS}	81	DQS8#	131	V_{SS}	181	V_{SS}
32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56
34	V_{SS}	84	V_{CC}	134	DQ37	184	V_{SS}
35	DQ11	85	V_{SS}	135	DQS4#	185	DQ57
36	DQ20	86	CB2	136	V_{SS}	186	DM7
37	V_{SS}	87	CKE0	137	DQS4	187	V_{SS}
38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	CKE1	139	V_{SS}	189	DQS7#
40	V_{SS}	90	V_{SS}	140	V_{SS}	190	V_{SS}
41	DQ17	91	NC/CS2#	141	DQ34	191	DQS7
42	NC	92	BA2	142	DQ38	192	DQ63
43	V_{SS}	93	V_{CC}	143	DQ35	193	DQ58
44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	V_{SS}	195	V_{SS}
46	V_{SS}	96	A11	146	V_{SS}	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59
48	DQ22	98	V_{CC}	148	DQ44	198	SA1
49	V_{SS}	99	A7	149	DQ41	199	V_{CC}SPD
50	DQ23	100	A8	150	DQ45	200	SA0

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
A10/AP	Address Input/Auto Precharge
BA0 - BA2	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes negative
ODT0, ODT1	On-die termination control
CK,CK#	Clock inputs, positive/negative
CKE0, CKE1	Clock enable input
CS0#, CS1#	Chip select input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
V_{CC}	Core Power (1.8V)
V_{SS}	Ground
SA0-SA1	SPD address
SDA	Serial Data Input/Output
V_{REF}	Input/Output Reference
DM0-DM8	Data-in mask
V_{CCSPD}	Serial EEPROM power supply
SCL	Serial Presence Detect(SPD) Clock Input
NC	No Connect

NOTES:
SA2 does NOT connect to memory connector and is shown ONLY on Block Diagram
SA2 is tied LOW on memory module for all memory configurations

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	˚C
T_{CASE}	Device operating Temperature		0	85	˚C
I_L	Input leakage current; Any input $0V<V_{IN}<V_{CC}$; V_{REF} input $0V<V_{IN}<0.95V$; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-90	90	µA
		CKE, CS#, ODT	-45	45	µA
		CK,CK#	-10	10	µA
		DM	-10	10	
I_{OZ}	Output leakage current; $0V<V_{IN}<V_{CCQ}$; DQs and ODT are disable	DQ, DQS, DQS#	-10	10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-36	36	µA

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.50 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	2

Notes:

1 V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.

2. V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0° to 85°	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(AC)	V_{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V_{IH}(AC)	V_{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(AC)	-	V_{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667	V_{IL}(AC)	-	V_{REF} - 0.200	V

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	C_{IN1}	22	40	pF
Input Capacitance (CKE0, CKE1), (ODT0, ODT1)	C_{IN2}	13	22	pF
Input Capacitance (CS0# ~ CS1#)	C_{IN3}	13	22	pF
Input Capacitance (CK, CK#)	C_{IN4}	6	7	pF
Input Capacitance (DM0 ~ DM8), (DQS0 ~ DQS8)	C_{IN5} (665)	9	11	pF
	C_{IN5} (534, 403)	9	12	pF
Input Capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	C_{OUT1} (665)	9	11	pF
	C_{OUT1} (534, 403)	9	12	pF

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

$0°C \le T_{CASE} < +70°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

Symbol	Proposed Conditions		806	665	534	403	Units
I_{CC0}*	Operating one bank active-precharge current; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,218	1,173	1,128	mA
I_{CC1}*	Operating one bank active-read-precharge current; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$, $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	1,308	1,263	1,218	mA
I_{CC2P}**	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	516	516	516	mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	1,020	930	930	mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,110	1,020	1,020	mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	840	750	750	mA
		Slow PDN Exit MRS(12) = 1	TBD	516	516	516	mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,200	1,110	1,110	mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,803	1,578	1,443	mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	1,803	1,578	1,443	mA
I_{CC5}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	4,260	4,170	4,080	mA
I_{CC6}**	Self refresh current; CK and CK\ at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		TBD	108	108	108	mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = $t_{RCD}(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I_{CC4R}; Refer to the following page for detailed timing conditions		TBD	3,108	2,928	2,748	mA

Note: I_{CC} specification is based on **SAMSUNG** components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in the operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				806		665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	$t_{CK\ (6)}$	TBD	TBD							ps
		CL = 5	$t_{CK\ (5)}$	TBD	TBD	3,000	8,000					ps
		CL = 4	$t_{CK\ (4)}$	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	TBD	TBD	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}	TBD	TBD		t_{AC} MAX		t_{AC} MAX		t_{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t_{DS}	TBD	TBD	100		100		150		ps
	DQ and DM input hold time relative to DQS		t_{DH}	TBD	TBD	175		225		275		ps
	DQ and DM input pulse width (for each input)		t_{DIPW}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}	TBD	TBD		340		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	TBD	TBD	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising … setup time		t_{DSS}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	TBD	TBD		240		300		350	ps
	DQS read preamble		t_{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	TBD	TBD	0		0		0		p s
	DQS write preamble		t_{WPRE}	TBD	TBD	0.25		0.25		0.25		t_{CK}
	DQS write postamble		t_{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}
	Address and control input pulse width for each input		t_{IPW}	TBD	TBD	0.6		0.6		0.6		t_{CK}
	Address and control input setup time		t_{IS}	TBD	TBD	200		250		350		ps
	Address and control input hold time		t_{IH}	TBD	TBD	275		375		475		ps
	Address and control input hold time		t_{CCD}	TBD	TBD	2		2		2		t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page

AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}	TBD	TBD	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t_{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	TBD	TBD	t_{WR} + t_{RP}		t_{WR} + t_{RP}		t_{WR} + t_{RP}		ns
	Internal WRITE to READ command delay	t_{WTR}	TBD	TBD	7.5		7.5		10		ns
	PRECHARGE command period	t_{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t_{RPA}	TBD	TBD	t_{RP}+t_{CK}		t_{RP}+t_{CK}		t_{RP}+t_{CK}		ns
	LOAD MODE command cycle time	t_{MRD}	TBD	TBD	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	TBD	TBD	t_{IS}+t_{CK} +t_{IH}		t_{IS}+t_{CK} +t_{IH}		t_{IS}+t_{CK} +t_{IH}		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t_{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}	TBD	TBD		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	TBD	TBD	t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t_{XSRD}	TBD	TBD	200		200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	t_{IS}		t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	ps
	ODT turn-off delay	t_{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	TBD	TBD	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	TBD	TBD	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	TBD	TBD	6 - AL		6 - AL		6 - AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	TBD	TBD	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	TBD	TBD	3		3		3		t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

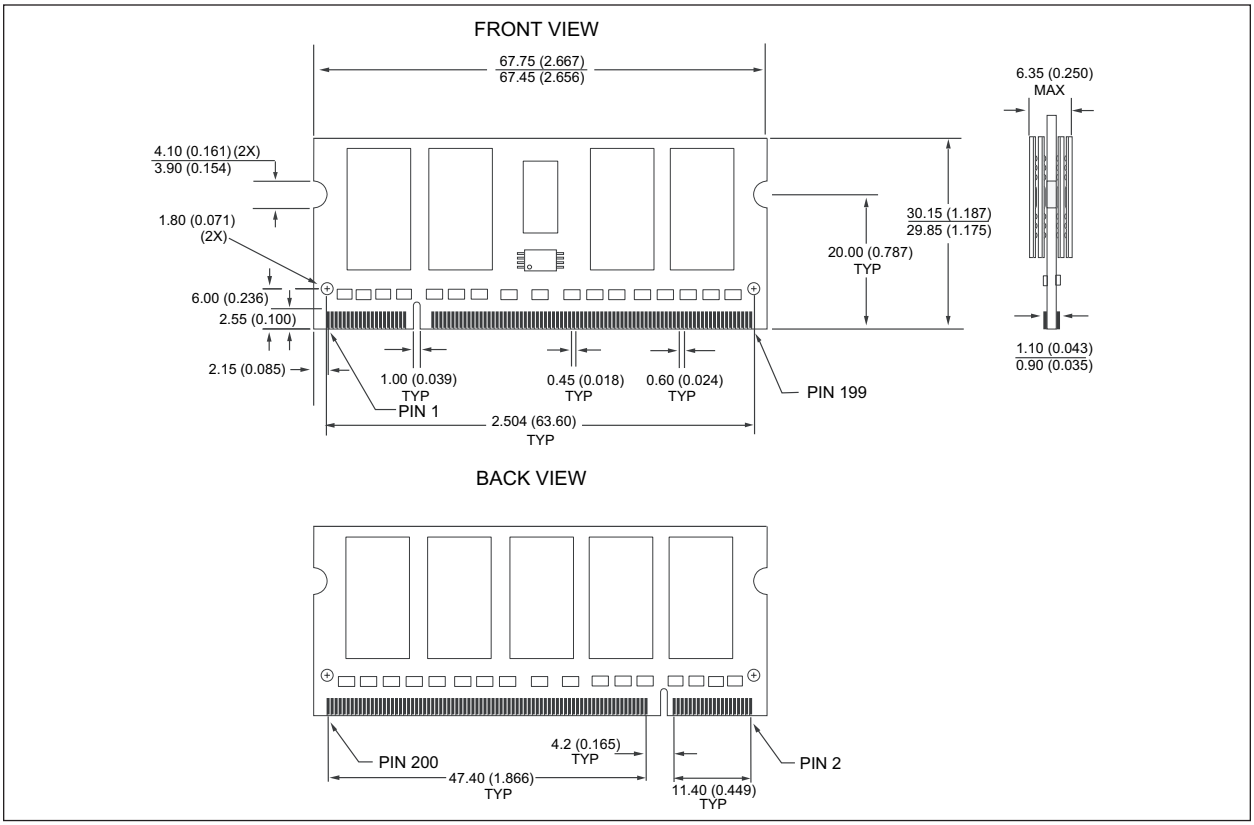
ORDERING INFORMATION FOR D4

Part Number	Clock/Data Rate Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3HG2128M72EEU806AD4-xG	400MHz/800Mb/s	6	6	6	30.00mm (1.181")
WV3HG2128M72EEU665AD4-xG	333MHz/667Mb/s	5	5	5	30.00mm (1.181")
WV3HG2128M72EEU534AD4-xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181")
WV3HG2128M72EEU403AD4-xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181")

NOTES:

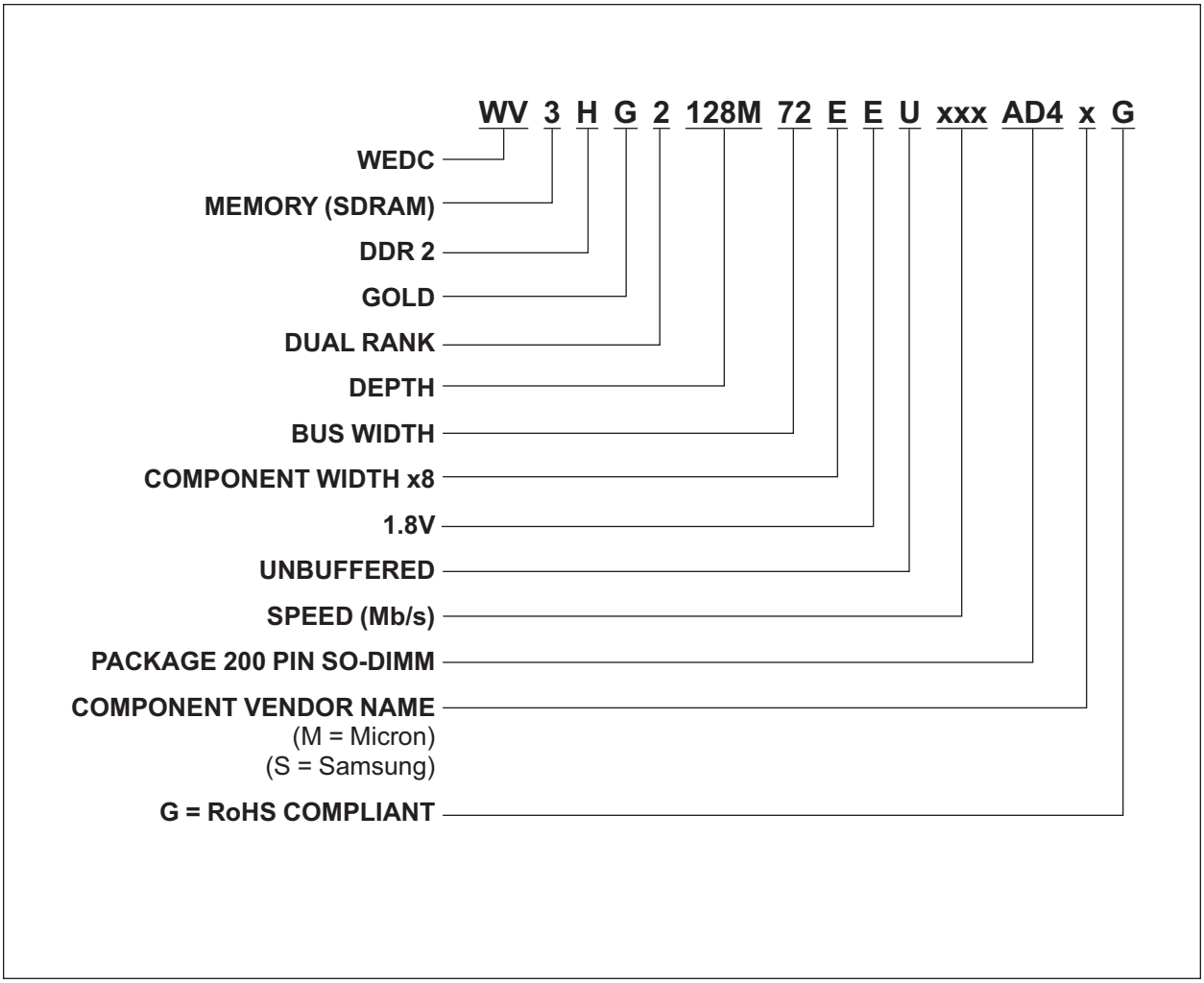
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "-x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR AD4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
Tolerances: ±0.13 (0.005) unless otherwise specified

PART NUMBERING GUIDE



Document Title

2GB – 2x128Mx72 DDR2 SDRAM UNBUFFERED, ECC w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	February 2006	Advanced