AN6296, AN6296S

Peak-Noise-Reduction System for Hi-Fi VTRs and 8mm VTRs

■ Outline

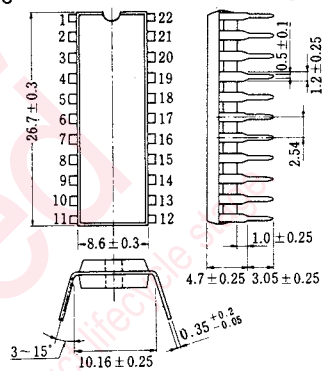
The AN6296 and the AN6296S are peak detection type noise reducing integrated circuits designed for a Hi-Fi VTR and an 8 mm VTR.

It has all the blocks necessary for the noise reduction of a Hi-Fi VHS VTR and an 8 mm VTR built-in. It is possible to manufacture a high performance VTR audio circuit with fewer parts.

■ Features

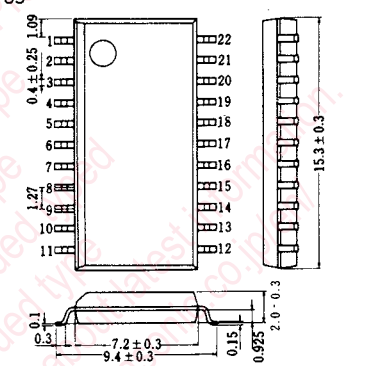
- Excellent matching to 8mm VTR noise-reduction characteristics
- Includes all functions of noise-reduction system
- Minimum number of external components
- Low power consumption

AN6296 Unit : mm



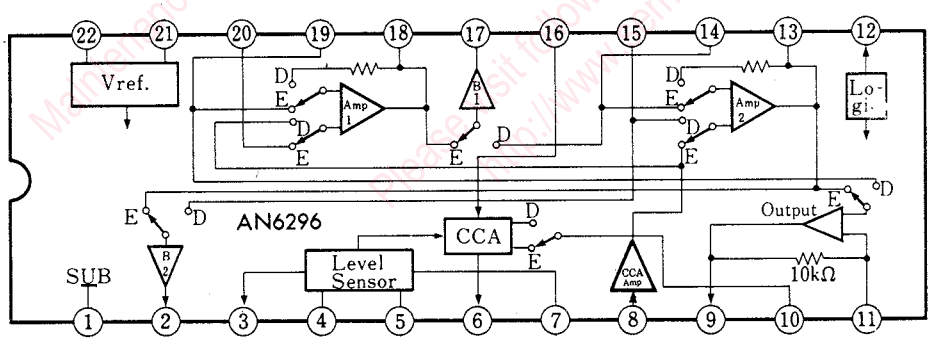
22-Lead DIL Plastic Package

AN6296S Unit : mm



22-Lead PANAFLAT Package (SO-22D)

■ Block Diagram



■ Absolute Maximum Ratings(Ta=25℃)

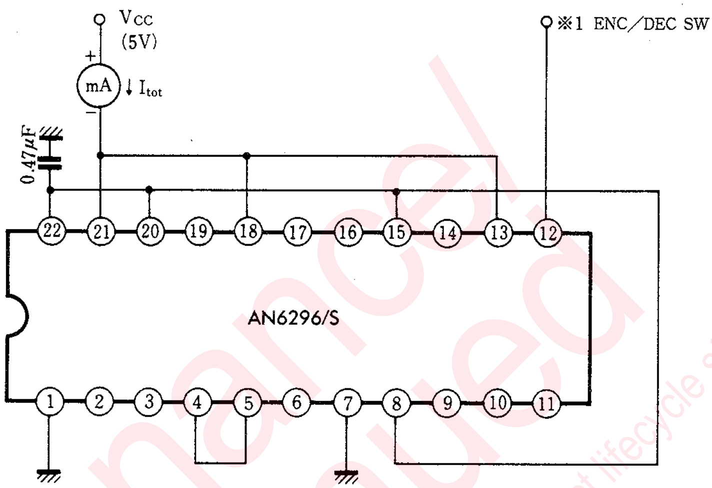
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6	V
Supply Current	I_{CC}	15	mA
Power Dissipation	P_D	90	mW
Operating Ambient Temperature	T_{opr}	−20∼+75	℃
Storage Temperature	T_{stg}	−55∼+125	℃

■ Electrical Characteristics(V_{cc}=5V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Current	I_{tot}	1	Circuit Current with No Signal		5	7	mA
Encode Holding Voltage	V_{SE}		Encode Pin ⑫ Applied Voltage	3.5			V
Decode Holding Voltage	V_{SD}		Decode Pin ⑫ Applied Voltage			1.5	V
Encode Maximum Voltage	V_{OME}	2	f=1kHz, THD=3%	−4	−2		dBV
Decode Maximum Voltage	V_{OMD}	2	f=1kHz, THD=3%	0	1.5		dBV
Encode Distortion Rate	THD_E	2	Vin=1kHz, −8.5dBV (Reference Level)		0.2	0.4	%
Decode Distortion Rate	THD_D	2	Vin=1kHz, −8.5dBV (Reference Level)		0.2	0.4	%
Encode Noise Voltage	V_{NE}	3	Output Voltage in the Case Where Rg=0 DIN AUDIO Filter		−64	−55	dBV
Decode Noise Voltage	V_{ND}	3	Output Voltage in the Case Where Rg=0 DIN AUDIO Filter		−100	−90	dBV
Encode Output Voltage-1	V_{OE1}*1	2	Vin=1kHz, −8.5dBV (Reference Level)	−9.5	−8.5	−7.5	dBV
Encode Output Voltage-2	V_{OE2}	2	Vin=1kHz, −20dBV	−15.3	−14.3	−13.3	dBV
Encode Output Voltage-3	V_{OE3}	2	Vin=1kHz, −40dBV	−25.6	−24.3	−23	dBV
Encode Output Voltage-4	V_{OE4}	2	Vin=1kHz, −60dBV	−35.8	−34.3	−32.8	dBV
Decode Output Voltage-1	V_{OD1}*1	2	Vin=1kHz, −8.5dBV (Reference Level)	−9.5	−8.5	−7.5	dBV
Decode Output Voltage-2	V_{OD2}	2	Vin=1kHz, −20dBV	−33	−31.5	−30	dBV
Decode Output Voltage-3	V_{OD3}	2	Vin=1kHz, −30dBV	−53.5	−51.5	−49.5	dBV
Decode Output Voltage-4	V_{OD4}	2	Vin=1kHz, −40dBV	−74.5	−71.5	−68.5	dBV
Encode Crosstalk	CT_E	4	Vin=1kHz, 0dBV DIN AUDIO Filter			−40	dBV
Decode Crosstalk	CT_D	4	Vin=1kHz, 0dBV DIN AUDIO Filter			−70	dBV
Operating Supply Voltage	V_{OPR}			4.5	5	5.5	V
Input Impedance (Pin⑳)	Z_{inE}		Encode Input f=1kHz		10		kΩ
Input Impedance (Pin⑮)	Z_{inD}		Decode Input f=1kHz		10		kΩ
Output Impedance (Pin⑨)	Z_{OUT}		f=1kHz			100	Ω

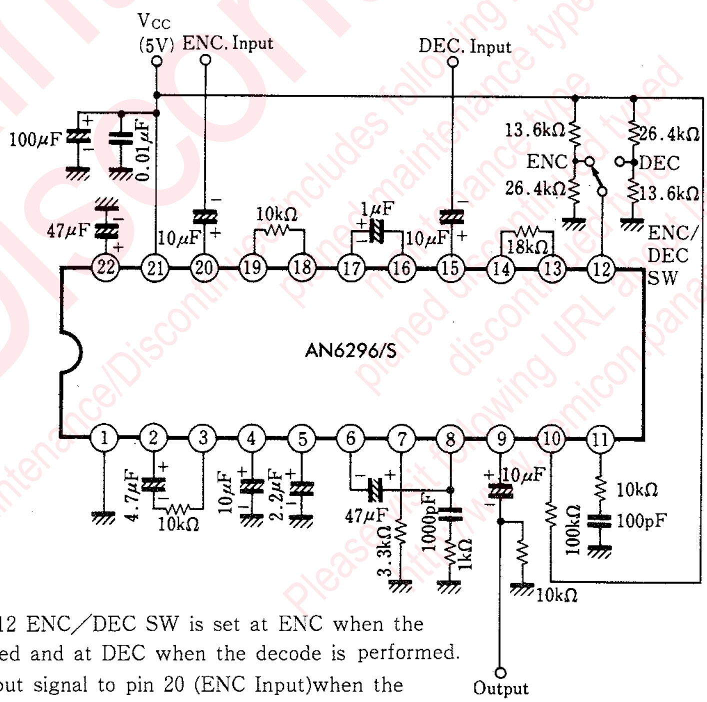
Note) Range of the Operating Supply Voltage : $V_{CC(opr)}$=4.5 to 5.5V

Test Circuit 1 (I_{tot})



*1 Set the pin 12 applied voltage at 3.3V when the encode is performed and as 1.7V when the decode is performed

Test Circuit 2 (V_{SE}, V_{SD}, V_{OME}, V_{OMD}, THD_E, THD_D, V_{OE1}, V_{OE2}, V_{OE3}, V_{OE4}, V_{OD1}, V_{OD2}, V_{OD3}, V_{OD4})



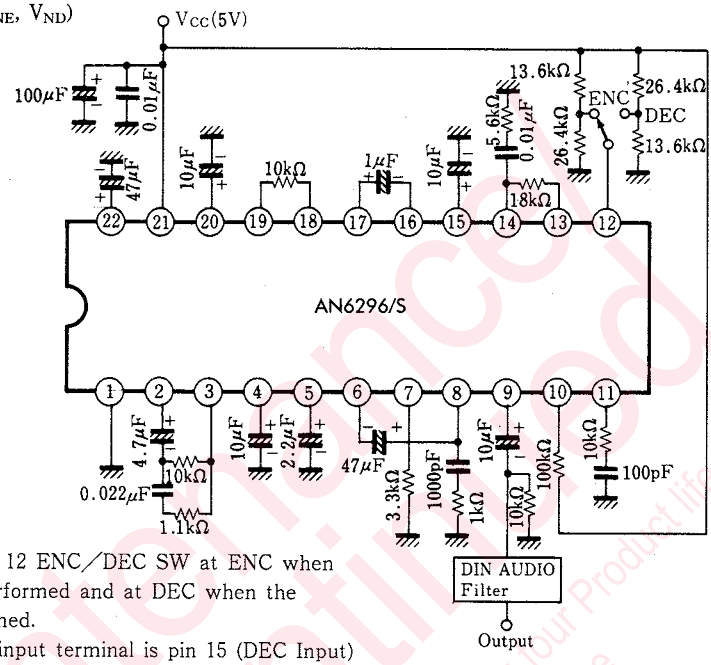
*1 Set the pin 12 ENC/DEC SW is set at ENC when the encode is performed and at DEC when the decode is performed.

*2 Input the input signal to pin 20 (ENC Input)when the encode is performed and to pin 15 (DEC Input) when the decode is performed.

*3 The output is pin 9 (output)

*4 The percentage of errors of the capacitance of 1 μf or less and all the resistances must be within 1 %.

Test Circuit 3 (V_{NE}, V_{ND})



*1 Set the pin 12 ENC/DEC SW at ENC when the encode is performed and at DEC when the decode is performed.

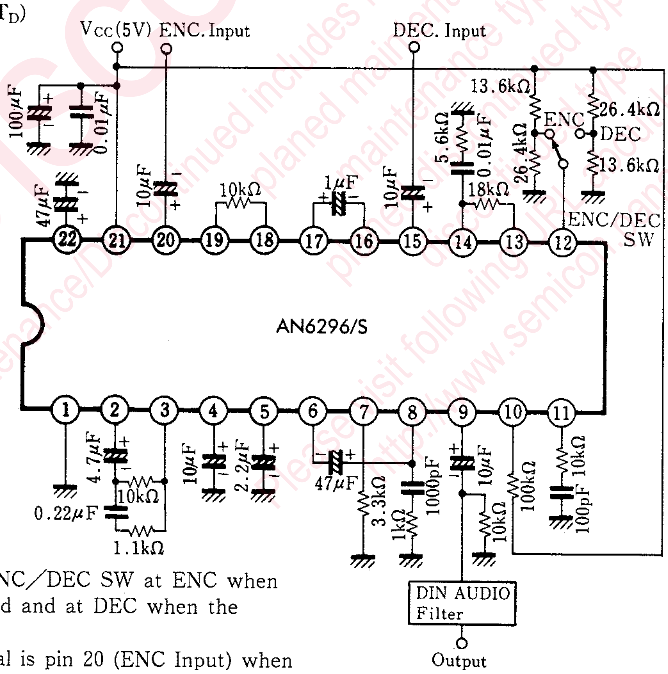
*2 The signal input terminal is pin 15 (DEC Input) when the encode is performed and pin 20 (ENC Input) when the decode is performed.

*3 The output is pin 9 (Output).

*4 The output must pass through the DIN AUDIO filter.

*5 The percentage of errors of the capacitance of 1 μf or less and all the resistances must be within 1 %.

Test Circuit 4 (CT_E, CT_D)



*1 Set the Pin 12 ENC/DEC SW at ENC when the encode is performed and at DEC when the decode is performed.

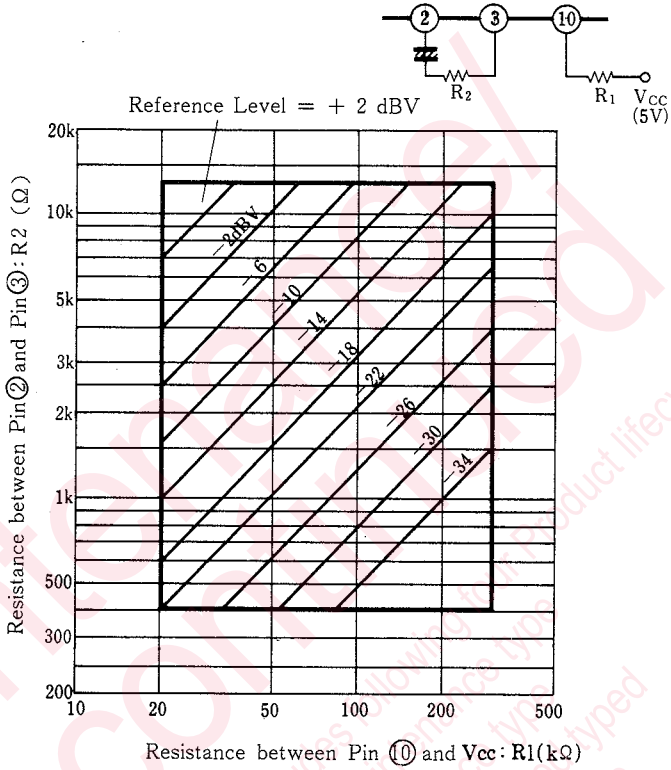
*2 The input terminal is pin 20 (ENC Input) when the encode is performed and Pin 15 (DEC Input) when the decode is performed.

*3 The output is Pin 9 (Output).

*4 The output must pass through the DIN AUDIO filter.

*5 The percentage of errors of the capacitance of 1 μf or less and all the resistances must be within 1 %.

■ Relation between Reference Level and External Resistance



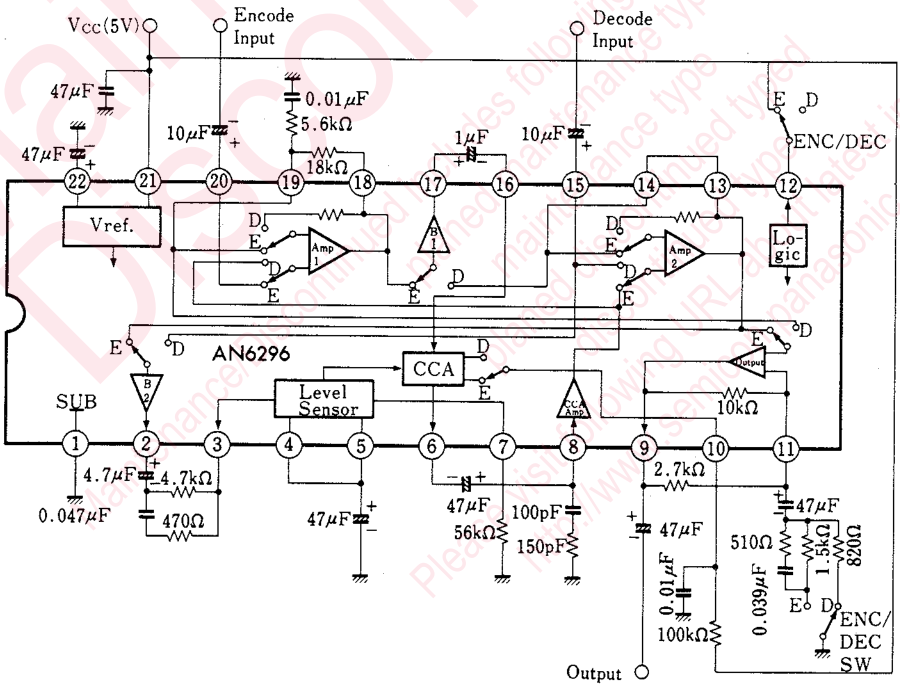
*1 The resistances must be used within the range enclosed with the heavy lines (20 kΩ ⟨R1⟨300kΩ and 400 Ω ⟨R2⟨13kΩ).

*2 The above values are reference ones for designing and not guaranteed ones.

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	GND	12	Encode/Decode SW
2	BF Amp. 2 Output	13	Output Amp. Input/Amp. 2 Output
3	L.S. Input	14	Amp. 2 Feedback/BF Amp. 1 Input
4	Hold Recovery	15	Decode Input
5	Recovery	16	CCA. G.C. Input
6	CCA. G.C. Output	17	BF Amp. 1 Output
7	Recovery Time Adjust	18	BF Amp. 1 Input/Amp. 1 Output
8	CCA Amp. Input	19	Amp. 1 Feedback/Output Amp. Input
9	Signal Output	20	Encode Input
10	Reference Level Adjust	21	V_{cc}
11	Output-Amp. Feedback	22	Reference Voltage

■ Application Circuits



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