

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

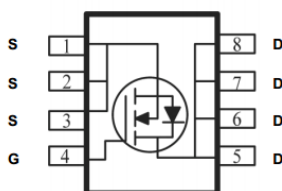
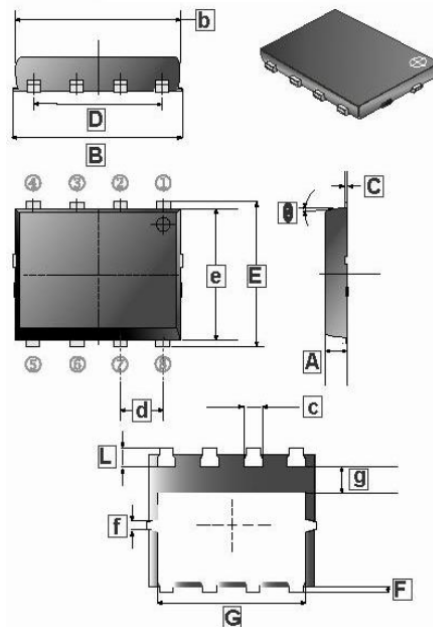
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8PP saves board space.
- Fast switching speed.
- High performance trench technology.

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8PP	3K	13 inch

SOP-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	0.85	1.00	θ	0°	10°
B	5.3 BCS.		b	5.2 BCS.	
C	0.15	0.25	c	0.30	0.50
D	3.8 BCS.		d	1.27 BCS.	
E	6.05 BCS.		e	5.55 BCS.	
F	0.03	0.30	f	0.10	0.40
G	4.35 BCS.		g	1.2 BCS.	
L	0.40	0.70			

ABSOLUTE MAXIMUM RATINGS AND THERMAL DATA ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current ¹	I_D	$T_A=25^\circ\text{C}$	24
		$T_A=70^\circ\text{C}$	19
Pulsed Drain Current ²	I_{DM}	50	A
Continuous Source Current (Diode Conduction) ¹	I_S	2.3	A
Power Dissipation ¹	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2.2
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Data			
Maximum Junction to Ambient ¹	$t \leq 10$ sec	$R_{\theta JA}$	25
	Steady-State		65

Notes

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	100	nA	$V_{DS} = 0\text{V}$, $V_{GS} = 20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$
		-	-	5		$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$, $T_J=55^\circ\text{C}$
On-State Drain Current ^A	$I_{D(ON)}$	40	-	-	A	$V_{DS} = 5\text{V}$, $V_{GS} = 10\text{V}$
Drain-Source On-Resistance ^A	$R_{DS(ON)}$	-	-	4.6	m Ω	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$
		-	-	5.5		$V_{GS} = 4.5\text{V}$, $I_D = 8\text{A}$
Forward Transconductance ^A	g_{FS}	-	40	-	S	$V_{DS} = 15\text{V}$, $I_D = 10\text{A}$
Diode Forward Voltage	V_{SD}	-	0.7	-	V	$I_S = 2.3\text{A}$, $V_{GS} = 0\text{V}$
Dynamic ²						
Total Gate Charge	Q_g	-	15	-	nC	$I_D = 10\text{A}$ $V_{DS} = 15\text{V}$ $V_{GS} = 4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	3	-		
Gate-Drain Charge	Q_{gd}	-	5	-		
Turn-On Delay Time	$T_{d(ON)}$	-	15	-	nS	$I_D = 1\text{A}$, $V_{DD} = 15\text{V}$ $V_{GEN} = 10\text{V}$ $R_L = 6\Omega$
Rise Time	T_r	-	10	-		
Turn-Off Delay Time	$T_{d(OFF)}$	-	54	-		
Fall Time	T_f	-	26	-		

Notes

1. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.