

## P-channel 20 V, 0.0195 $\Omega$ typ., 7 A STripFET™ H7 Power MOSFET in a SOT23-6L package

Datasheet - production data

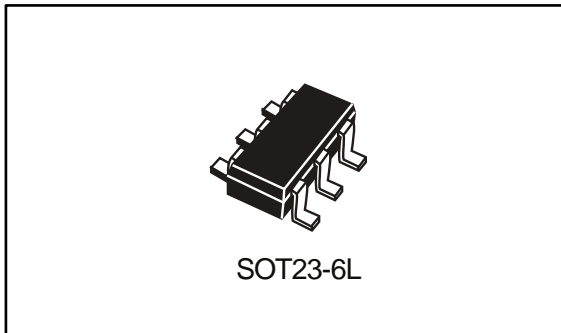
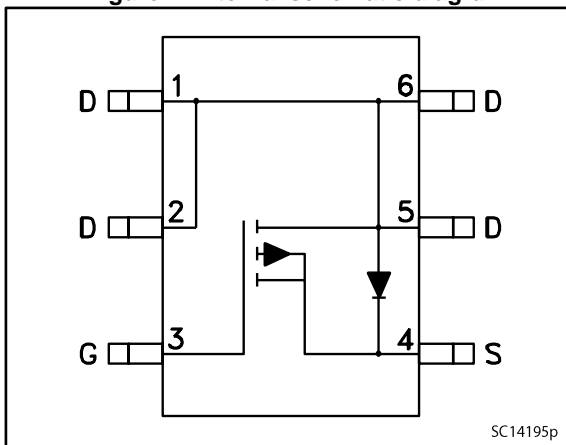


Figure 1: Internal schematic diagram



- Very low on-resistance
- Very low capacitance and gate charge
- High avalanche ruggedness

### Applications


- Switching applications

### Description

This P-channel Power MOSFET utilizes the STripFET H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Table 1: Device summary

Order code	Marking	Package	Packaging
STT7P2UH7	7L2U	SOT23-6L	Tape and reel

 For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STT7P2UH7	20 V	0.0225 $\Omega$ @ 4.5 V	7 A

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package mechanical data .....</b>	<b>9</b>
	4.1 SOT23-6L package mechanical data .....	10
<b>5</b>	<b>Revision history .....</b>	<b>12</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	20	V
$V_{GS}$	Gate-source voltage	$\pm 8$	V
$I_D$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	7	A
$I_D$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	4.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	1.6	W
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	78	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	20			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 20\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 5\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 3.5\text{ A}$		0.0195	0.0225	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 3.5\text{ A}$		0.02	0.025	$\Omega$
		$V_{GS} = 1.8\text{ V}, I_D = 3.5\text{ A}$		0.036	0.043	$\Omega$
		$V_{GS} = 1.5\text{ V}, I_D = 3.5\text{ A}$		0.05	0.085	$\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 16\text{ V}, f = 1\text{ MHz}$	-	2390	-	pF
$C_{oss}$	Output capacitance		-	220	-	pF
$C_{rss}$	Reverse transfer capacitance		-	188	-	pF
$Q_g$	Total gate charge	$V_{DD} = 16\text{ V}, I_D = 7\text{ A}, V_{GS} = 4.5\text{ V}$	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	4.2	-	nC
$Q_{gd}$	Gate-drain charge		-	3.6	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 16\text{ V}, I_D = 7\text{ A}, R_G = 1\text{ }\Omega, V_{GS} = 4.5\text{ V}$	-	12.5	-	ns
$t_r$	Rise time		-	30.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	128	-	ns
$t_f$	Fall time		-	84.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1 \text{ A}, V_{GS} = 0$	-		1	V
$t_{rr}$	Reverse recovery time	$V_{DD} = 16 \text{ V}$ $di/dt = 100 \text{ A/ms}, I_{SD} = 1 \text{ A}$	-	15.8		ns
$Q_{rr}$	Reverse recovery charge		-	5.9		nC
$I_{RRM}$	Reverse recovery current		-	0.7		A

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup>Pulsed: pulse duration = 300 ms, duty cycle 1.5%



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

## 2.1 Electrical characteristics (curves)

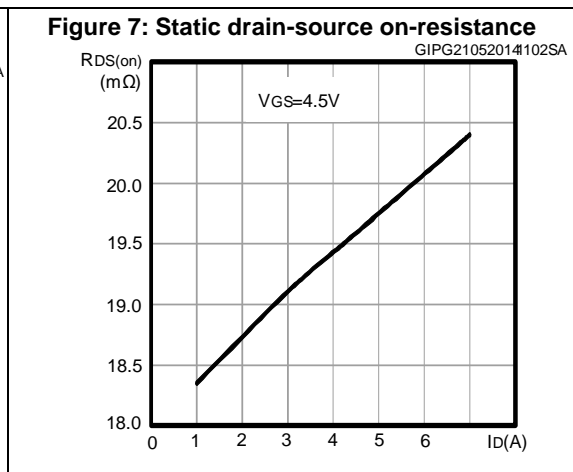
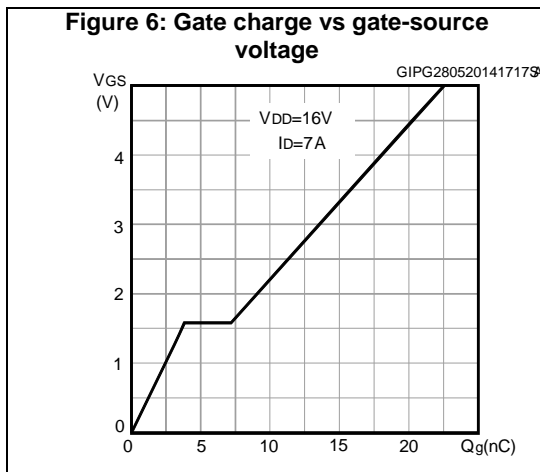
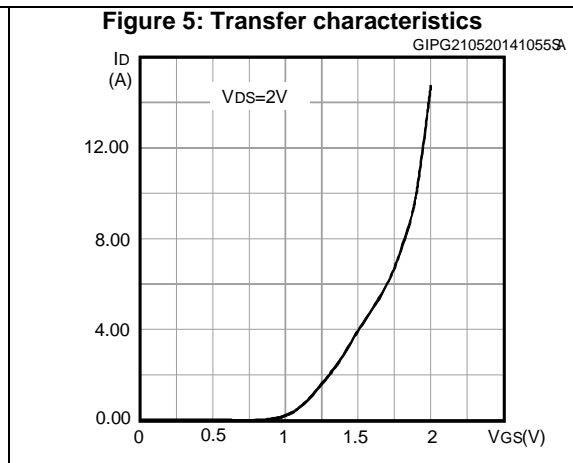
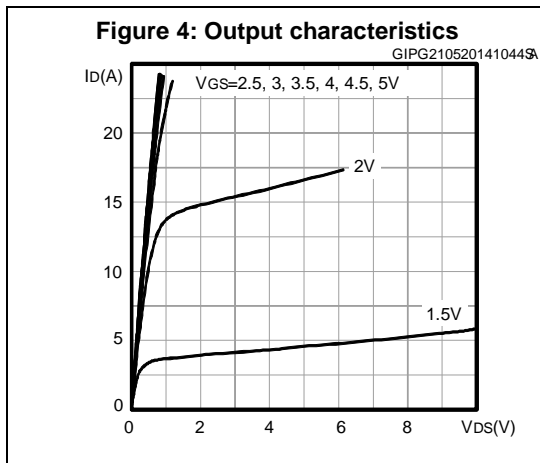
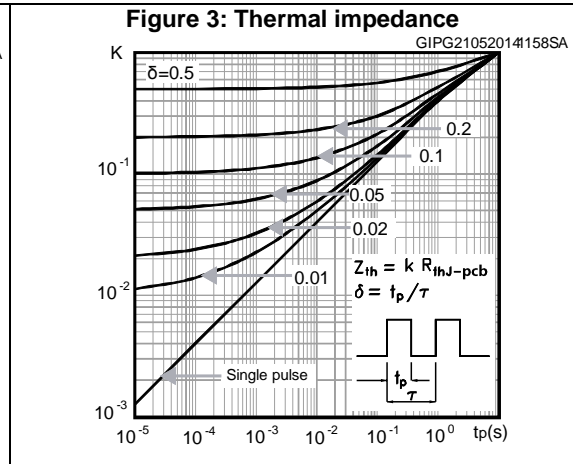
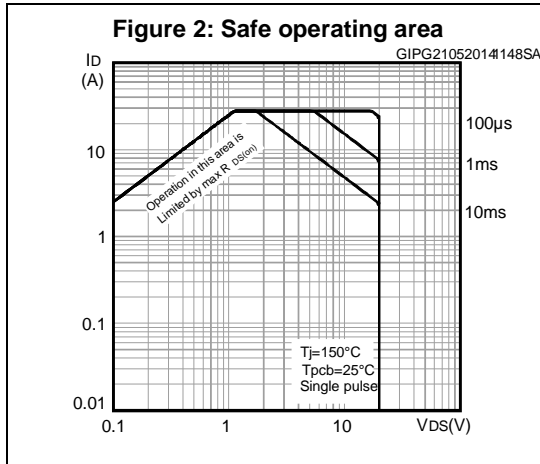


Figure 8: Capacitance variations

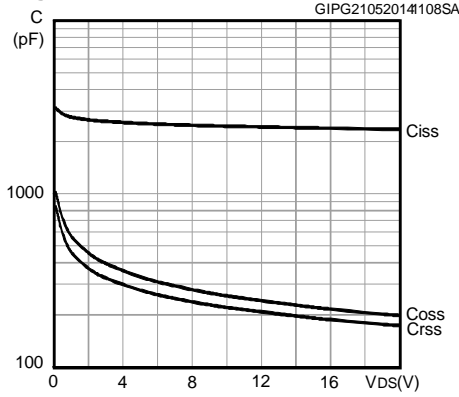


Figure 9: Normalized gate threshold voltage vs temperature

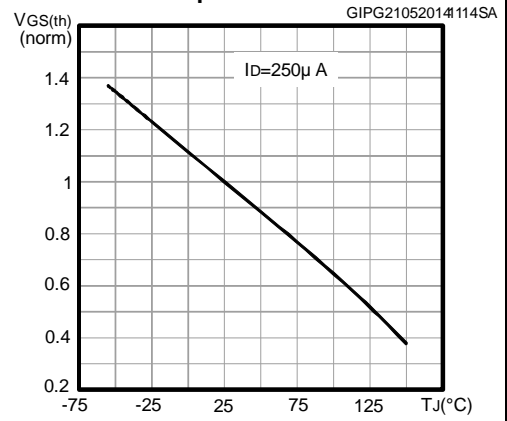


Figure 10: Normalized on-resistance vs temperature

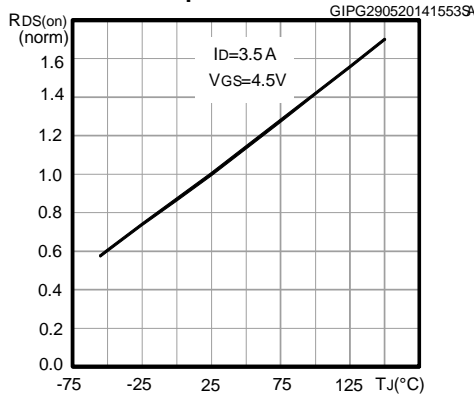


Figure 11: Normalized V(BR)DSS vs temperature

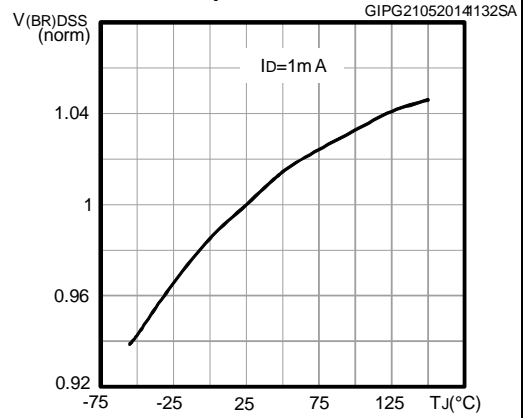
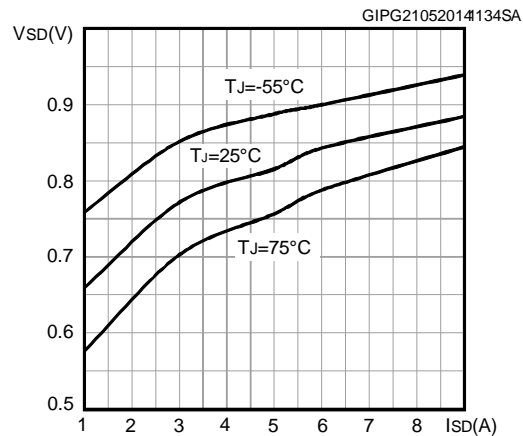
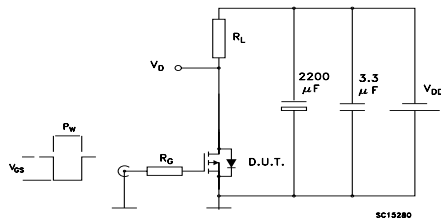


Figure 12: Source-drain diode forward characteristics

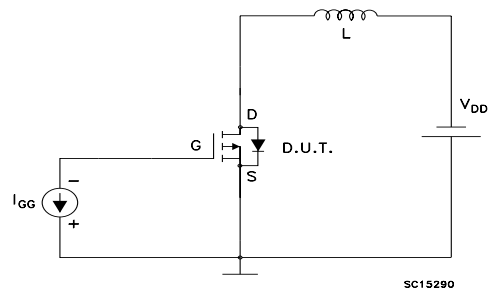


### 3 Test circuits

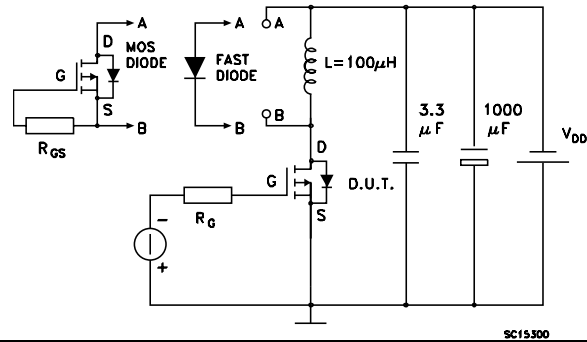
**Figure 13: Switching times test circuit for resistive load**



**Figure 14: Gate charge test circuit**



**Figure 15: Test circuit for inductive load switching and diode recovery times**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 SOT23-6L package mechanical data

Figure 16: SOT23-6L package drawing

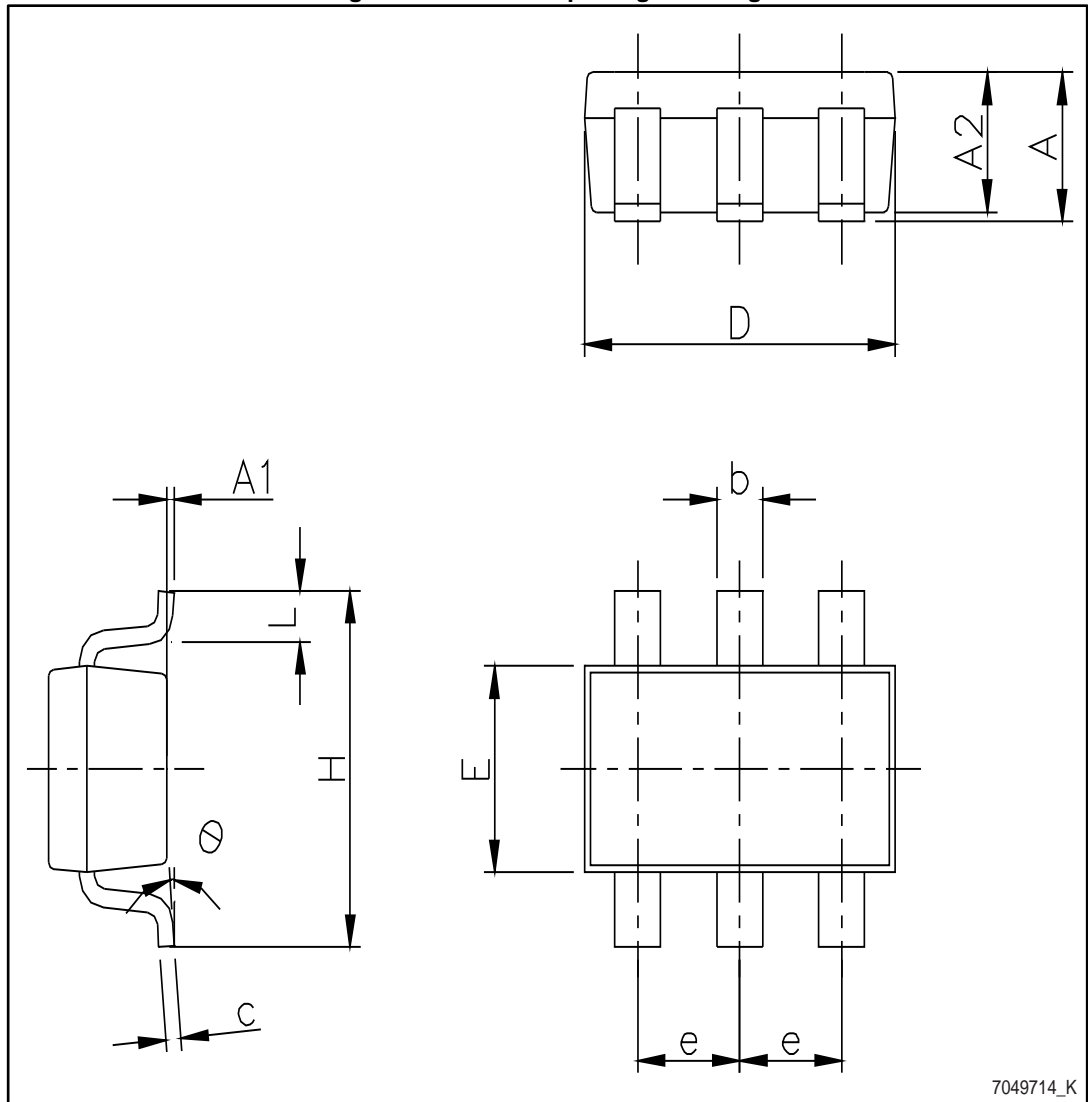
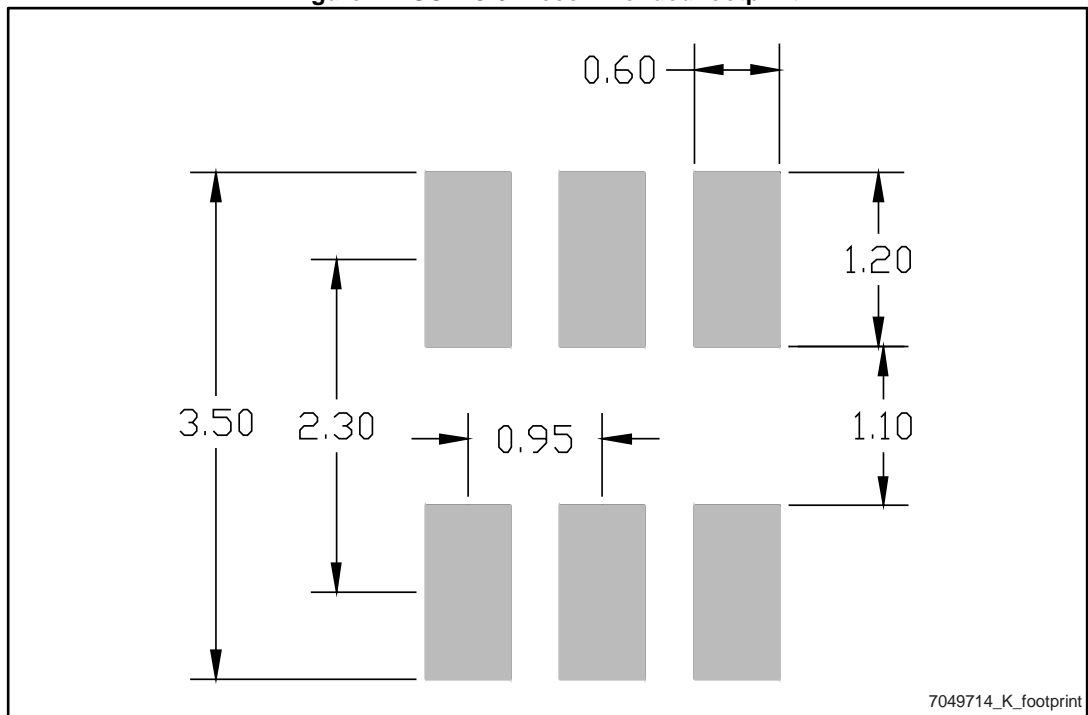


Table 8: SOT23-6L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.00		0.15
A2	1.00	1.10	1.20
b	0.36		0.50
C	0.14		0.20
D	2.826	2.926	3.026
E	1.526	1.626	1.726
e	0.90	0.95	1.00
H	2.60	2.80	3.00
L	0.35	0.45	0.60
$\theta$	0 °C		8 °C

Figure 17: SOT23-6L recommended footprint



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
26-Aug-2013	1	First release.
04-Jun-2014	2	Document status promoted from target data to production data Modified: title Modified: $R_{DS(on)}$ max value in cover page Modified: $R_{DS(on)}$ (typical and maximum) values in <a href="#">Table 4: "On /off states"</a> Modified: the entire typical values in <a href="#">Table 5: "Dynamic"</a> , <a href="#">Table 6: "Switching times"</a> and <a href="#">Table 7: "Source drain diode"</a> Added: <a href="#">Section 2.1: "Electrical characteristics (curves)"</a> Updated: <a href="#">Section 4.1: "SOT23-6L package mechanical data"</a> Minor text changes
02-Oct-2014	3	Updated title, features and description in cover page. Updated <a href="#">Table 4: "On /off states"</a> . Minor text changes.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved