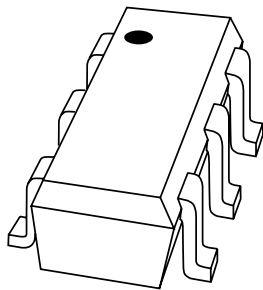


DATA SHEET



PUMD15

**NPN/PNP resistor-equipped
transistors;**

$R1 = 4.7 \text{ k}\Omega$, $R2 = 4.7 \text{ k}\Omega$

Product specification

2004 Feb 04

**NPN/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 4.7 kΩ**

PUMD15

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | TYP. | MAX. | UNIT |
|------------------|---------------------------|------|------|------|
| V _{CEO} | collector-emitter voltage | – | 50 | V |
| I _O | output current (DC) | – | 100 | mA |
| TR1 | NPN | – | – | – |
| TR2 | PNP | – | – | – |
| R1 | bias resistor | 4.7 | – | kΩ |
| R2 | bias resistor | 4.7 | – | kΩ |

DESCRIPTION

NPN/PNP resistor-equipped transistors (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

| TYPE NUMBER | PACKAGE | | MARKING CODE | PNP/PNP COMPLEMENT | NPN/PNP COMPLEMENT |
|-------------|---------|-------|--------------|--------------------|--------------------|
| | PHILIPS | EIAJ | | | |
| PUMD15 | SOT363 | SC-88 | D0*(1) | PUMB15 | PUMH15 |

Note

- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

| TYPE NUMBER | SIMPLIFIED OUTLINE AND SYMBOL | PINNING | |
|-------------|-------------------------------|---------|---------------|
| | | PIN | DESCRIPTION |
| PUMD15 | <p>Top view</p> <p>MAM468</p> | 1 | emitter TR1 |
| | | 2 | base TR1 |
| | | 3 | collector TR2 |
| | | 4 | emitter TR2 |
| | | 5 | base TR2 |
| | | 6 | collector TR1 |

NPN/PNP resistor-equipped transistors;
R1 = 4.7 k Ω , R2 = 4.7 k Ω

PUMD15

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|--|---------|
| | NAME | DESCRIPTION | VERSION |
| PUMD15 | – | plastic surface mounted package; 6 leads | SOT363 |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|--|-------------------------------|----------------------------------|------|------|------|
| Per transistor; for the PNP transistor with negative polarity | | | | | |
| V _{CBO} | collector-base voltage | open emitter | – | 50 | V |
| V _{CEO} | collector-emitter voltage | open base | – | 50 | V |
| V _{EBO} | emitter-base voltage | open collector | – | 10 | V |
| V _I | input voltage TR1 | positive | – | +30 | V |
| | | negative | – | –10 | V |
| V _I | input voltage TR2 | positive | – | +10 | V |
| | | negative | – | –30 | V |
| I _O | output current (DC) | | – | 100 | mA |
| I _{CM} | peak collector current | | – | 100 | mA |
| P _{tot} | total power dissipation | T _{amb} ≤ 25 °C; note 1 | – | 200 | mW |
| T _{stg} | storage temperature | | –65 | +150 | °C |
| T _j | junction temperature | | – | 150 | °C |
| T _{amb} | operating ambient temperature | | –65 | +150 | °C |
| Per device | | | | | |
| P _{tot} | total power dissipation | T _{amb} ≤ 25 °C; note 1 | – | 300 | mW |

Note

- Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|-----------------------|---|----------------------------------|-------|------|
| Per transistor | | | | |
| R _{th j-a} | thermal resistance from junction to ambient | T _{amb} ≤ 25 °C; note 1 | 625 | K/W |
| Per device | | | | |
| R _{th j-a} | thermal resistance from junction to ambient | T _{amb} ≤ 25 °C; note 1 | 416 | K/W |

Note

- Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

NPN/PNP resistor-equipped transistors;
 $R1 = 4.7 \text{ k}\Omega$, $R2 = 4.7 \text{ k}\Omega$

PUMD15

CHARACTERISTICS $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--------------------------------------|---|------|------|------|------------------|
| Per transistor; for the PNP transistor with negative polarity | | | | | | |
| I_{CBO} | collector-base cut-off current | $V_{\text{CB}} = 50 \text{ V}$; $I_{\text{E}} = 0$ | – | – | 100 | nA |
| I_{CEO} | collector-emitter cut-off current | $V_{\text{CE}} = 30 \text{ V}$; $I_{\text{B}} = 0$ | – | – | 1 | μA |
| | | $V_{\text{CE}} = 30 \text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$ | – | – | 50 | μA |
| I_{EBO} | emitter-base cut-off current | $V_{\text{EB}} = 5 \text{ V}$; $I_{\text{C}} = 0$ | – | – | 0.9 | mA |
| h_{FE} | DC current gain | $V_{\text{CE}} = 5 \text{ V}$; $I_{\text{C}} = 10 \text{ mA}$ | 30 | – | – | |
| V_{CEsat} | collector-emitter saturation voltage | $I_{\text{C}} = 10 \text{ mA}$; $I_{\text{B}} = 0.5 \text{ mA}$ | – | – | 150 | mV |
| $V_{\text{i(off)}}$ | input-off voltage | $I_{\text{C}} = 100 \text{ }\mu\text{A}$; $V_{\text{CE}} = 5 \text{ V}$ | – | 1.1 | 0.5 | V |
| $V_{\text{i(on)}}$ | input-on voltage | $I_{\text{C}} = 20 \text{ mA}$; $V_{\text{CE}} = 0.3 \text{ V}$ | 2.5 | 1.9 | – | V |
| R1 | input resistor | | 3.3 | 4.7 | 6.1 | $\text{k}\Omega$ |
| $\frac{R2}{R1}$ | resistor ratio | | 0.8 | 1 | 1.2 | |
| C_{c} | collector capacitance | $I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = 10 \text{ V}$; $f = 1 \text{ MHz}$ | – | – | 2.5 | pF |
| | TR1 (NPN) | | | | | |
| | TR2 (PNP) | | – | – | 3 | pF |

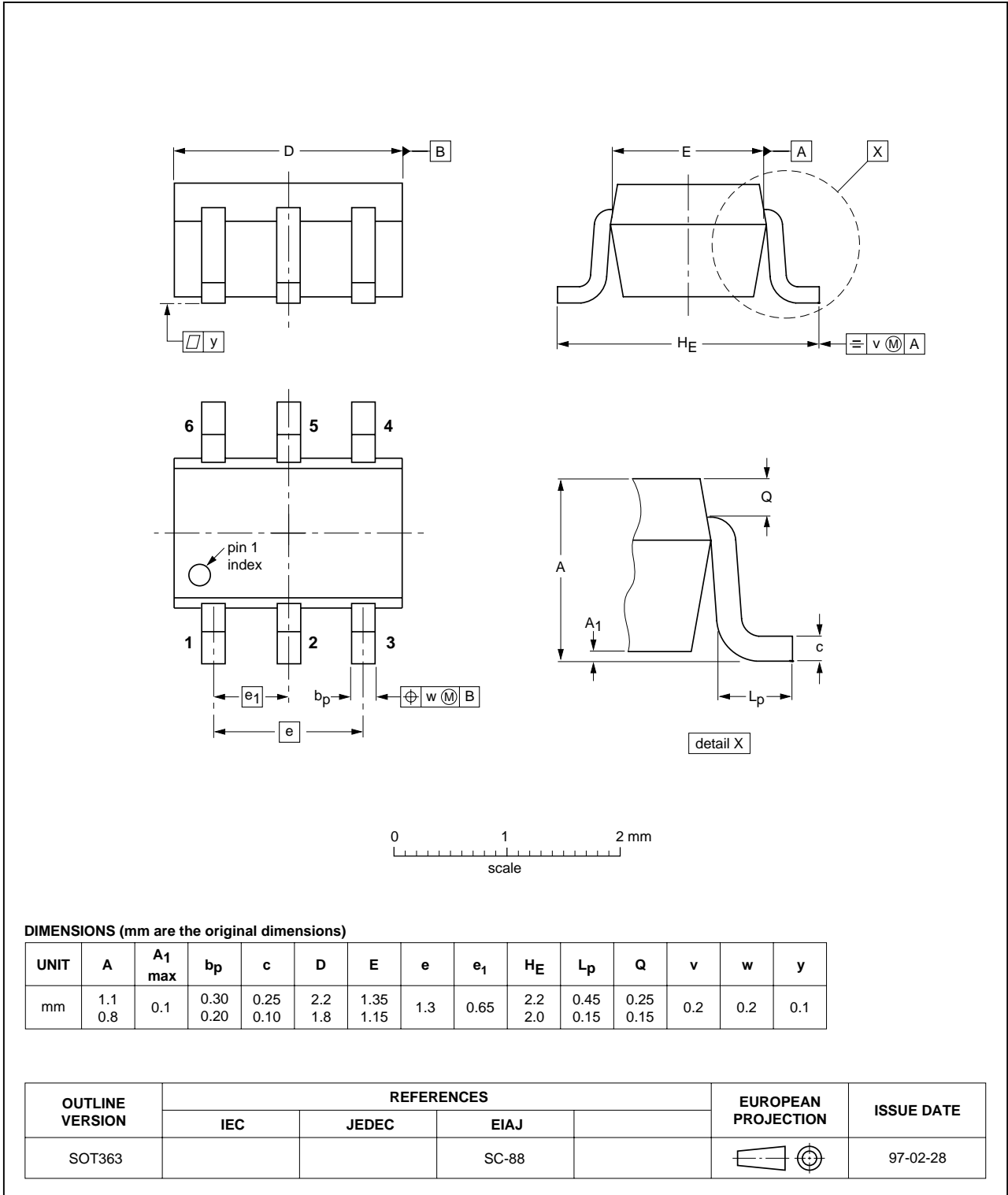
NPN/PNP resistor-equipped transistors;
 R1 = 4.7 kΩ, R2 = 4.7 kΩ

PUMD15

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT363



NPN/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 4.7 kΩ

PUMD15

DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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