

# PM50CSD060

FLAT-BASE TYPE  
INSULATED PACKAGE

## PM50CSD060



### FEATURE

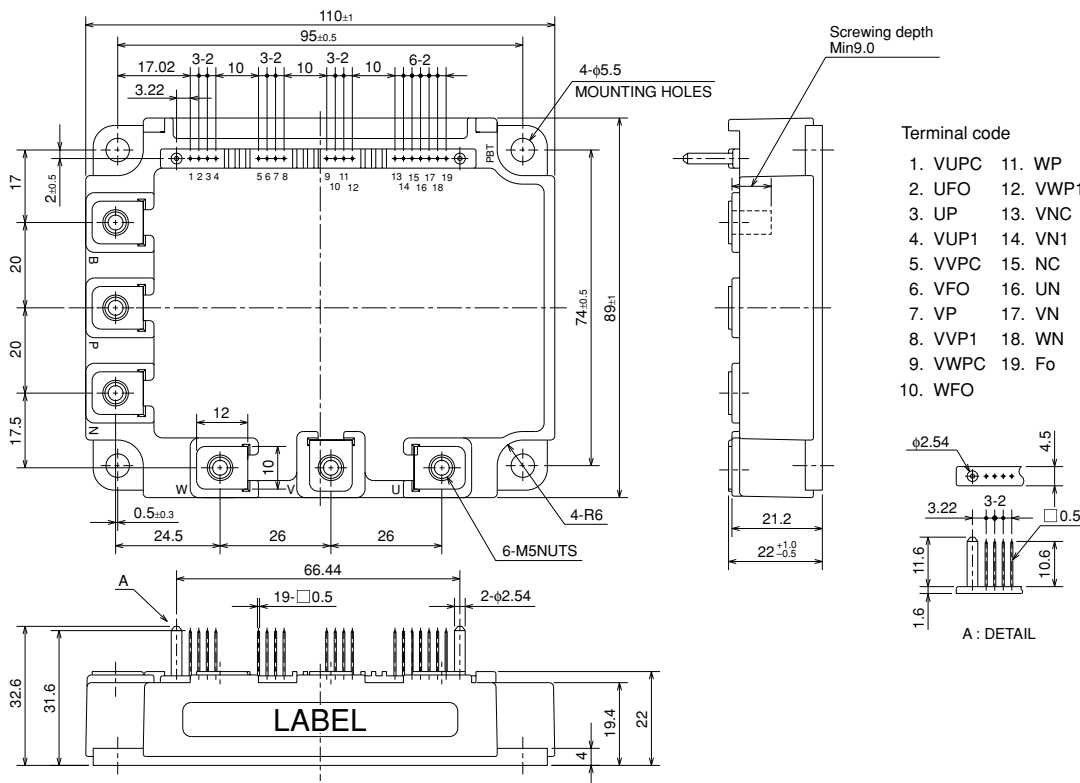
- a) Adopting new 4th generation planar IGBT chip, which performance is improved by 1 $\mu$ m fine rule process.  
For example, typical  $V_{CE(sat)}$ =1.7V
- b) Using new Diode which is designed to get soft reverse recovery characteristics.
- c) Keeping the package compatibility.  
The layout/position of both terminal pin and mounting hole is same as S-series 3rd generation IPM.
  - 3 $\phi$  50A, 600V Current-sense IGBT for 15kHz switching
  - Monolithic gate drive & protection logic
  - Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage (P-Fo available from upper leg devices)
  - Acoustic noise-less 3.7kW class inverter application

## APPLICATION

General purpose inverter, servo drives and other motor controls

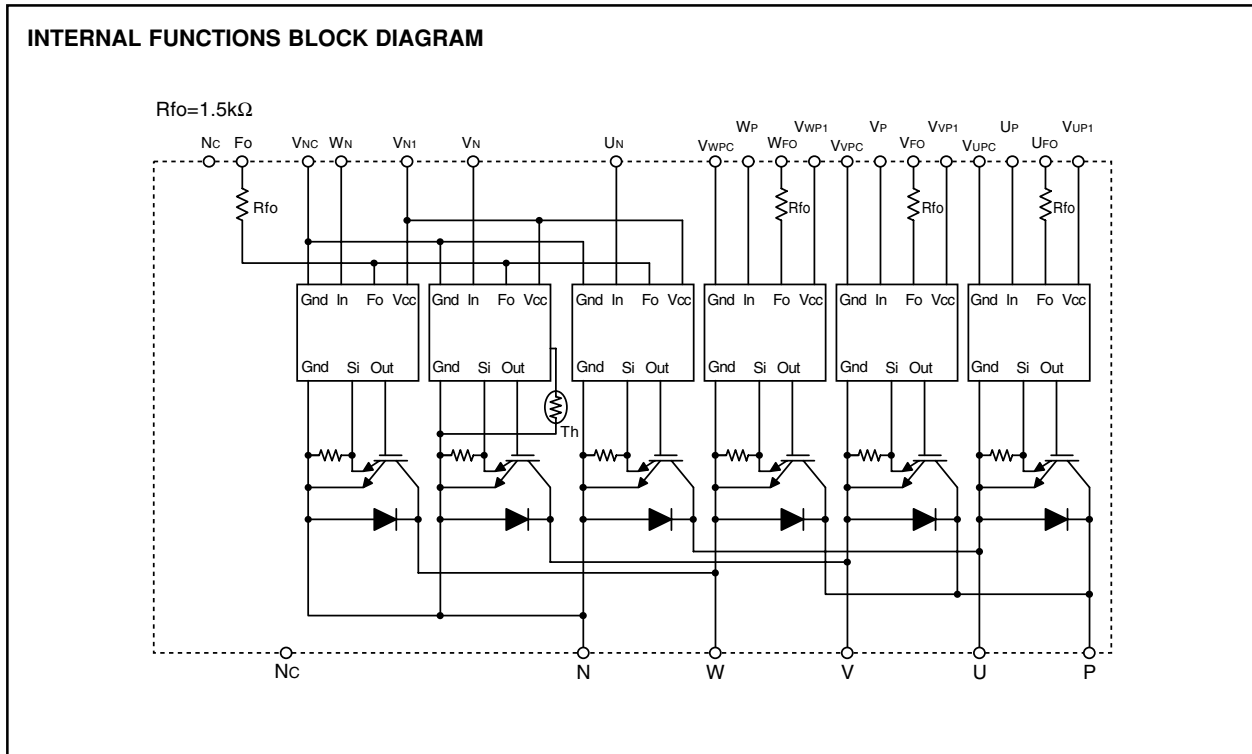
## PACKAGE OUTLINES

Dimensions in mm



# PM50CSD060

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INSULATED PACKAGE



**MAXIMUM RATINGS** (Tj = 25°C, unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V <sub>CES</sub>	Collector-Emitter Voltage	V <sub>D</sub> = 15V, V <sub>CIN</sub> = 15V	600	V
±I <sub>C</sub>	Collector Current	T <sub>C</sub> = 25°C	50	A
±I <sub>CP</sub>	Collector Current (Peak)	T <sub>C</sub> = 25°C	100	A
P <sub>C</sub>	Collector Dissipation	T <sub>C</sub> = 25°C	125	W
T <sub>j</sub>	Junction Temperature		-20 ~ +150	°C

**CONTROL PART**

Symbol	Parameter	Condition	Ratings	Unit
V <sub>D</sub>	Supply Voltage	Applied between : V <sub>UP1</sub> -V <sub>UPC</sub> V <sub>V<sub>P1</sub></sub> -V <sub>V<sub>PC</sub></sub> , V <sub>W<sub>P1</sub></sub> -V <sub>W<sub>PC</sub></sub> , V <sub>N1</sub> -V <sub>N<sub>C</sub></sub>	20	V
V <sub>CIN</sub>	Input Voltage	Applied between : U <sub>P</sub> -V <sub>UPC</sub> , V <sub>P</sub> -V <sub>VPC</sub> W <sub>P</sub> -V <sub>WPC</sub> , U <sub>N</sub> • V <sub>N</sub> • W <sub>N</sub> -V <sub>N<sub>C</sub></sub>	20	V
V <sub>FO</sub>	Fault Output Supply Voltage	Applied between : U <sub>FO</sub> -V <sub>UPC</sub> , V <sub>FO</sub> -V <sub>VPC</sub> , W <sub>FO</sub> -V <sub>WPC</sub> F <sub>O</sub> -V <sub>N<sub>C</sub></sub>	20	V
I <sub>FO</sub>	Fault Output Current	Sink current at U <sub>FO</sub> , V <sub>FO</sub> , W <sub>FO</sub> , F <sub>O</sub> terminals	20	mA

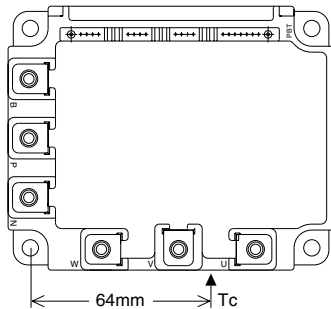
# PM50CSD060

FLAT-BASE TYPE  
INSULATED PACKAGE

## TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Supply Voltage Protected by OC & SC	V <sub>D</sub> = 13.5 ~ 16.5V, Inverter Part, T <sub>j</sub> = 125°C Start	400	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value or without switching	500	V
T <sub>c</sub>	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T <sub>stg</sub>	Storage Temperature		-40 ~ +125	°C
V <sub>iso</sub>	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V <sub>rms</sub>

(Note-1) T<sub>c</sub> measurement point is as shown below. (Base plate depth 3mm)



## THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
R <sub>th(j-c)Q</sub>	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element), (Note-1)	—	—	1.00	°C/W
R <sub>th(j-c)F</sub>		Inverter FWDi part (per 1 element), (Note-1)	—	—	2.50	
R <sub>th(j-c)Q</sub>		Inverter IGBT part (per 1 element), (Note-2)	—	—	0.82	
R <sub>th(j-c)F</sub>		Inverter FWDi part (per 1 element), (Note-2)	—	—	1.51	
R <sub>th(c-f)</sub>	Contact Thermal Resistance	Case to fin, Thermal grease applied (per 1 module)	—	—	0.027	

(Note-2) T<sub>c</sub> measurement point is just under the chips.

If you use this value, R<sub>th(f-a)</sub> should be measured just under the chips.

## ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise noted)

### INVERTER PART

Symbol	Parameter	Test Condition	Limits			Unit	
			Min.	Typ.	Max.		
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage	V <sub>D</sub> = 15V, I <sub>C</sub> = 50A V <sub>CIN</sub> = 0V, Pulsed (Fig. 1)	T <sub>j</sub> = 25°C	—	1.7	2.3	V
			T <sub>j</sub> = 125°C	—	1.7	2.3	
V <sub>EC</sub>	FWDi Forward Voltage	-I <sub>C</sub> = 50A, V <sub>D</sub> = 15V, V <sub>CIN</sub> = 15V (Fig. 2)	—	2.2	3.3	V	
t <sub>on</sub>	Switching Time	V <sub>D</sub> = 15V, V <sub>CIN</sub> = 15V↔0V V <sub>CC</sub> = 300V, I <sub>C</sub> = 50A T <sub>j</sub> = 125°C Inductive Load (upper and lower arm) (Fig. 3)	0.8	1.2	2.4	μs	
t <sub>rr</sub>			—	0.15	0.3		
t <sub>c(on)</sub>			—	0.4	1.0		
t <sub>off</sub>			—	2.4	3.3		
t <sub>c(off)</sub>			—	0.6	1.2		
I <sub>CES</sub>	Collector-Emitter Cutoff Current	V <sub>CE</sub> = V <sub>CEs</sub> , V <sub>CIN</sub> = 15V (Fig. 4)	T <sub>j</sub> = 25°C	—	—	1	mA
			T <sub>j</sub> = 125°C	—	—	10	

# PM50CSD060

FLAT-BASE TYPE  
INSULATED PACKAGE

## CONTROL PART

Symbol	Parameter	Test Condition	Limits			Unit	
			Min.	Typ.	Max.		
ID	Circuit Current	V <sub>D</sub> = 15V, V <sub>CIN</sub> = 15V	V <sub>N1</sub> -V <sub>Nc</sub>	—	40	55	mA
			V <sub>XP1</sub> -V <sub>XPC</sub>	—	13	18	
V <sub>th(ON)</sub>	Input ON Threshold Voltage	Applied between : UP-VU <sub>PC</sub> , VP-VV <sub>PC</sub> , WP-VW <sub>PC</sub> UN • VN • WN-V <sub>Nc</sub>		1.2	1.5	1.8	V
V <sub>th(OFF)</sub>	Input OFF Threshold Voltage			1.7	2.0	2.3	
OC	Over Current Trip Level	V <sub>D</sub> = 15V (Fig. 5,6)	T <sub>j</sub> = -20°C	—	—	220	A
			T <sub>j</sub> = 25°C	109	128	180	
			T <sub>j</sub> = 125°C	65	—	—	
SC	Short Circuit Trip Level	-20 ≤ T <sub>j</sub> ≤ 125°C, V <sub>D</sub> = 15V (Fig. 5,6)	—	132	—	A	
t <sub>off(OC)</sub>	Over Current Delay Time	V <sub>D</sub> = 15V (Fig. 5,6)	—	10	—	μs	
OT	Over Temperature Protection	Base-plate Temperature detection, V <sub>D</sub> = 15V	Trip level	111	118	125	°C
OT <sub>r</sub>			Reset level	—	100	—	
UV	Supply Circuit Under-Voltage Protection	-20 ≤ T <sub>j</sub> ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV <sub>r</sub>			Reset level	—	12.5	—	
I <sub>FO(H)</sub>	Fault Output Current	V <sub>D</sub> = 15V, V <sub>FO</sub> = 15V (Note-3)		—	—	0.01	mA
I <sub>FO(L)</sub>				—	10	15	
t <sub>FO</sub>	Minimum Fault Output Pulse Width	V <sub>D</sub> = 15V (Note-3)	1.0	1.8	—	ms	

(Note-3) Fault output is given only when the internal OC, SC, OT & UV protection.  
 Fault output of OC, SC and UV protection operate by upper and lower arms.  
 Fault output of OT protection operate by lower arm.  
 Fault output of OC, SC protection given pulse.  
 Fault output of OT, UV protection given pulse while over level.

## MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	560	—	g

## RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V <sub>CC</sub>	Supply Voltage	Applied across P-N terminals	≤ 400	V
V <sub>D</sub>	Control Supply Voltage	Applied between : V <sub>UP1</sub> -V <sub>U<sub>PC</sub></sub> , V <sub>VP1</sub> -V <sub>V<sub>PC</sub></sub> V <sub>WP1</sub> -V <sub>W<sub>PC</sub></sub> , V <sub>N1</sub> -V <sub>Nc</sub> (Note-4)	15 ± 1.5	V
V <sub>CIN(ON)</sub>	Input ON Voltage	Applied between : UP-VU <sub>PC</sub> , VP-VV <sub>PC</sub> , WP-VW <sub>PC</sub> UN • VN • WN-V <sub>Nc</sub>	≤ 0.8	V
V <sub>CIN(OFF)</sub>	Input OFF Voltage		≥ 4.0	
f <sub>PWM</sub>	PWM Input Frequency	Using Application Circuit input signal of IPM, 3φ sinusoidal PWM VVVF inverter (Fig. 8)	≤ 20	kHz
t <sub>dead</sub>	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

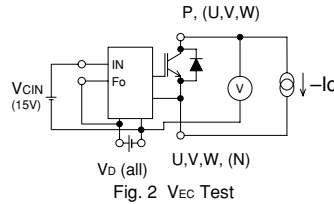
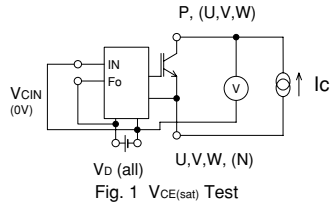
(Note-4) Allowable Ripple rating of Control Voltage : dv/dt ≤ ±5V/μs, 2V<sub>p-p</sub>

# PM50CSD060

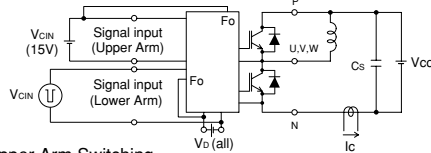
FLAT-BASE TYPE  
INSULATED PACKAGE

## PRECAUTIONS FOR TESTING

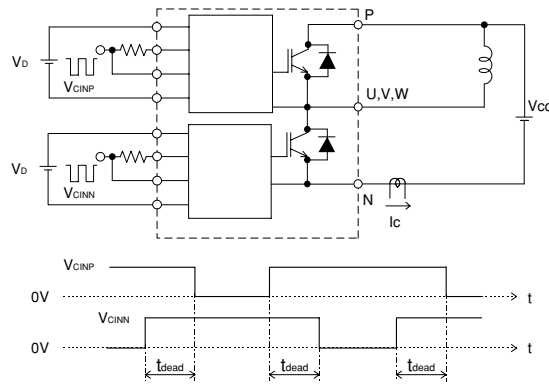
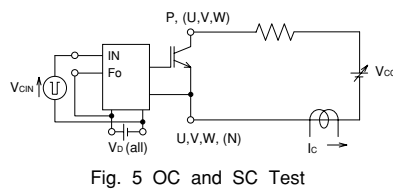
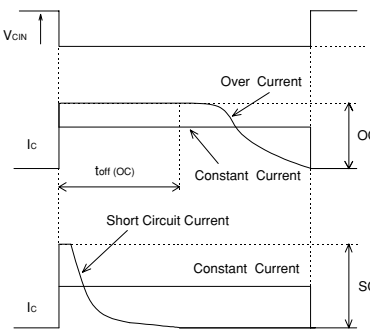
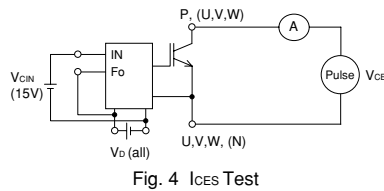
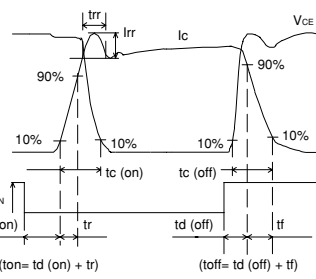
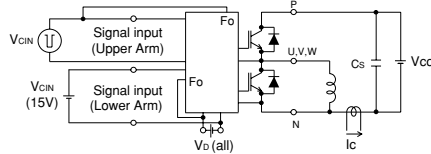
1. Before applying any control supply voltage ( $V_D$ ), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.  
After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above  $V_{CES}$  rating of the device.  
(These test should not be done by using a curve tracer or its equivalent.)



### a) Lower Arm Switching



### b) Upper Arm Switching



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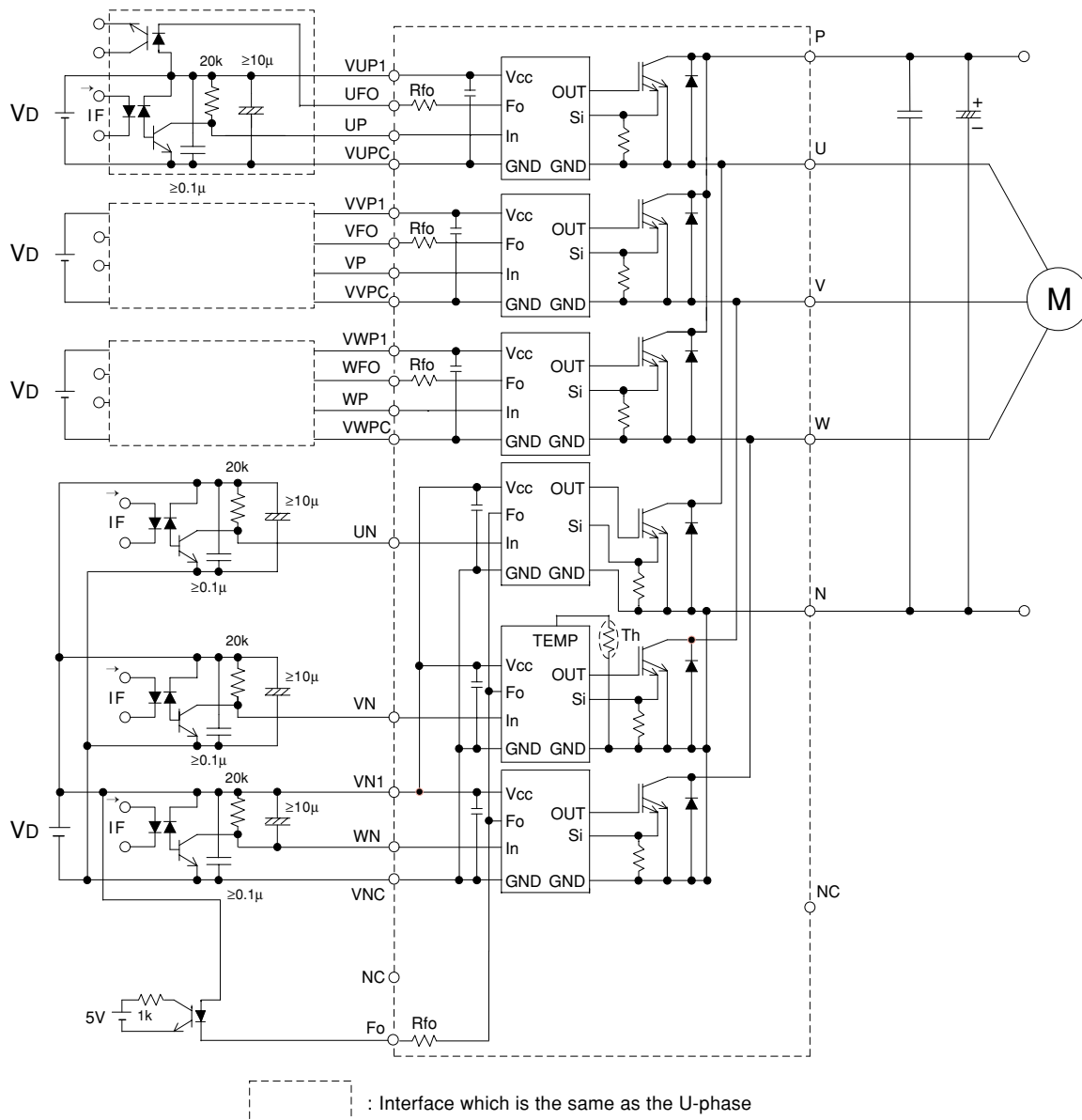


Fig. 8 Application Example Circuit

### NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Quick opto-couplers:  $T_{PLH}, T_{PHL} \leq 0.8\mu s$ . Use High CMR type. The line between opto-coupler and intelligent module should be shortened as much as possible to minimize the floating capacitance.
- Slow switching opto-coupler: recommend to use at  $CTR = 100 \sim 200\%$ , Input current = 8 ~ 10mA, to work in active.
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.