ML22808/ML22804/ML22802-XXX
ML22P808/ML22P804/ML22P802

LAPIS Semiconductor ADPCM Algorithm-Based Speech Synthesis LSI

GENERAL DESCRIPTION

The ML22808/ML22804/ML22802-xxx are speech synthesis LSI devices that have P2ROM for storing voice data. The voice output component has an ADPCM2 decoder to enable high speech quality, a D/A converter, and a low-pass filter.

It is easy to configure a speech synthesizer by connecting a power amplifier and a CPU externally.

The ML22808/ML22804/ML22802-xxx allow selection of a playback method from among the 8-bit PCM, non-linear 8-bit PCM, 16-bit PCM, and 4-bit ADPCM2 algorithms and enable volume control.

The ML22808/ML22804/ML22802-xxx, supported by the ROM codes, are the products in which written speech data is included.

The ML22P808/ML22P804/ML22P802 are OTP products in which speech data can be easily written by the user using a dedicated writer. These devices are suitable for applications in developing products, manufacturing of a wide variety of products in small quantities, and requiring quick turn around.

- Capacity of the internal memory device and the maximum vocal reproduction time (when 4-bit ADPCM2 algorithm used)

| Product name	ROM capacity	Maximum vocal reproduction time (sec)		
		F_{SAM} = 4.0 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz
ML22808-XXX/ML22P808	8 Mbits	524	262	131
ML22804-XXX/ML22P804	4 Mbits	262	131	65
ML22802-XXX/ML22P802	2 Mbits	131	65	32

- Speech synthesis method: An algorithm can be specified for each phrase from among the following:
  4-bit ADPCM2
  8-bit Nonlinear PCM
  8-bit PCM/16-bit PCM
- Sampling frequency: A fsam value can be specified fro each phrase.
  4.0/8.0/16.0 kHz, 5.3/10.7 kHz, 6.4/12.8 kHz
- Built-in low-pass filter and 12-bit D/A converter
- CPU command interface: 3-wired serial / clock synchronous
- Maximum number of phrases: 256 phrases, from 00h to FFh (per bank)
- Memory bank switching: Enabled between bank 1 and bank 4 using the SEL0 and SEL1 pins
- Memory bank selecting: Selectable between bank 1 and bank 4 by setting the SEL0 and SEL1 pins
  (Other than ML22802/ML22P802)
  Selectable between bank1 and bank 2 (ML22802/ML22P802)
- Volume control: Can be adjusted in 16 levels or set to OFF
- Repeat function: LOOP command
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 3.6 V
- Operating temperature range: -20 to +85°C
- Package: 30-pin plastic SSOP (SSOP30-P-56-0.65-K)
- Product name: ML22P808MB, ML22P804MB, ML22P802MB
  ML22808-xxxMB, ML22804-xxxMB, ML22802-xxxMB
  (xxx indicates a ROM code number)

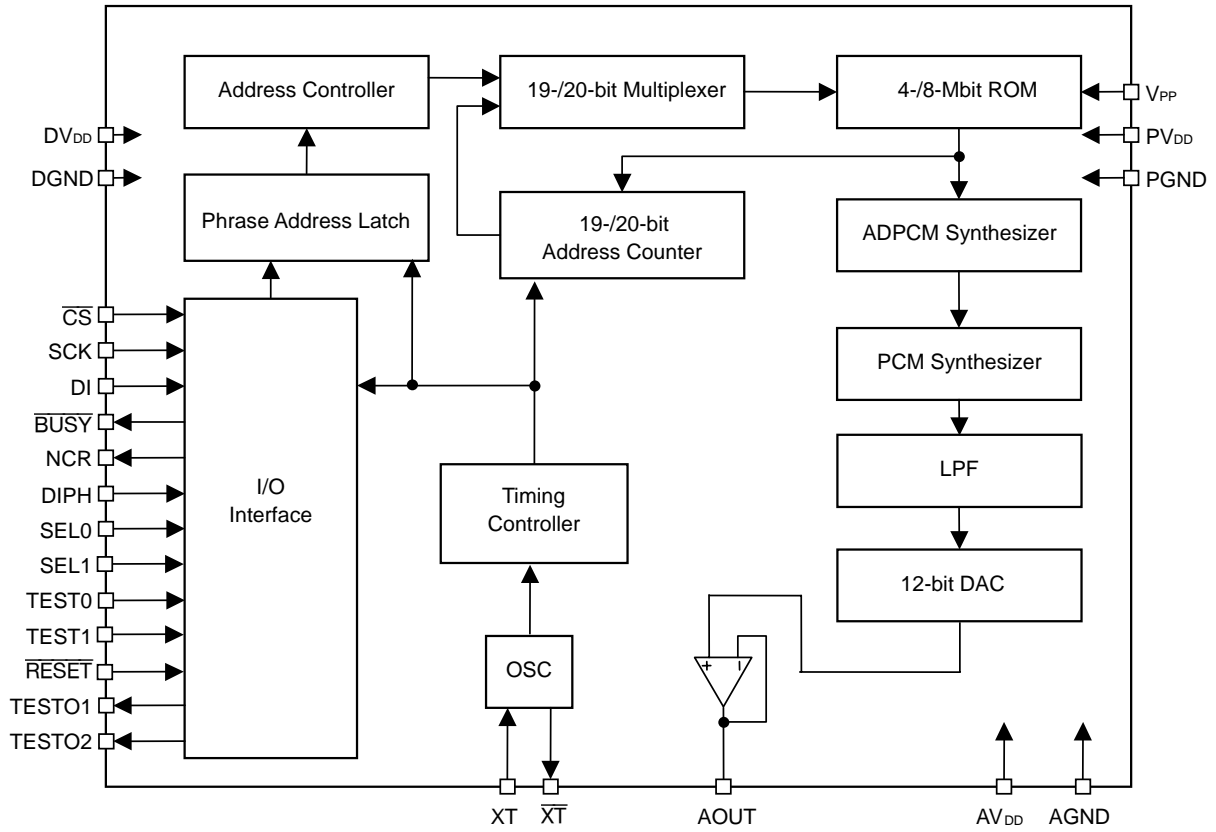The table below summarizes the differences between the ML2216 and the ML2280X.

Item	ML2216	ML2280X
CPU interface	Serial	Serial
Playback method	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM
Maximum number of phrases	256	256 up to 1024 (per bank)
Sampling frequency (kHz)	4.0/5.3/6.4/ 8.0/10.7/12.8 16.0	4.0/5.3/6.4/ 8.0/10.7/12.8 16.0
Clock frequency	4.096 MHz (has a crystal oscillator circuit built-in)	4.096 MHz (has a crystal oscillator circuit built-in)
D/A converter	Current-type 12-bit	Current-type 12-bit
Low-pass filter	3D comb filter	3D comb filter
Speaker driving amplifier	Built-in type; 0.3W (at 8Ω, VDD=5V)	No
Edit ROM	Yes	Yes
Volume control	16 levels	16 levels
Silence insertion	Yes 20 to 1024 ms (4 ms steps)	Yes 20 to 1024 ms (4 ms steps)
Repeat function	Yes	Yes
Interval at which a seam is silent during continuous playback (*1)	No	No
Memory bank switching	No	Yes
Package	44-pin QFP	30-pin SSOP

*1: Continuous playback as shown below is possible.

No silence interval
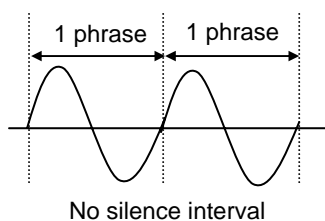
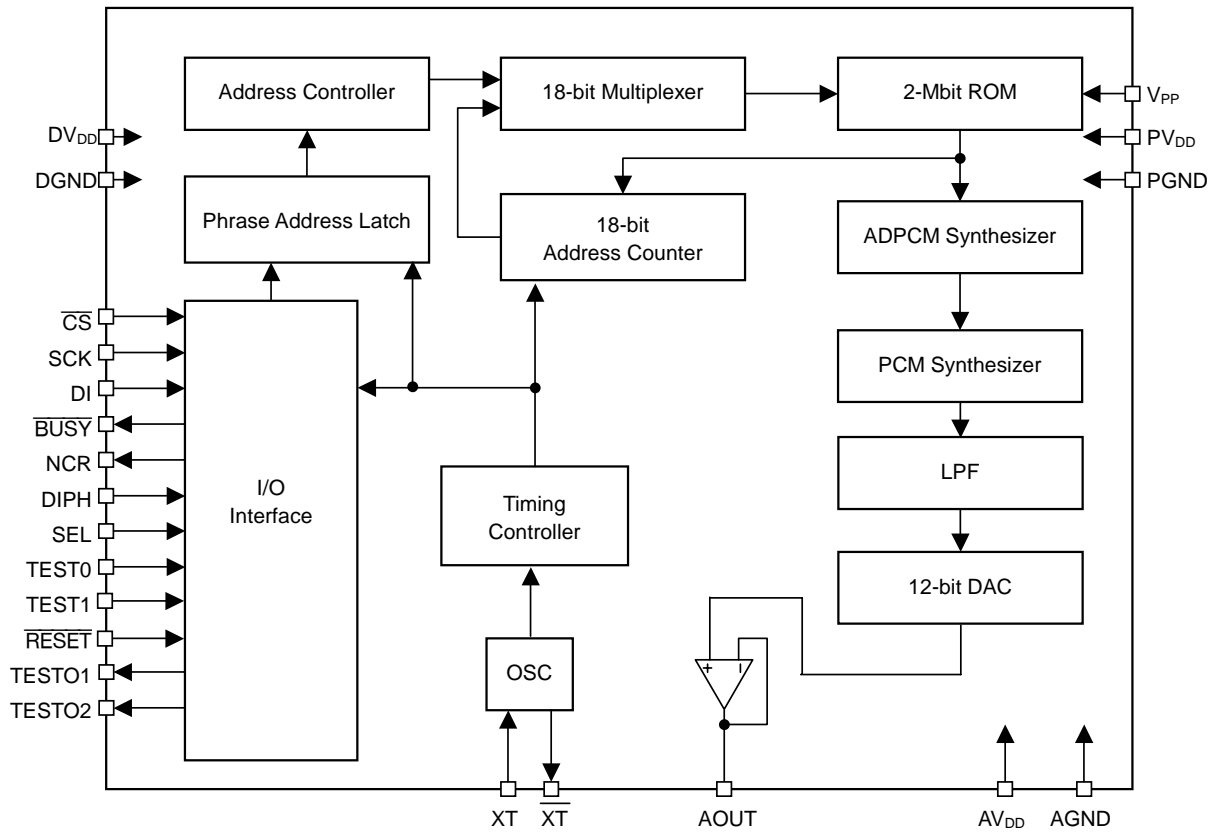## BLOCK DIAGRAM

ML22808/ML22804/ML22P808/ML22P804:

ML22802/ML22P802:

PIN CONFIGURATION (TOP VIEW)

ML22808/ML22804/ML22P808/ML22P804:

XT	1	30	DV_{DD}
$\overline{XT}$	2	29	AV_{DD}
TEST0	3	28	AOUT
TEST1	4	27	NC
DGND	5	26	AGND
DIPH	6	25	V_{PP}
SEL0	7	24	PGND
SEL1	8	23	TESTO1
$\overline{CS}$	9	22	PVDD
SCK	10	21	NC
DI	11	20	NC
$\overline{BUSY}$	12	19	PGND
NCR	13	18	TESTO0
$\overline{RESET}$	14	17	NC
NC	15	16	NC
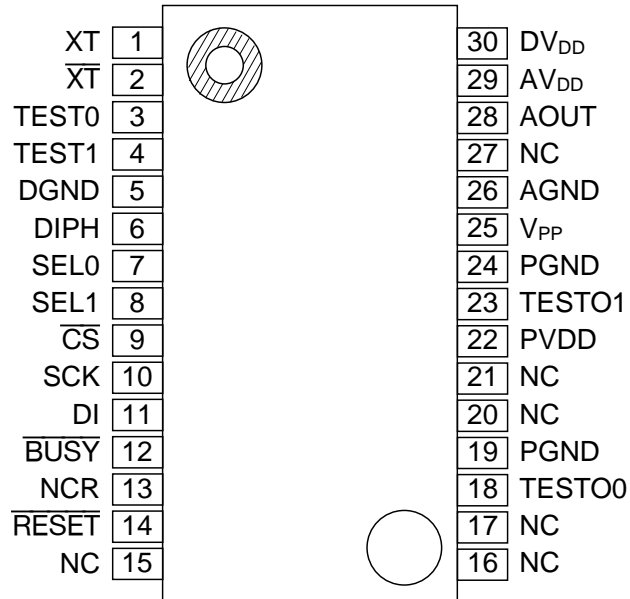
NC: No Connection

30-Pin Plastic SSOP

ML22802/ML22P802:

Pin	Signal		Pin	Signal
1	XT		30	DV_{DD}
2	$\overline{XT}$		29	AV_{DD}
3	TEST0		28	AOUT
4	TEST1		27	NC
5	DGND		26	AGND
6	DIPH		25	V_{PP}
7	SEL		24	PGND
8	TEST2		23	TESTO1
9	$\overline{CS}$		22	PVDD
10	SCK		21	NC
11	DI		20	NC
12	$\overline{BUSY}$		19	PGND
13	NCR		18	TESTO0
14	$\overline{RESET}$		17	NC
15	NC		16	NC
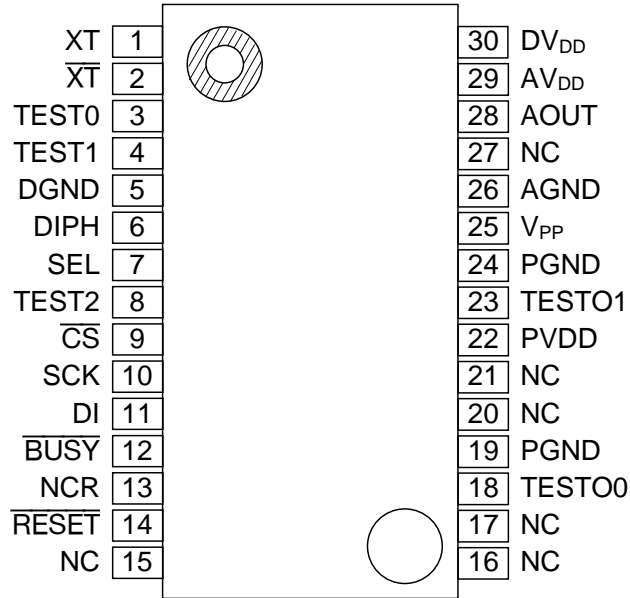
NC: No Connection

30-Pin Plastic SSOP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	XT	I	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{XT}$ pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
2	$\overline{XT}$	O	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible
3	TEST0	I	Input pin for testing. Tie this pin at a "L" level (DGND level).
4	TEST1	I	Input pin for testing. Tie this pin at a "L" level (DGND level).
5	DGND	—	Digital ground pin.
6	DIPH	I	Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the DI pin into the inside of the LSI. When this pin is at a "L" level, DI input data is shifted into the LSI on the rising edges of the SCK clock pulses; when this pin is at a "H" level, DI input data is shifted into the LSI on the falling edges of the SCK clock pulses.
7 (SEL)	SEL0	I	Memory bank selecting pin. Enabled when memory bank selecting is specified at the time the PUP1 or PUP2 command is input. Do not change during speech playback (when the $\overline{BUSY}$ pin is at "L")
8 (TEST2)	SEL1	I	ML22808/ML22804/ML22P808/ML22P804: Memory bank selecting pin. Enabled when memory bank selecting is specified at the time the PUP1 or PUP2 command is input. Do not change during speech playback (when the $\overline{BUSY}$ pin is at "L") ML22802/ML22P802: Input pin for testing. Tie this pin at "L" (DGND level).
9	$\overline{CS}$	I	Chip select input pin. A "L" level on this pin enables the serial interface.
10	SCK	I	Serial clock input pin.
11	DI	I	Serial data input pin.
12	$\overline{BUSY}$	O	Pin that outputs a signal that indicates the phrase playback status. If the LSI is playing a phrase, this pin outputs a "L" level. If the LSI is in a standby state, this pin outputs a "H" level.
13	NCR	O	Pin that outputs a signal that indicates whether command input is enabled or disabled. If command input is enabled, this pin outputs a "H" level. If command input is disabled, this pin outputs a "L" level.
14	$\overline{RESET}$	I	During a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a "L" level to this pin. Put this pin into a "H" level after the power supply voltage is stabilized.
18	TESTO0	O	Output pin for testing. Leave this pin open.
19,24	PGND	—	Ground pin for the internal P2ROM.
22	PV$_{DD}$	—	Power supply pin for the internal P2ROM. Connect a capacitor of 0.1 μF or more between this pin and PGND.
23	TESTO1	O	Output pin for testing. Leave this pin open.

Pin	Symbol	Type	Description
25	V$_{PP}$	I	VPP power supply pin used for writing data to the internal P2ROM. Tie this pin at the DGND level.
26	AGND	—	Analog ground pin.
28	AOUT	O	Playback signal output pin.
29	AV$_{DD}$	—	Analog power supply pin. Connect a capacitor of 0.1 μF or more between this pin and PGND.
30	DV$_{DD}$	—	Digital power supply pin. Connect a capacitor of 0.1 μF or more between this pin and PGND.

Note:
The pin names in the parentheses are applied to ML22802/ML22P802.

ABSOLUTE MAXIMUM RATINGS

(DGND = PGND = AGND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage	DV_{DD}, PV_{DD}	Ta = 25°C	−0.3 to +5.0	V
Analog power supply voltage	AV_{DD}		−0.3 to +5.0	V
Input voltage	V_{IN}	Ta = 25°C When a JEDEC2-layer board is mounted	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		1.3	W
Output short-circuit current	I_{SC}	—	10	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = PGND = AGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Digital power supply voltage	DV_{DD}, PV_{DD}	—	2.7 to 3.6			V
Analog power supply voltage	AV_{DD}	—	2.7 to 3.6			V
Operating temperature	T_{OP}	—	-20 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External crystal oscillator capacitance	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

$DV_{DD} = PV_{DD} = AV_{DD} = 2.7$ to 3.6 V, $DGND = PGND = AGND = 0$ V, $Ta = -20$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.86 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.14 \times V_{DD}$	V
"H" output current 1	V_{OH1}	$I_{OH} = -1$ mA	$V_{DD} - 0.4$	—	—	V
"H" output current 2 (*1)	V_{OH2}	$I_{OH} = -100$ µA	$V_{DD} - 0.4$	—	—	V
"L" output current 1	V_{OL1}	$I_{OL} = 2$ mA	—	—	0.4	V
"L" output current 2 (*1)	V_{OL2}	$I_{OL} = 100$ µA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = DV_{DD}$	—	—	10	µA
"H" input current 2 (*2)	I_{IH2}	$V_{IH} = DV_{DD}$	0.3	2.0	15	µA
"L" input current 1	I_{IL1}	$V_{IL} = DGND$	−10	—	—	µA
"L" input current 2 (*2)	I_{IL2}	$V_{IL} = DGND$	−15	−2.0	−0.3	µA
"H" output leakage current (*3)	I_{LOH}	$V_{IH} = DV_{DD}$	—	—	10	µA
"L" output leakage current (*3)	I_{LOL}	$V_{IL} = DGND$	−10	—	—	µA
Supply current during playback	I_{DD}	$f_{OSC} = 4.096$ MHz No output load	—	—	10	mA
Power-down supply current	I_{DDS}	$Ta = -20$ to $+85°C$	—	1	20	µA

Note: The input voltages and input currents apply to all the input pins except the XT pin.

   The output voltages apply to all the output pins except the AOUT pin.

*1: Applies to the $\overline{XT}$ pin.

*2: Applies to the XT pin.

*3: Applies to the TESTO0 and TESTO1 pins.

Analog Section Characteristics

$DV_{DD} = PV_{DD} = AV_{DD} = 2.7$ to 3.6 V, $DGND = PGND = AGND = 0$ V, $Ta = -20$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	During silence playback	5	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	$0.07 \times AV_{DD}$	—	$0.64 \times AV_{DD}$	V

AC Characteristics

$DV_{DD} = AV_{DD} = 2.7$ to 3.6 V, DGND = PGND = AGND = 0 V, Ta = -20 to +85°C

| Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	t_{RST}	—	1	—	—	μs
SCK setup time for falling edge of $\overline{CS}$	t_{CKS}	—	200	—	—	ns
SCK hold time for falling edge of $\overline{CS}$	t_{CKH}	—	200	—	—	ns
Data setup time for rising edge of SCK	t_{DIS1}	DIPH = "L"	50	—	—	ns
Data hold time for rising edge of SCK	t_{DIH1}	DIPH = "L"	50	—	—	ns
Data setup time for rising edge of SCK	t_{DIS2}	DIPH = "H"	50	—	—	ns
Data hold time for rising edge of SCK	t_{DIH2}	DIPH = "H"	50	—	—	ns
SCK "H" level pulse width	t_{SCKH}	—	200	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	200	—	—	ns
NCR output delay time for rising edge of SCK	t_{DN1}	DIPH = "L"	—	—	150	ns
NCR output delay time for falling edge of SCK	t_{DN2}	DIPH = "H"	—	—	150	ns
$\overline{BUSY}$ output delay time for rising edge of SCK	t_{DB1}	DIPH = "L"	—	—	150	ns
$\overline{BUSY}$ output delay time for falling edge of SCK	t_{DB2}	DIPH = "H"	—	—	150	ns
SEL0 and SEL1 setup time for falling edge of $\overline{BUSY}$ (*4)	t_{SB}	Memory bank function used	1	—	—	μs
SEL0 and SEL1 hold time for falling edge of $\overline{BUSY}$ (*4)	t_{BS}	Memory bank function used	1	—	—	μs
Command input interval time	t_{INT}	f_{OSC} = 4.096 MHz; At STOP, SLOOP, CLOOP or VOL command input	6	—	—	μs
Command input enable time	t_{cm}	f_{OSC} = 4.096 MHz; During continuous playback; At SLOOP input	—	—	10	ms
"L" level output time of NCR and $\overline{BUSY}$ at PUP1 command input	t_{PUP1}	When a 4.096 MHz external clock is input	1.9	2.0	2.1	ms
"L" level output time of NCR and $\overline{BUSY}$ at PUP2 command input	t_{PUP2}	When a 4.096 MHz external clock is input	65	66	67	ms
"L" level output time of NCR and $\overline{BUSY}$ at PDWN1 command input	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	6	μs
"L" level output time of NCR and $\overline{BUSY}$ at PDWN2 command input	t_{PD2}	f_{OSC} = 4.096 MHz	63	64	65	ms
NCR "L" level output time 1 (*1)	t_{NCR1}	f_{OSC} = 4.096 MHz	—	—	6	μs
NCR "L" level output time 2 (*2)	t_{NCR2}	f_{OSC} = 4.096 MHz; After phrase data input by the PLAY command	—	4.125	4.38	ms
$\overline{BUSY}$ "L" level output time (*3)	t_{BSY}	f_{OSC} = 4.096 MHz	—	—	6	μs

Note: Output pin load capacitance = 55 pF (Max)

*1: Applies to cases where a command is input except after a PUP1, PUP2, PDWN1, PDWN2, SLOOP, or CLOOP command input or except after a phrase data input by the PLAY command.

*2: Indicates the time when the sampling frequency of the phrase played last was 4 kHz. For any other sampling frequency, the NCR "L" output time 2 is proportional to that sampling frequency. After reset release, a sampling freuency is set to 4 kHz.
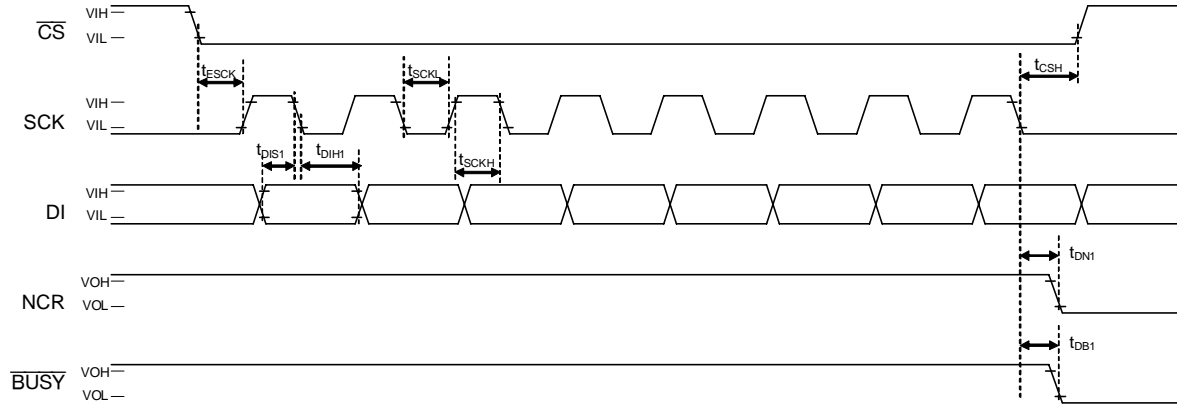
*3:　Applies to when a command is input except after a PUP1, PUP2, PDWN1, PDWN2, SLOOP, or CLOOP command input or except after a phrase data input by the PLAY command, providing no phrase is being played.

*4:　For ML22802/ML22P802, applied to the SEL pin.
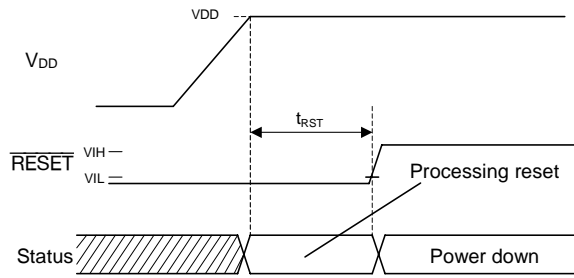
TIMING DIAGRAMS

Serial CPU Interface Timing (When DIPH = "L")
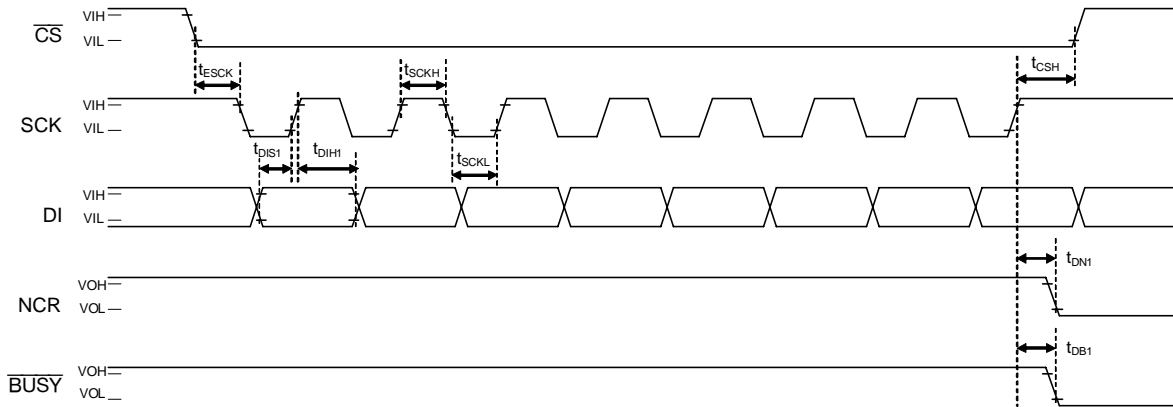
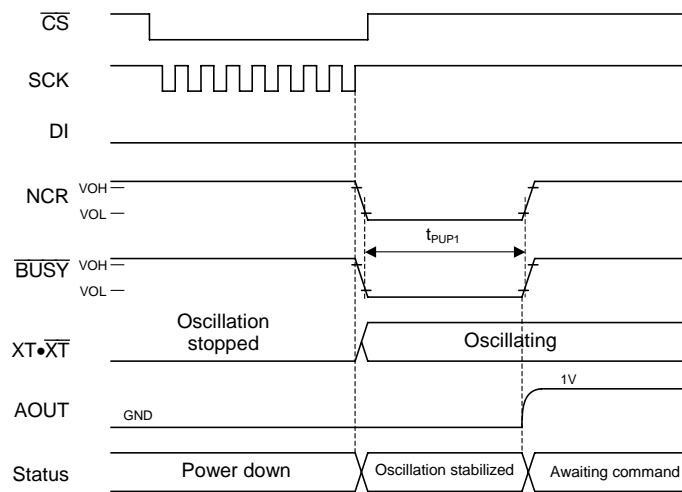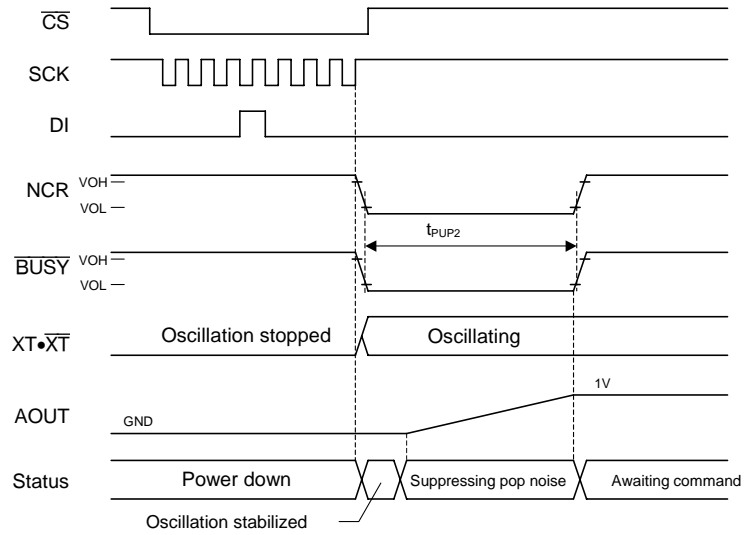
Serial CPU Interface Timing (When DIPH = "H")

Power-On Timing

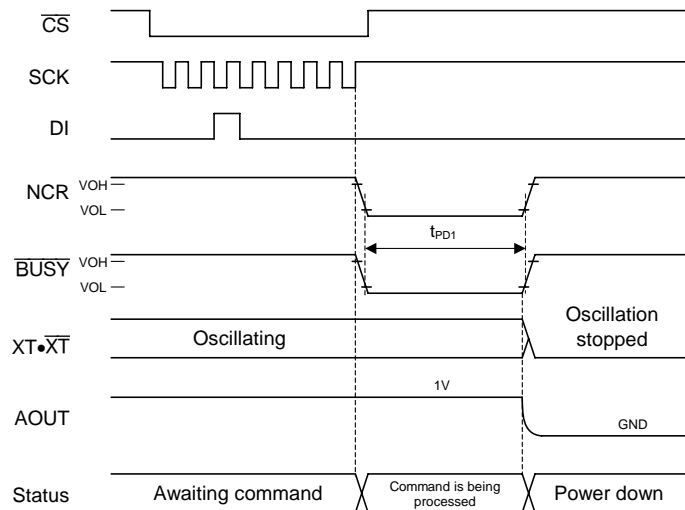
Oscillation is stopped at power-on.

Power-Up Timing

• PUP1 command input

• PUP2 command input

Power-Down Timing

• PDWN1 command input

● PDWN2 command input
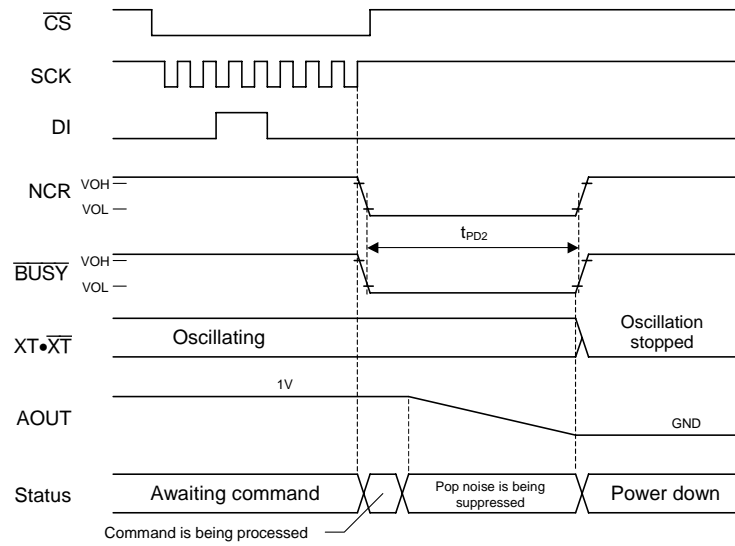
● $\overline{\text{RESET}}$ input
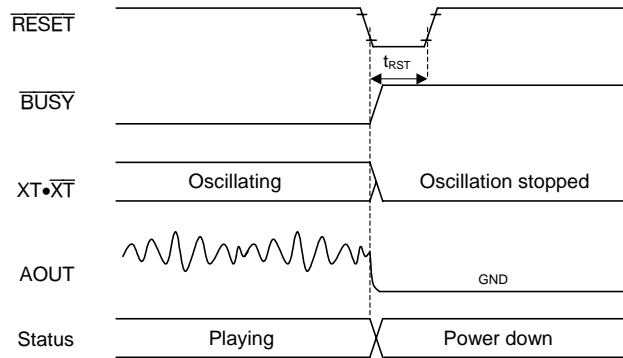
Note: The same timing applies in cases where the $\overline{\text{RESET}}$ signal is input during waiting for command.

• Playback Timing by the PLAY Command
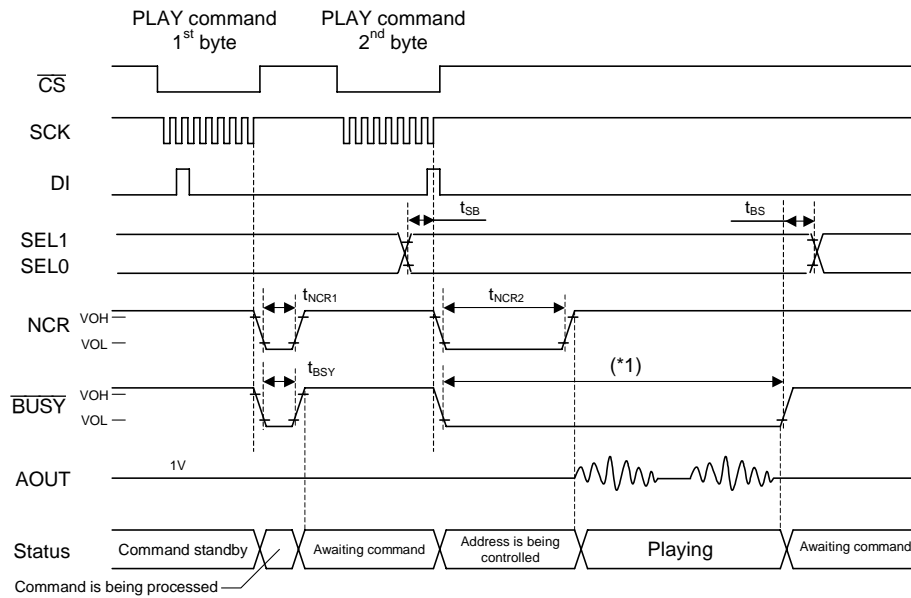
Note: Length of a "L" interval of $\overline{\text{BUSY}}$ is = t_{NCR2} + voice reproduction time length.

• Playback Stop Timing
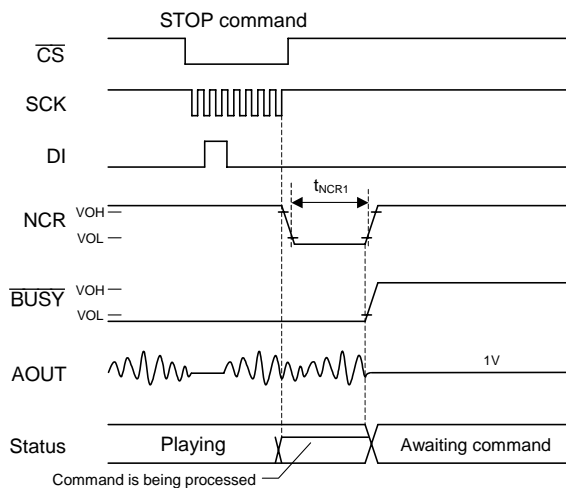
• Continuous Playback Timing by the PLAY Command
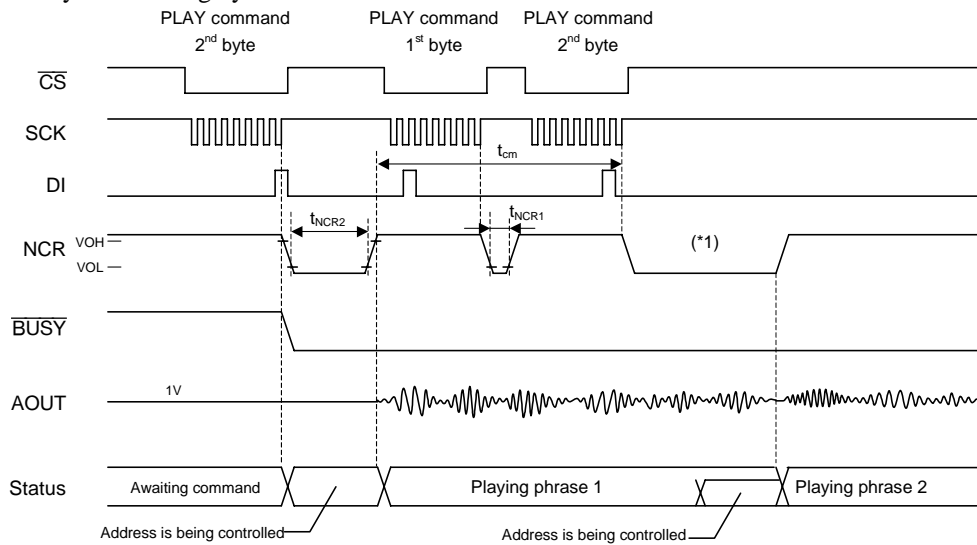
*1:   The "L" level period of the NCR pin during playback varis depending on the timing at which the PLAY command is input.
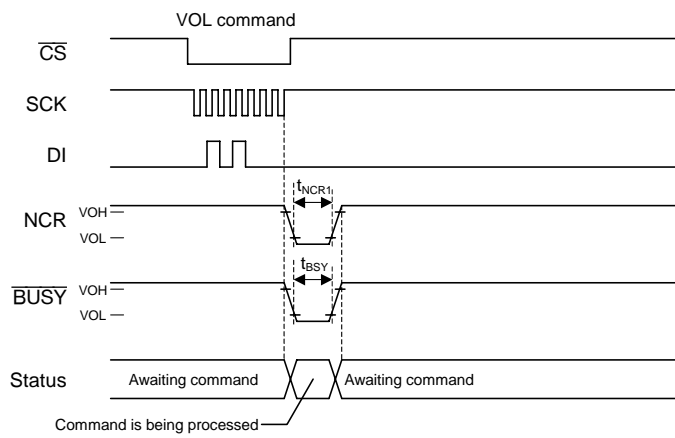
• Silence Insertion Timing by the MUON Command
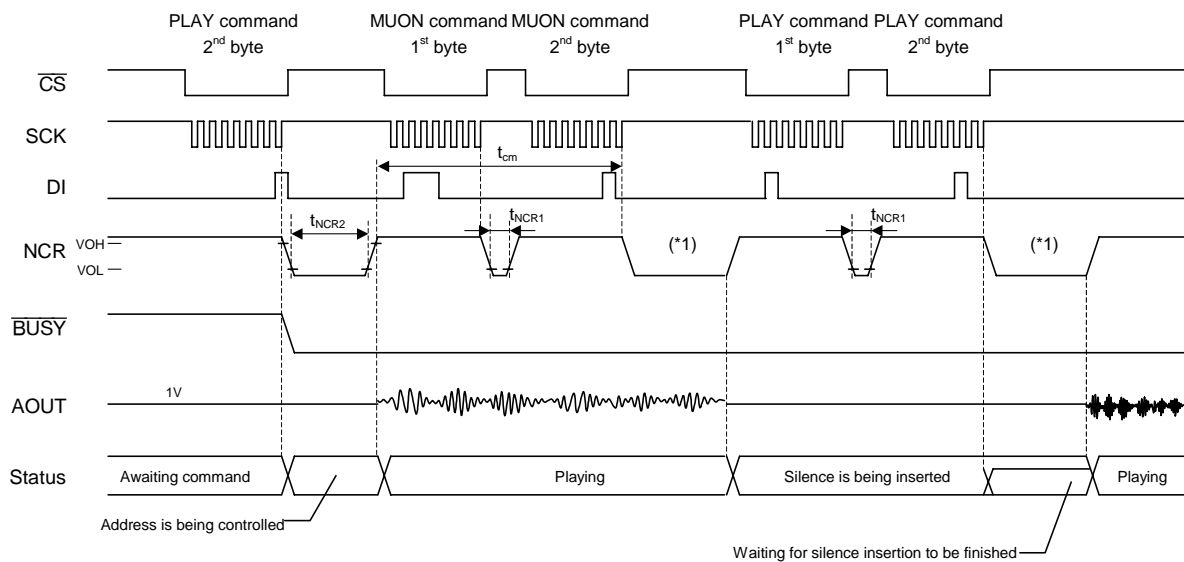
*1:   The "L" level period of the NCR pin during playback or silence insertion operation varis depending on the timing at which the MUON command is input.

• Repeat Playback Set/Release Timing by the SLOOP and CLOOP Commands
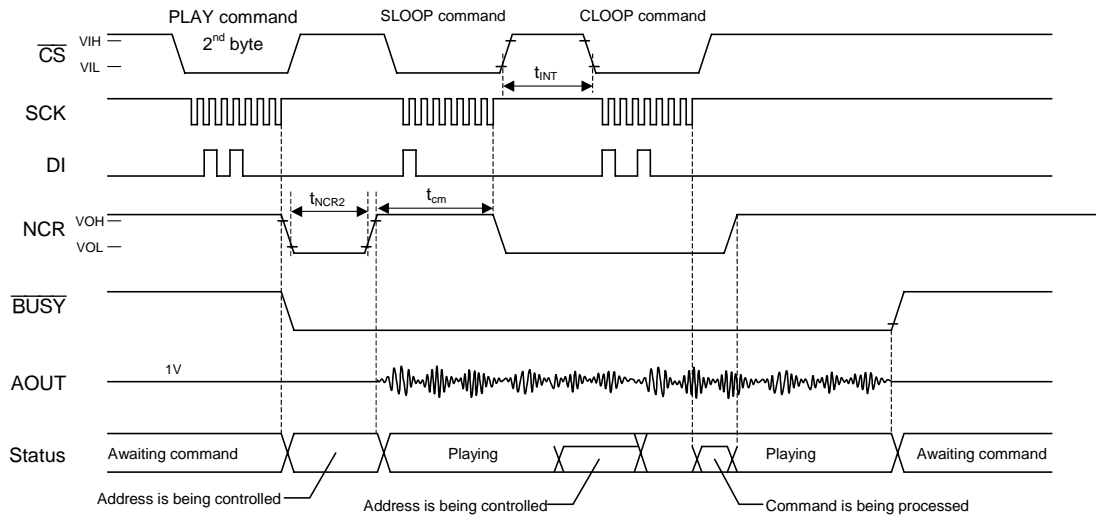
• Volume Change Timing by the VOL Command

FUNCTIONAL DESCRIPTION

Serial CPU Interface

Command data can be input through the DI pin by signals input through the $\overline{CS}$ and SCK pins.

Setting the $\overline{CS}$ pin to a "L" level enables the serial CPU interface.

After the $\overline{CS}$ pin is set to a "L" level, the command data, which is synchronized with the SCK clock signal, is input through the DI pin from the MSB.   The command data input through the DI pin is shifted into the LSI on the rising or falling edges of the SCK clock pulses and the command is executed by the rising or falling edge of the eighth pulse of the SCK clock.

Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:
  - When the DIPH pin is at a "L" level, the data input through the DI pin is shifted into the LSI on the rising edges of the SCK clock pulses.
  - When the DIPH pin is at a "H" level, the data input through the DI pin is shifted into the LSI on the falling edges of the SCK clock pulses.

It is possible to input command data in the LSI even by holding the $\overline{CS}$ pin continuously at a "L" level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted.   As a result, command data cannot be input correctly.   Setting the $\overline{CS}$ pin to a "H" level returns the count of the SCK clock pulses to the initial state.

Command and Data Input Timings
  • SCK rising edge operation (when DIPH pin = "L" level)
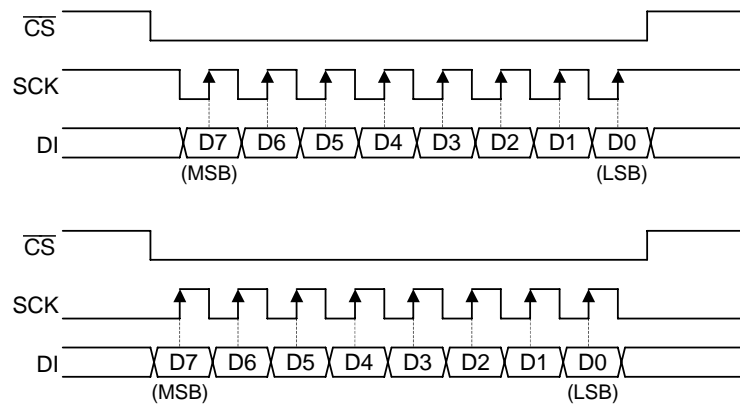
  • SCK falling edge operation (when DIPH pin = "H" level)
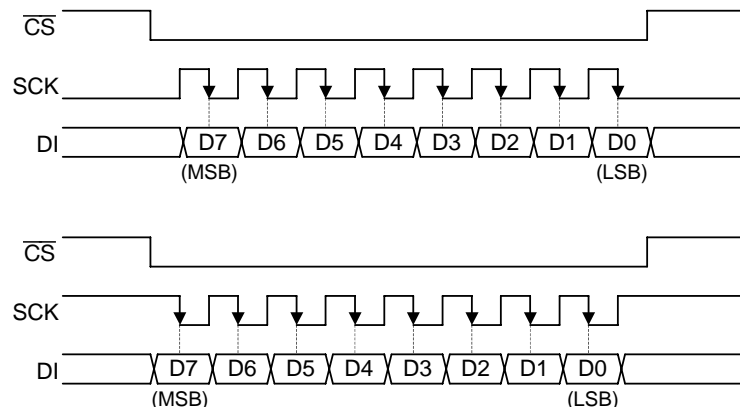
Command List

Each command is configured in 1-byte (8-bit) units. Each of the PLAY and MUON command forms one command by two bytes each.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	—	—	S1	S0	Instantly shifts the device currently powered down to a command wait state.
PUP2	0	0	0	1	—	—	S1	S0	Suppresses pop noise and shifts the device currently powered down to a command wait state.
PDWN1	0	0	1	0	—	—	—	—	Instantly shifts the device from a command wait state to a power down state.
PDWN2	0	0	1	1	—	—	—	—	Suppresses pop noise and shifts the device from a command wait state to a power down state.
PLAY	0	1	0	0	—	—	—	—	Phrase-specified playback start command. Use the data of the 2nd byte to specify a phrase number.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	—	—	—	—	Playback stop command.
MUON	0	1	1	1	—	—	—	—	Inserts silence. Use the data of the 2nd byte to specify the length of silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	—	—	—	—	Command for setting the repeat playback mode. Enabled during playback.
CLOOP	1	0	0	1	—	—	—	—	Command for releasing the repeat playback mode. If the STOP command is input, repeat playback mode is released automatically.
VOL	1	0	1	0	V3	V2	V1	V0	Volume setting command.

S1, S0   : Number of memory banks (*)
F7–F0   : Phrase address
M7–M0   : Length of silence period
V3–V0   : Sound volume

* S0 is fixed to "0" for ML22802/ML22P802.

Power Down Function

This LSI has the power down function.   When in a power down state, all the circuits including the oscillator circuit stop operating, thus minimizing the supply current.   When supplying an external clock to the XT pin, tie the pin at a "L" level during power down.

The figure below shows a equivalent circuit to an oscillator circuit.

Power down signal
(During power down = "L")

approx. 1 MΩ

Master clock inside the LSI

XT $\overline{XT}$
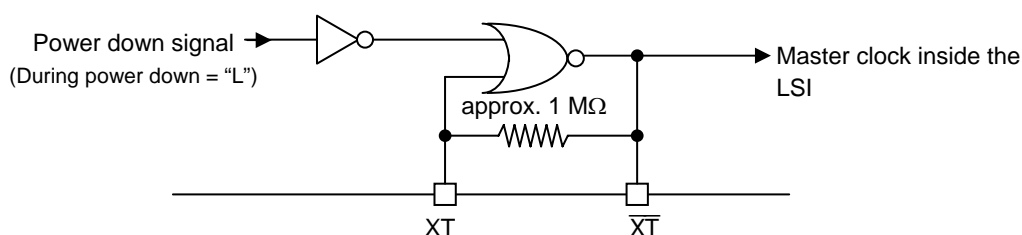
The Initial Status at Reset Input and the Status at Power Down of Output Pins

The status of relative output pins at reset input and power down is shown below.

Digital output pin	State	Analog output pin	State
NCR	"H" level	AOUT	GND level
$\overline{BUSY}$	"H" level		

Voice Synthesis Algorithm

The ML22804/ML22808-xxx contain four algorithm types to match the characteristic of playback voice: 4-bit ADPCM2 algorithm, 8-bit straight ADPCM2 algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
4-bit ADPCM2	Normal voice waveform	LAPIS Semiconductor 's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm, which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM		Normal 8-bit PCM algorithm
16-bit PCM		Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the ROM's voice data.   It contains data for controlling the start/stop addresses of voice data for 256 phrases, use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data.   For the details, refer to the section of "Edit ROM Function."
No edit ROM area is available unless the edit ROM is used.

The ROM data is created using a dedicated tool.

ROM address (ML22808/ML22804/ML22802-XXX, ML22P808/ML22P804/ML22P802)

0x00000 0x007FF	Voice control area (Fixed16 Kbits)
0x00800 0x00807	Test area
0x00808 Max: 0xFFFFF	Voice area
Max: 0xFFFFF	Edit ROM area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.
The equation below gives the playback time when the edit ROM function is not used.

(Bit length is 2 bits for 2-bit ADPCM2; 4 bits for 4-bit ADPCM2; 8 bits for PCM.)

Example
: Let the sampling frequency be 16 kHz and 4-bit ADPCM2 algorithm.   Then the playback time is approx. 65 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (4096 - 16) \text{ (Kbit)}}{16 \text{ (kHz)} \times 4 \text{ (bit)}} \cong 65 \text{ (sec)}$$

Edit ROM Function

The edit ROM function makes it possible to play back multiple phrases in succession.   The following functions are set using the edit ROM function:
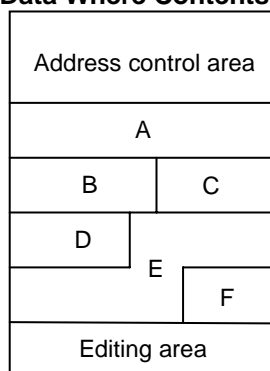
- Continuous playback: There is no limit to the number of times a continuous playback can be specified.   It depends on the memory capacity only.
- Silence insertion function: 20 to 1024 ms

Using the edit ROM function enables an effective use of the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the edit ROM function.

Example 1:   Phrases Using the Edit ROM Function

Phrase 1	A	B	D		
Phrase 2	A	C	D		
Phrase 3	E	B	D		
Phrase 4	E	C	D		
Phrase 5	A	B	D	Silence	E	C	D
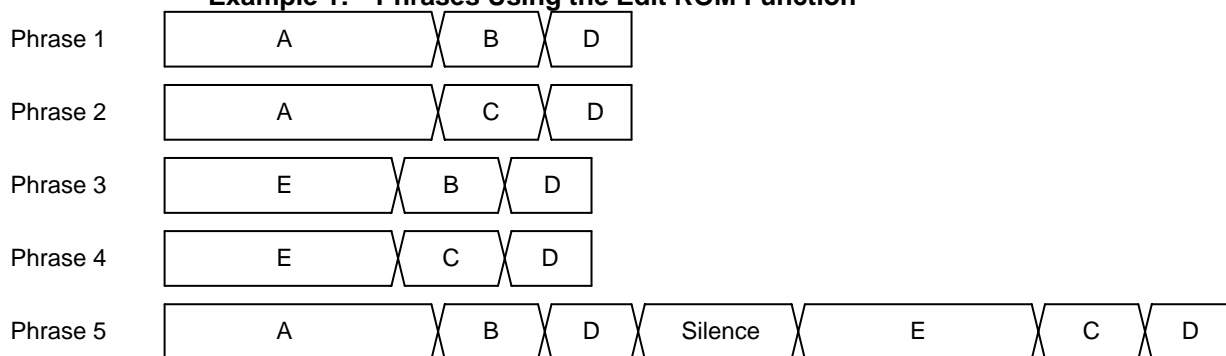
Example 2:   Example of ROM Data Where Contents of Example 1 Are Stored in ROM

Address control area
A
B | C
D
E
F
Editing area

Memory Bank Selecting Function

Using the memory bank selecting function, the internal ROM area in the ML22808/ML22804/ML22P808/ ML22P804 can be divided into up to four areas.   If four banks are used, up to 1024 phrases can be played back since each bank is capable of up to 256 phrases.   Using the memory bank selecting function, the internal ROM area in the MLl22802/ML22P802 can be divided into up to two areas.   If two banks are used, up to 512 phrases can be played back because each bank is capable of up to 256 phrases.   Using this function, it is possible to put together multiple ROM codes into one code.

In the case of the ML22808/ML22804/ML22P808/ML22P804, the memory is used by setting the SEL1 and SEL0 pins and in the case of the ML22802/ML22P802, the memory is used by setting the SEL pin, as shown in the tables below.   In addition, when playing phrases, it is necessary to specify the number of memory banks by PUP1 or PUP2.

"—" in the tables below means Don't Care, whether 0 or 1.

Note that, if the memory bank selecting fnction is used, it is necessary to divide data when ROM data is created and store the divided data in the specified area in advance.

For one memory banks:

SEL1	SEL0	ML22P808/ML22808-XXX	ML22P804/ML22804-XXX	SEL	ML22P802/ML22802-XXX
—	—	00000h -FFFFFh	00000h – 7FFFFh	—	00000h – 3FFFFh

For two memory banks:

SEL1	SEL0	ML22P808/ML22808-XXX	ML22P804/ML22804-XXX	SEL	ML22P802/ML22802-XXX
—	0	00000h – 7FFFFh	00000h – 3FFFFh	0	00000h – 1FFFFh
—	1	80000h – FFFFFh	40000h – 7FFFFh	1	20000h – 3FFFFh

For four memory banks:

SEL1	SEL0	ML22P808/ML22808-XXX	ML22P804/ML22804-XXX
0	0	00000h–3FFFFh	00000h–1FFFFh
0	1	40000h–7FFFFh	20000h–3FFFFh
1	0	80000h–BFFFFh	40000h–5FFFFh
1	1	C0000h–FFFFFh	60000h–7FFFFh

Shown below is an example of memory division for the M22808 (8 Mbits).

Command Function Descriptions

1.   PUP1 command

| • command | 0 | 0 | 0 | 0 | — | — | S1 | S0 |

PUP1 command is used to shift the ML22804/ML22808-xxx from power down state to the command standby state.
In the power down state, any command input other than PUP1 and PUP2 will be ignored.

The ML22804/ML22808-xxx enters the power down state in any of the following conditions:
1) When power is turned on
2) At $\overline{\text{RESET}}$ input
3) When both NCR and $\overline{\text{BUSY}}$ go to a "H" level after inputting the power down command.

The relationship between S1/S0 and the memory bank is as follows.

S1	S0	ML22808/ML22804/ML22P808/ML22P804	ML22802/ML22P802
0	0	Uses the entire space of the internal memory as one area.	Uses the entire space of the internal memory.
0	1	Divides the internal memory into two areas to select the memory areas with the SEL0 pin.	Setting prohibited (fix S0 to "0")
1	0	Divides the internal memory into four areas to select the memory areas with the SEL0 and SEL1 pins.	Divides the internal memory into two areas to select the memory areas with the SEL pin.
1	1	Setting prohibited	Setting prohibited (Fix S0 to "0".)
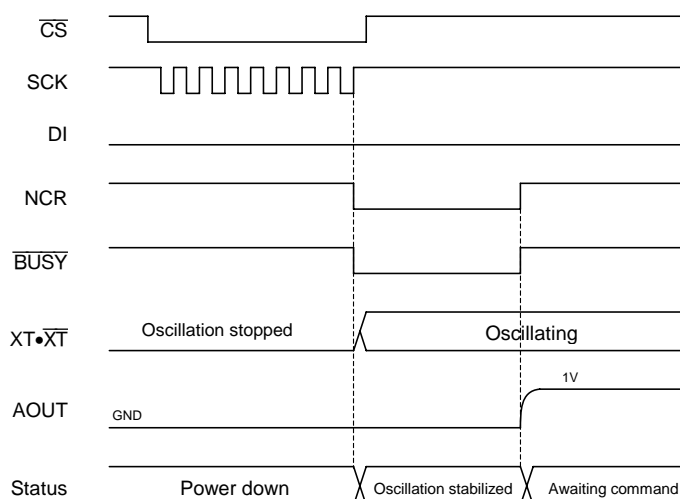
The oscillation starts when the PUP1 command is input and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output abruptly changes from GND level to approx. 1 V level.   Therefore, this abrupt change in AOUT output will cause generation of pop noise if the AOUT output is not processed outside. To suppress pop noise, input the PUP2 command.
Any command that is input during oscillation stabilization will be ignored.   However, if a "L" level is input to the $\overline{\text{RESET}}$ pin, the device enters the power down state immediately.

2.   PUP2 command

- command

0	0	0	1	—	—	S1	S0

PUP2 command is used to shift the ML22804/ML22808-xxx from the power down state to the command standby state.
In the power down state, any command input other than PUP1 and PUP2 will be ignored.

The ML22804/ML22808-xxx enters the power down state in any of the following conditions:
  1) When power is turned on
  2) At $\overline{RESET}$ input
  3) When both NCR and $\overline{BUSY}$ go to a "H" level after inputting the power down command.

The relationship between S1/S0 and the memory bank is as follows.

S1	S0	ML22808/ML22804/ML22P808/ML22P804	ML22802/ML22P802
0	0	Uses the entire space of the internal memory.	Uses the entire space of the internal memory.
0	1	Divides the internal memory into two areas to switch the memory areas with the SEL0 pin.	Setting prohibited (fix S0 to "0")
1	0	Divides the internal memory into four areas to switch the memory areas with the SEL0 and SEL1 pins.	Divides the internal memory into two areas to select the memory areas with the SEL pin.
1	1	Setting prohibited (Operation is the same as above.)	Setting prohibited (Fix S0 to "0".)
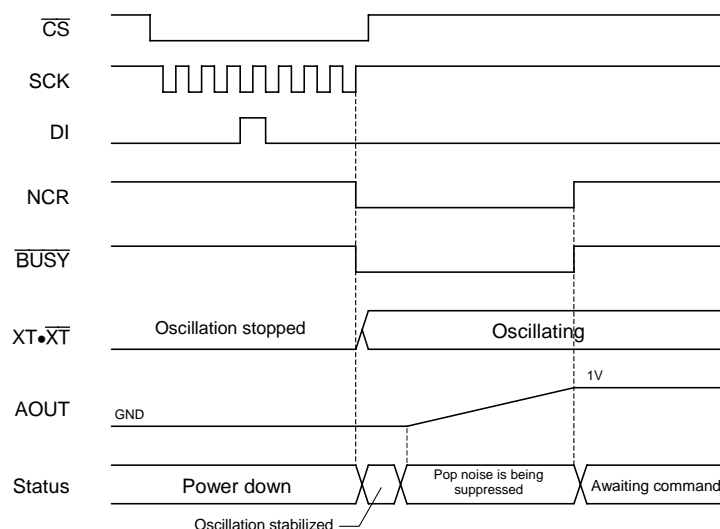
The oscillation starts when the PUP2 command is input and, after an elapse of about 2 ms oscillation stabilization time, the AOUT output gradually changes from GND level to approx. 1 V level in about 64 ms.

Any command that is input during oscillation stabilization will be ignored.   However, if a "L" level is input to the $\overline{RESET}$ pin, the device enters the power down state immediately.

3.   PDWN1 command

• command

0	0	1	0	—	—	—	—

The PDWN1 command is used to shift the ML22804/ML22808-xxx from a command wait state (both NCR and $\overline{\text{BUSY}}$ are "H") to a power down state.   However, this command is disabled during playback.
To resume playback after the ML22804/ML22808-xxx has shifted to the power down state, first input the PUP1 or PUP2 command and then input the PLAY command.
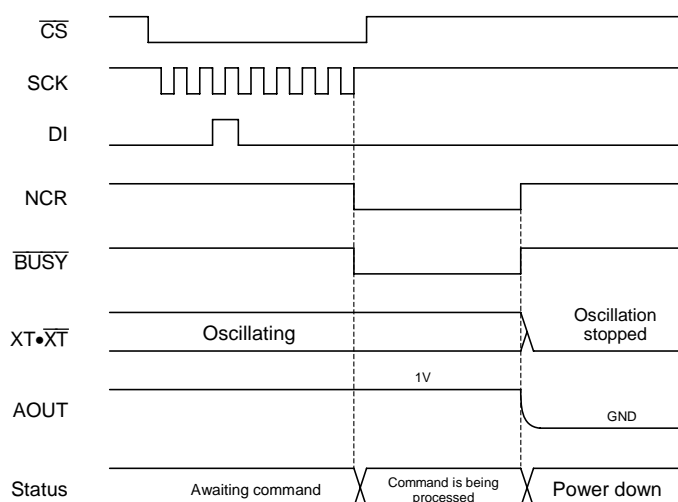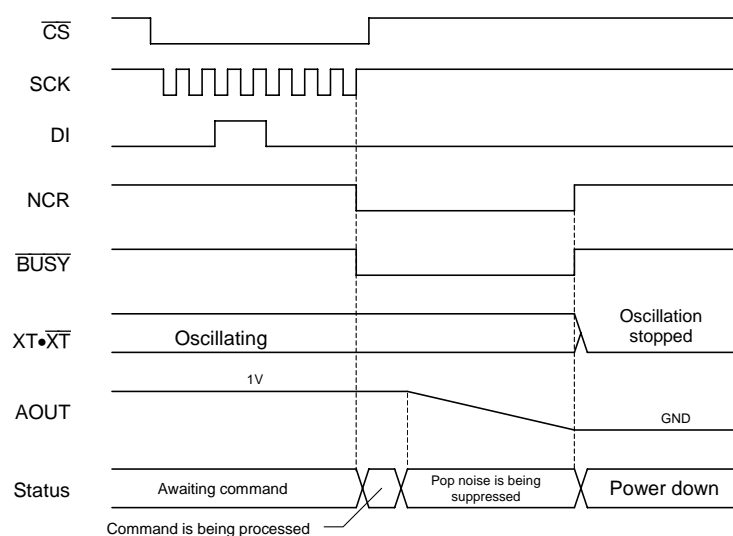

After the PDWN1 command is input and after an elapse of command processing time, the oscillation stops and the AOUT output abruptly changes from approx. 1 V level to GND level.   This abrupt change in the AOUT output will cause generation of pop noise if the AOUT output is not processed outside.   To suppress pop noise, input the PDWN2 command.

4.   PDWN2 command

• command

0	0	1	1	—	—	—	—

The PDWN2 command is used to shift the ML22804/ML22808-xxx from a command wait state (both NCR and $\overline{BUSY}$ are "H") to a power down state.   However, this command is disabled during playback.

To resume playback after the ML22804/ML22808-xxx has shifted to the power down state, first input the PUP1 or PUP2 command and then input the PLAY command.

After the PDWN1 command is input and after an elapse of command processing time, the oscillation stops and the AOUT output gradually changes from approx. 1 V level to GND level in about 64 ms.

Any command that is input while pop noise is being suppressed will be ignored.   However, if a "L" level is input to the $\overline{RESET}$ pin, the device enters the power down state immediately.

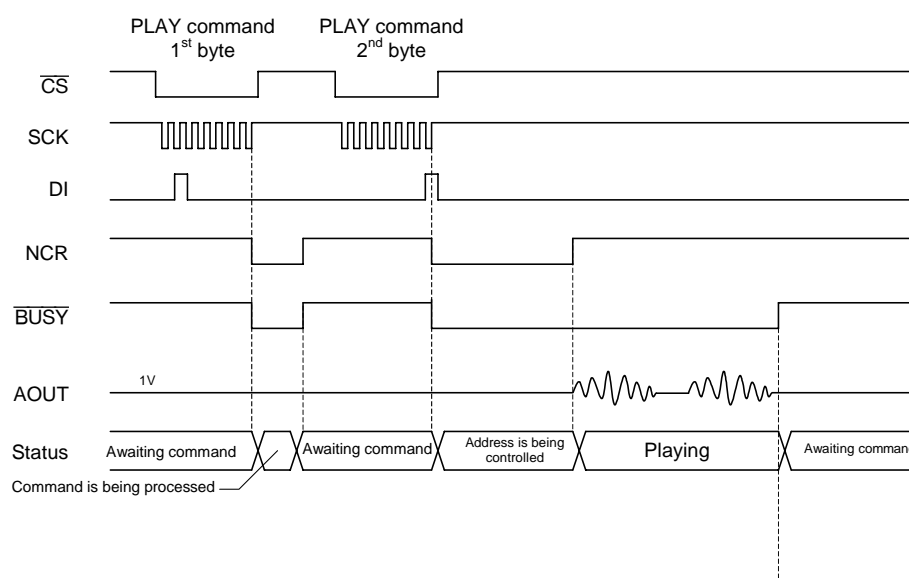5.   PLAY command

• command

0	1	0	0	—	—	—	—	1st byte
F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The PLAY command is a 2-byte command.   Set the playback phrase using the second byte of this command.
The PLAY command can be input when the NCR signal is at a "H" level.
Since it is possible to specify the playback phrase (F7 to F0) at the time of creating the ROM that stores voice
data, set the phrase that was set when the ROM was created.
Figure below shows the timing of phrase (F7 to F0 = 01H) playback.

When the 1st byte of the PLAY command is input, the device enters a state in which it waits for the 2nd byte to be
input after the elapse of the command processing time.   When the 2nd byte of PLAY command is input, after an
elapse of the command processing time, the device starts reading from the ROM the address information of the
phrase to be played.   Thereafter, playback operation starts, the playback is performed up to the specified ROM
address, and then the playback ends automatically.
The NCR1 signal is at a "L" level during address control, and goes "H" when the address control is finished and
playback is started.   When this NCR signal goes "H", then it is possible to input the PLAY command for the
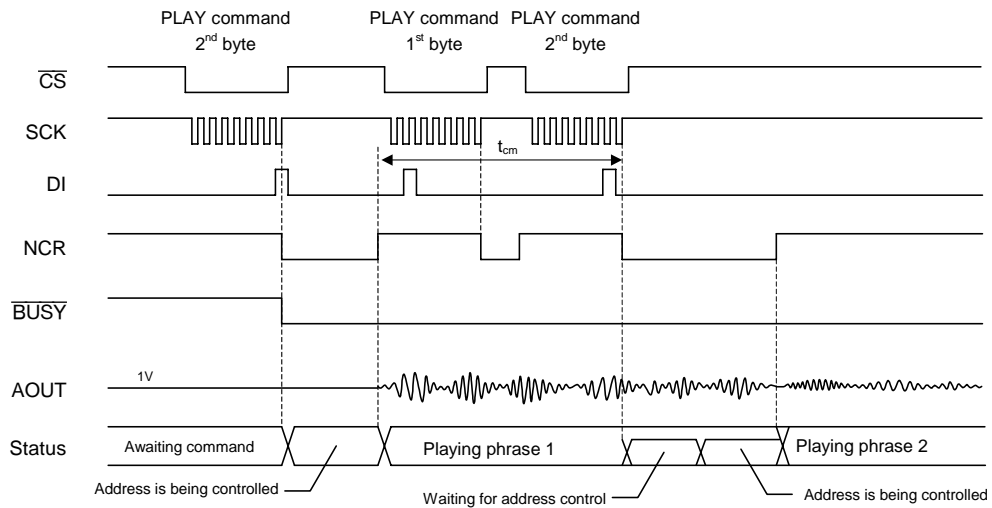next playback phrase.
During address control, the $\overline{BUSY}$ signal is at a "L" level during playback and goes "H" when playback is
finished.   Whether the playback is going on can be known by the $\overline{BUSY}$ signal.

Time Required for Address Control

The time required for controlling the address of the playback phrase after input of the PLAY command is the
time of 16 to 17 periods of the sampling frequency of the the phrase that was played last.   After power is turned
on or after $\overline{RESET}$ is input, it is the time of 16 to 17 periods of 4 kHz sampling frequency.

PLAY Command Input Timing for Continuous Playback

The diagram below shows the PLAY command input timing in cases where one phrase is played and then the next phrase is played in succession.

As shown in the diagram above, if continuous playback is carried out, input the PLAY command for the second phrase within 10 ms (tcm) after NCR goes "H". This will make it possible to start playing the second phrase immediately after the playback of the first phrase finishes. Phrases can thus be played back continuously without inserting silence between phrases.
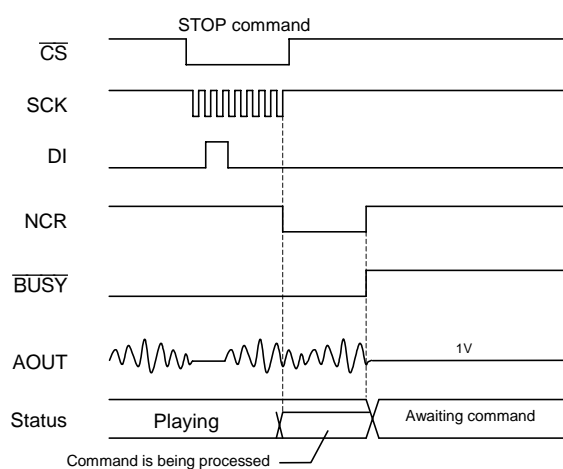
6.   STOP command

      • command | 0 | 1 | 1 | 0 | — | — | — | — |

The STOP command is used to stop playback.   When speech synthesis processing stops, the AOUT output becomes $1/4V_{DD}$ and the NCR and $\overline{BUSY}$ signals go "H".
Although it is possible to input the STOP command regardless of the status of NCR during playback, a prescribed command interval time needs taking.
Note that STOP command input during power down, shifting to power up, and shifting to power down will be ignored.

Because the AOUT output abruptly changes to approx. 1 V level after the STOP command is input, pop noise may be generated.   To prevent pop noise, input the STOP command after gradually decreasing the volume by the VOL command.

7.   MUON command

- command

0	1	1	1	—	—	—	—	1st byte
M7	M6	M5	M4	M3	M2	M1	M0	2nd byte

The MUON command is a 2-byte command.   This command is used to insert silence between the two playback phrases.   The MUON command is enabled when the NCR signal is at a "H" level.   Set the silence time length using the second byte of this command.

As the silence length (M7 to M0), a value between 4 ms and 1024 ms can be set in 4 ms intervals (252 steps in total).

The equation to set the silence time length is shown below.

The silence length (M7-M0) must be set to 04h or higher.

$$t_{mu} = (2^7 \times (M7) + 2^6 \times (M6) + 2^5 \times (M5) + 2^4 \times (M4) + 2^3 \times (M3) + 2^2 \times (M2) + 2^1 \times (M1) + 2^0 \times (M0) + 1) \times 4ms$$

The timing diagram shown below is a case of inserting a silence of 20 ms between the repetitions of a phrase of (F7–F0) = 01h.
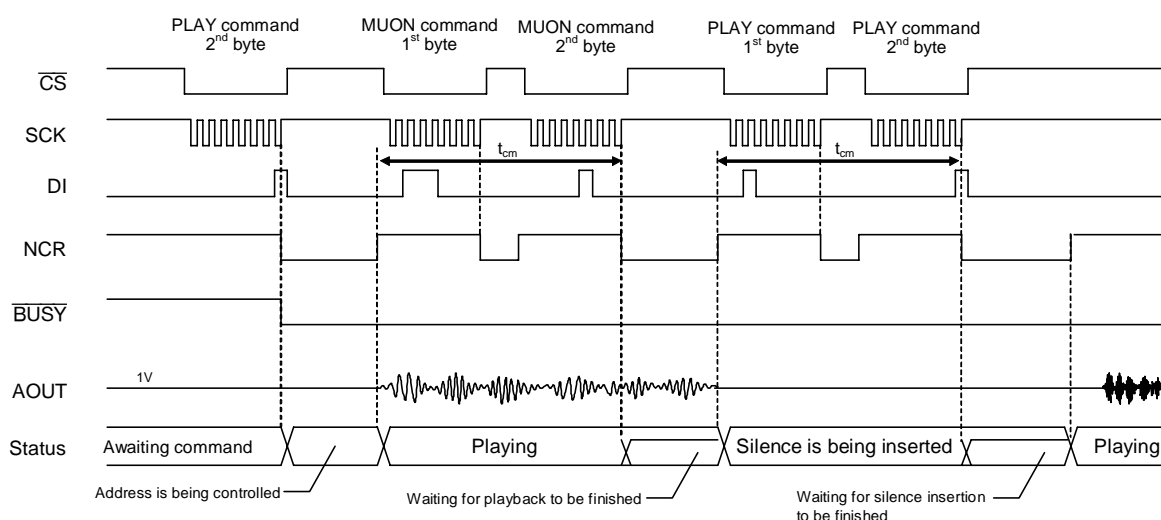
When the PLAY command is input, the address control of phrase 1 ends, the phrase playback starts, and the NCR signal goes "H" level.   Input the MUON command after this NCR signal changes to the "H" level.   After the MUON command input, the NCR signal remains "L" up to the end of phrase 1 playback, and the device enters a state waiting for the phrase 1 playback to end.

When the phrase 1 playback finishes, the silence playback starts, and NCR1 signal goes "H" level.   After this NCR signal has changed to the "H" level, re-input the PLAY command in order to play phrase 1.

After the PLAY command input, the NCR signal once again returns to "L" level and the device enters the state waiting for the end of silence playback.

When the silence playback finishes and then the phrase 1 playback starts, the NCR signal goes "H", and the device enters a state in which it is possible to input the next PLAY or MUON command.

The $\overline{BUSY}$ signal remains "L" until the end of a series of playback.

8.   SLOOP command

• command

| 1	0	0	0	—	—	—	—

The SLOOP command is used to set repeat playback mode.   The CLOOP command is used to release repeat playback mode.
Since the SLOOP command is valid only during playback, be sure to input the SLOOP command while the NCR signal is at a "H" level after the PLAY command is input.   The NCR signal remains "L" during repeat playback mode.
Once repeat playback mode is set, the current phrase is repeatedly played back until the repeat playback setting is released by SLOOP command or until playback is stopped by the STOP command.   In the case of a phrase using the edit function, the edited phrase is repeatedly played back.
Since repeat playback mode is released when playback is stopped by the STOP command, input the SLOOP command once again if desired to repeat the playback.
Following shows the SLOOP command input timing.
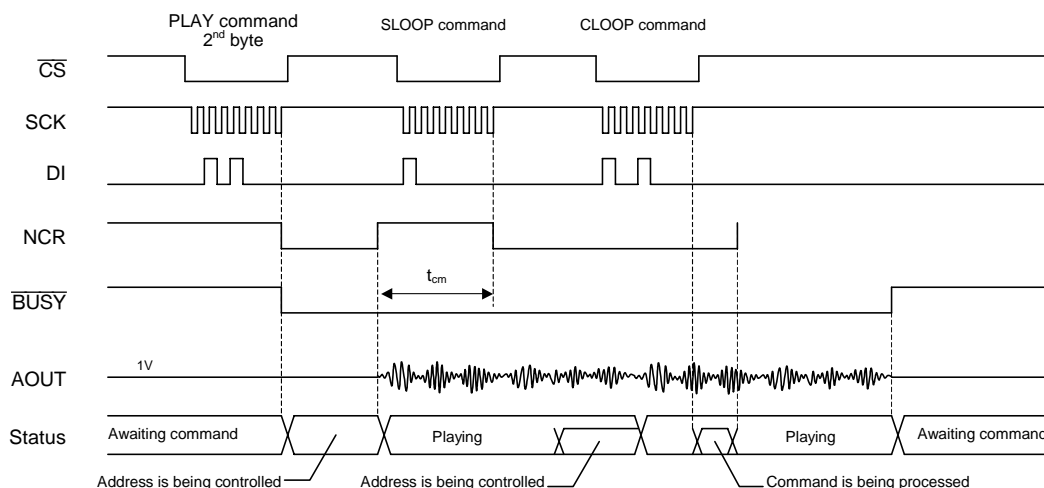
Effective Range of SLOOP Command Input

After the PLAY command is input, input the SLOOP command within 10 ms (tcm) after NCR goes "H".   This will enable the SLOOP command, so that repeat playback will be carried out.

9.   CLOOP command

  • command | 1 | 0 | 0 | 1 | — | — | — | — |

The CLOOP command releases repeat playback mode.
When repeat playback mode is released, NCR goes "H". It is possible to input the CLOOP command regardless of the NCR status during playback, but a prescribed command interval needs taking.
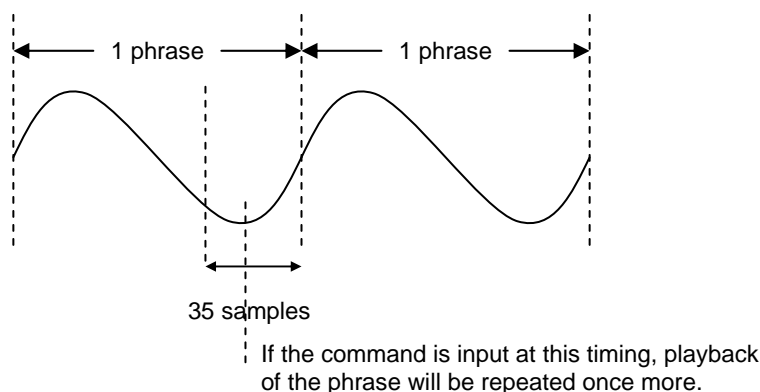
CLOOP Command Input Timing

Depending on the timing of the CLOOP command input during repeat playback, the repeat playback will end either at the end of the currently playing phrase or after one more repetition of the phrase.
The repeat playback will end at the currently playing phrase at the CLOOP command input timing shown in the table below.

Playback method	CLOOP input timing Amount of remaining voice data in the phrase being played
4-bit ADPCM2	35 samples or more
8-bit nonlinear/straight PCM	18 samples or more
16-bit straight PCM	18 samples or more

In 4-bit ADPCM2, if the CLOOP command is input 35 or more samples earlier than the time when playback of 1 phrase ends, repeat playback will end with that phrase.   If the command is input after the amount of remaining voice data becomes less than 35 samples, playback of the phrase will be repeated once more.

35 samples

If the command is input at this timing, playback
of the phrase will be repeated once more.

In 8-bit nonlinear/straight PCM or 16-bit straight PCM, if the CLOOP command is input 18 or more samples earlier than the time when playback of 1 phrase ends, repeat playback will end with that phrase. If the command is input after the amount of remaining voice data becomes less than 18 samples, playback of the phrase will be repeated once more.

18 samples

If the command is input at this timing, playback
will end with this phrase.
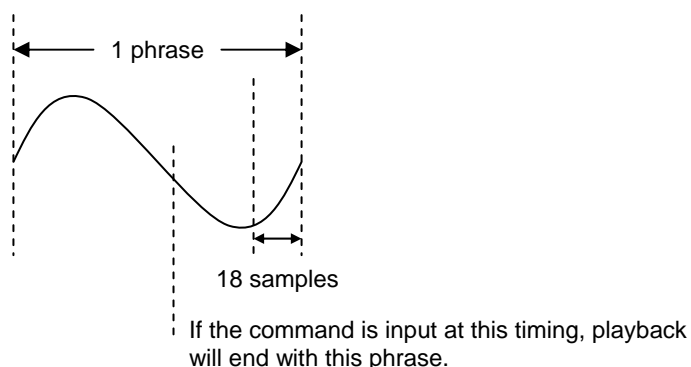
10.   VOL command

• command	1	0	1	0	V3	V2	V1	V0

The VOL command is used to adjust the playback volume.   Although it is possible to input the VOL command regardless of the status of the NCR signal, a prescribed command interval time needs taking.   Note that VOL command input during power down, shifting to power up, and shifting to power down will be ignored.

The volume can be set in 16 steps, as shown in the table below.   The initial value after reset release is set to 0 dB.   During power down or at the time of input of the STOP command, the value set by the VOL command will be retained.

| V3	V2	V1	V0	Volume
0	0	0	0	0 dB
0	0	0	1	−0.63 dB
0	0	1	0	−1.31 dB
0	0	1	1	−2.05 dB
0	1	0	0	−2.85 dB
0	1	0	1	−3.74 dB
0	1	1	0	−4.73 dB
0	1	1	1	−5.85 dB
1	0	0	0	−7.13 dB
1	0	0	1	−8.64 dB
1	0	1	0	−10.45 dB
1	0	1	1	−12.76 dB
1	1	0	0	−15.92 dB
1	1	0	1	−20.90 dB
1	1	1	0	−33.98 dB
1	1	1	1	OFF

Power Supply Wiring

The power supplies of this LSI are divided into the following three:
- Digital power supply (DV$_{DD}$)
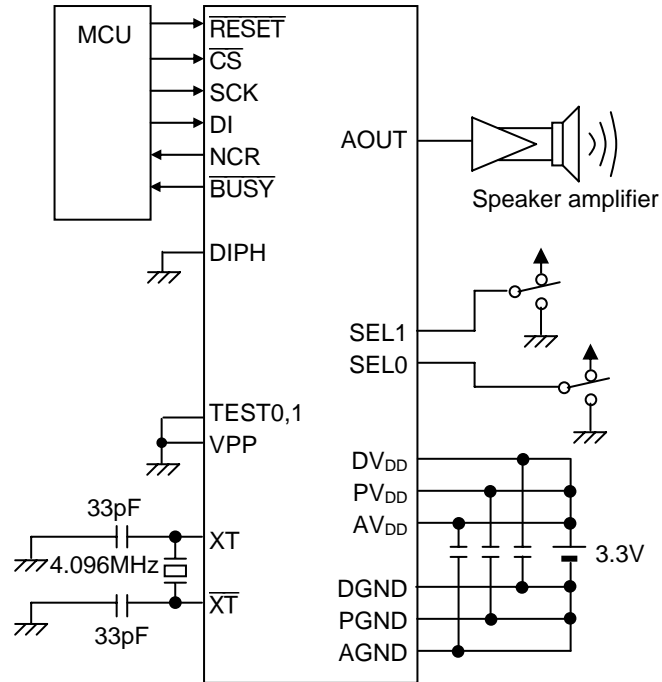- ROM power supply (PV$_{DD}$)
- Analog power supply (AV$_{DD}$)

As shown in the figure below, supply DV$_{DD}$, PV$_{DD}$, and AV$_{DD}$ from the same power supply, and separate them into analog and digital power supplies in the wiring.
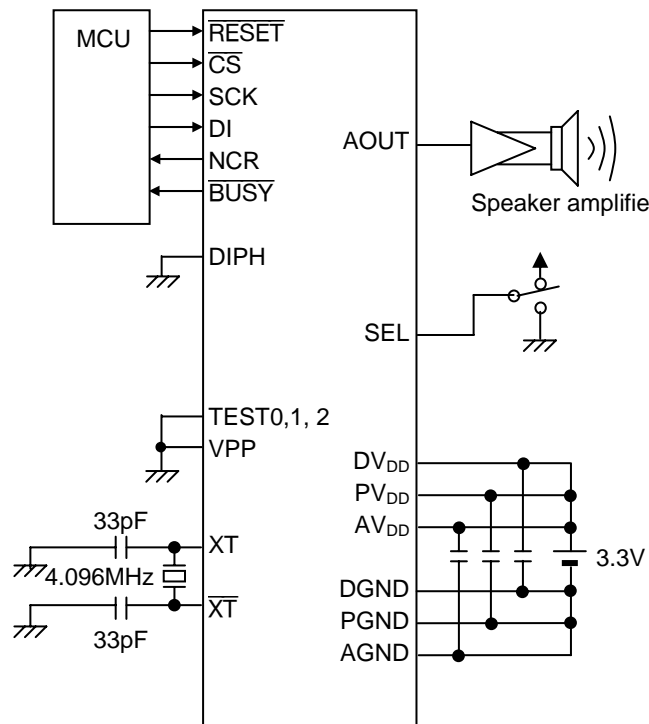
When power supply voltage = 3 V
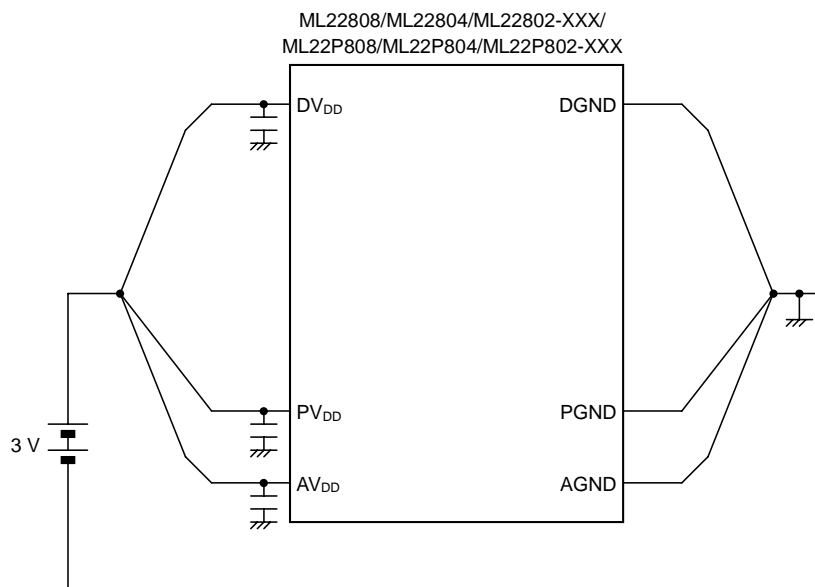
APPLICATION CIRCUITS
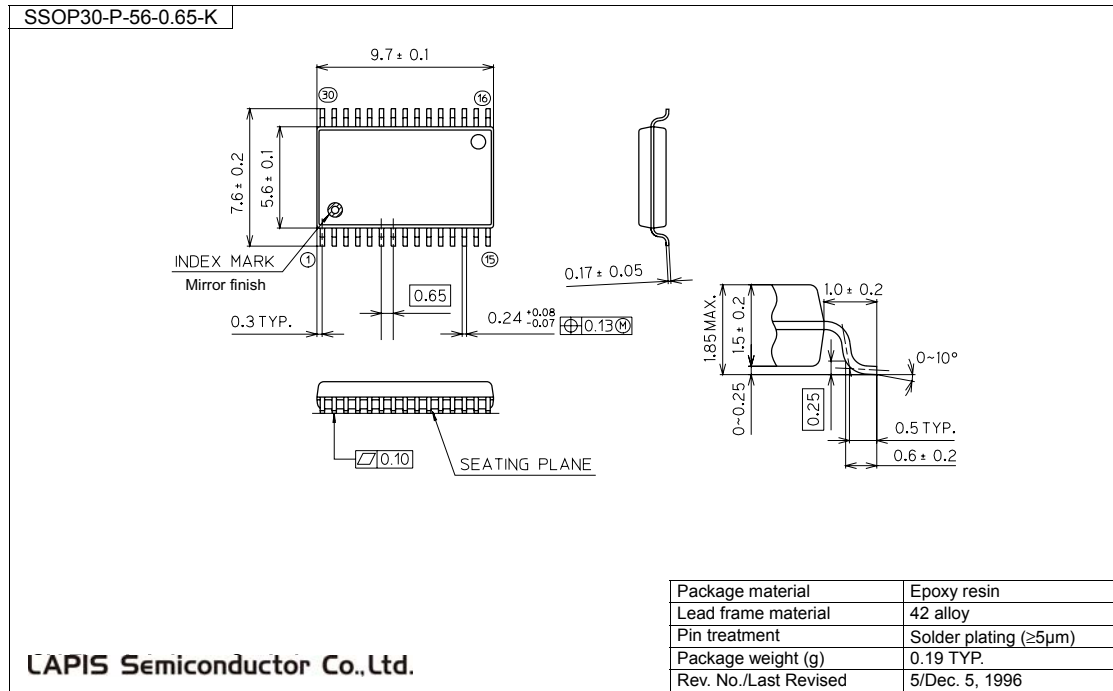
• ML22808/ML22804/ML22P808/ML22P804

• ML22802/ML22P802

PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2280XFULL-01	Sep. 29, 2006	–	–	Final edition 1
FEDL2280XFULL-02	Apr. 09, 2007	–	–	Final edition 2
		–	1 to 8, 11, 20, 22, 24 to 26, and 36	The product names (ML22802 and ML22P808/ ML22P804/ML22P802) have been added.
		–	18	Volume Change Timing by the VOL Channel in the "TIMING DIAGRAMS" Section has been modified.
FEDL2280XFULL-03	Dec.25.2007	–	22	The explanation for POWER down was modified.
		–	1,9 to 11,	Operating temperature was expanded.
FEDL2280XFULL-04	Nov. 11, 2009	41	41	Change the item of "NOTICE"

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