

Three Phase Bridge + Thyristor

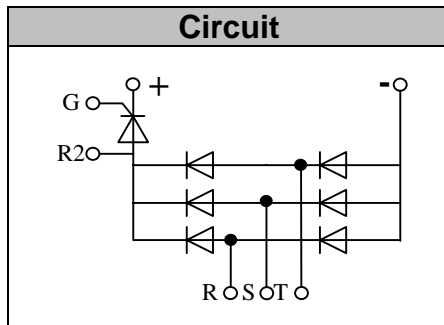
VRRM / VDRM 800 to 1600V
IFAV / ITAV 150Amp

Features

- Blocking voltage:800 to 1600V
- Three Phase Bridge and a Thyristor
- Low Forward Voltage

Applications

- Inverter for AC or DC motor control
- Current stabilized power supply
- Switching power supply
- UL E243882 approved



Module Type

TYPE	VRRM/ VDRM	VRSM
MSDT150-08	800V	900V
MSDT150-12	1200V	1300V
MSDT150-16	1600V	1700V

◆ Diode

Maximum Ratings

Symbol	Item	Conditions	Values	Units
ID	Output Current(D.C.)	Tc=93°C Three phase full wave	150	A
IFSM	Surge forward current	t=10mS Tvj =45°C	1500	A
i ² t	Circuit Fusing Consideration		11250	A ² s
Visol	Isolation Breakdown Voltage(R.M.S)	a.c.50HZ;r.m.s.;1min	3000	V
Tvj	Operating Junction Temperature		-40 to +150	°C
Tstg	Storage Temperature		-40 to +125	°C
Mt	Mounting Torque	To terminals(M4)	2±15%	Nm
Mt		To terminals(M6)	5±15%	Nm
Ms		To heatsink(M6)	5±15%	Nm
Weight		Module (Approximately)	320	g

Thermal Characteristics

Symbol	Item	Conditions	Values	Units
Rth(j-c)	Thermal Impedance, max.	Junction to Case(TOTAL)	0.14	°C/W
Rth(c-s)	Thermal Impedance, max.	Case to Heat sink	0.07	°C/W

Electrical Characteristics

Symbol	Item	Conditions	Values	Units
VFM	Forward Voltage Drop, max.	T=25°C IF =150A	1.35	V
I _{RRM}	Repetitive Peak Reverse Current, max.	Tvj =25°C VRD=VRRM Tvj =150°C VRD=VRRM	≤2 ≤10	mA mA

◆Thyristor Maximum Ratings

Symbol	Item	Conditions	Values	Units
I_{TAV}	Average On-State Current	$T_c=93^{\circ}\text{C}$, Single Phase half wave 180° conduction	150	A
I_{TSM}	Surge On-State Current	$T_{VJ}=45^{\circ}\text{C}$ $t=10\text{ms}$ (50Hz), sine $VR=0$	1500	A
i^2t	Circuit Fusing Consideration		11250	A^2s
Visol	Isolation Breakdown Voltage(R.M.S)	a.c.50HZ;r.m.s.;1 min	3000	V
T_{vj}	Operating Junction Temperature		-40 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature		-40 to +125	$^{\circ}\text{C}$
Mt	Mounting Torque	To terminals(M4)	$2\pm 15\%$	Nm
Mt		To terminals(M6)	$5\pm 15\%$	
Ms		To heatsink(M6)	$5\pm 15\%$	Nm
di/dt	Critical Rate of Rise of On-State Current	$T_{VJ}=T_{VJM}$, $V_D=1/2V_{DRM}$, $I_G=100\text{mA}$ $d_{iG}/d_t=0.1\text{A}/\mu\text{s}$	150	$\text{A}/\mu\text{s}$
dv/dt	Critical Rate of Rise of Off-State Voltage, min.	$T_J=T_{VJM}$, $V_D=2/3V_{DRM}$, linear voltage rise	500	$\text{V}/\mu\text{s}$

Electrical and Thermal Characteristics

Symbol	Item	Conditions	Values			Units
			Min.	Typ.	Max.	
V_{TM}	Peak On-State Voltage, max.	$T=25^{\circ}\text{C}$ $I_T=500\text{A}$			1.80	V
I_{RRM}/I_{DRM}	Repetitive Peak Reverse Current, max. / Repetitive Peak Off-State Current, max.	$T_{VJ}=T_{VJM}$, $V_R=V_{RRM}$, $V_D=V_{DRM}$			40	mA
V_{TO}	Threshold voltage	$T_{VJ}=T_{VJM}$			0.85	V
r_T	Slope resistance				1.5	$\text{m}\Omega$
V_{GT}	Gate Trigger Voltage, max.	$T_{VJ}=25^{\circ}\text{C}$, $V_D=6\text{V}$			3	V
I_{GT}	Gate Trigger Current, max.	$T_{VJ}=25^{\circ}\text{C}$, $V_D=6\text{V}$			150	mA
V_{GD}	Max. required DC gate voltage not to trigger	$T_{VJ}=125^{\circ}\text{C}$, $V_D=2/3V_{DRM}$			0.25	V
I_{GD}	Max. required DC gate current not to trigger	$T_{VJ}=125^{\circ}\text{C}$, $V_D=2/3V_{DRM}$			10	mA
I_L	Maximum latching current	$T_{VJ}=25^{\circ}\text{C}$, $R_G=33\Omega$		300	1000	mA
I_H	Maximum holding current	$T_{VJ}=25^{\circ}\text{C}$, $V_D=6\text{V}$		150	400	mA
tgd	Gate controlled delay time	$T_{VJ}=25^{\circ}\text{C}$, $I_G=1\text{A}$, $d_{iG}/dt=1\text{A}/\mu\text{s}$		1		μs
tq	Circuit commutated turn-off time	$T_{VJ}=T_{VJM}$		100		μs
Rth(j-c)	Thermal Impedance, max.	Junction to Case			0.16	$^{\circ}\text{C}/\text{W}$
Rth(c-s)	Thermal Impedance, max.	Case to Heatsink			0.07	$^{\circ}\text{C}/\text{W}$

Performance Curves

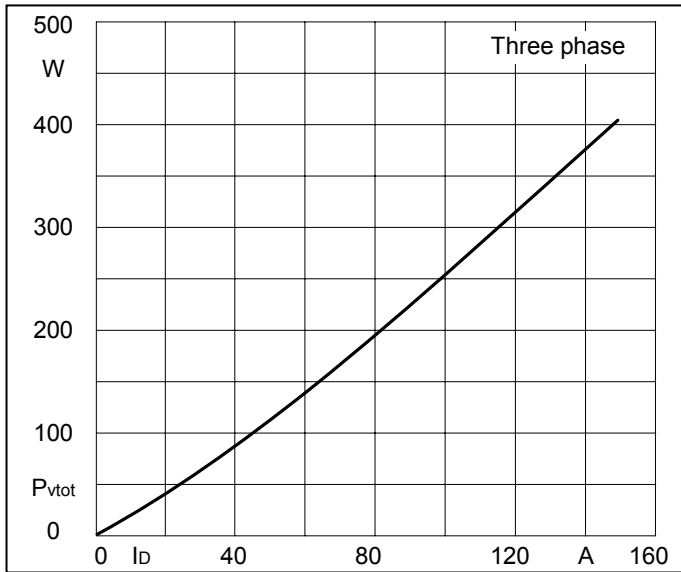


Fig1. Power dissipation

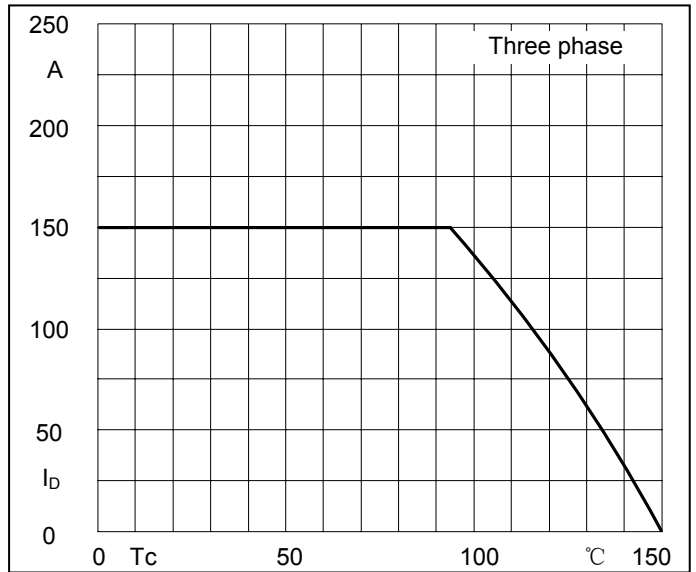


Fig2. Forward Current Derating Curve

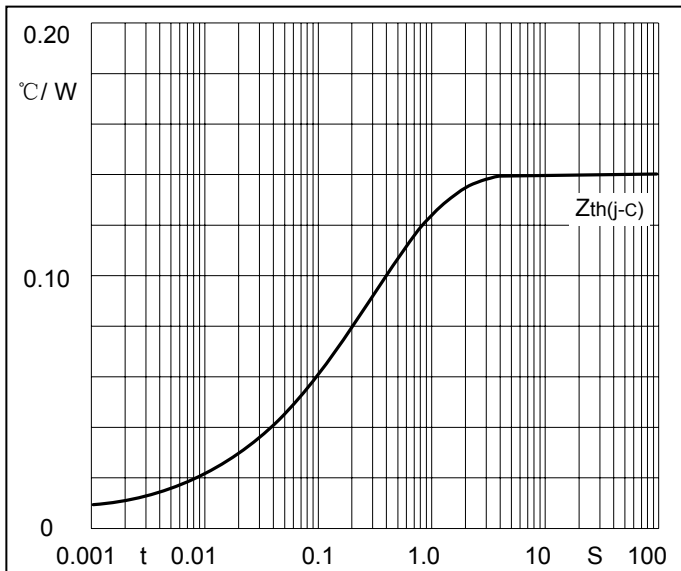


Fig3. Transient thermal impedance

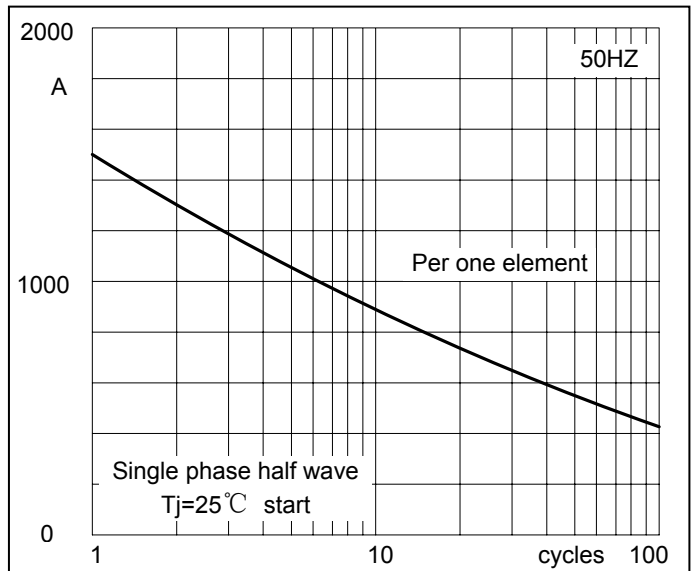


Fig4. Max Non-Repetitive Forward Surge Current

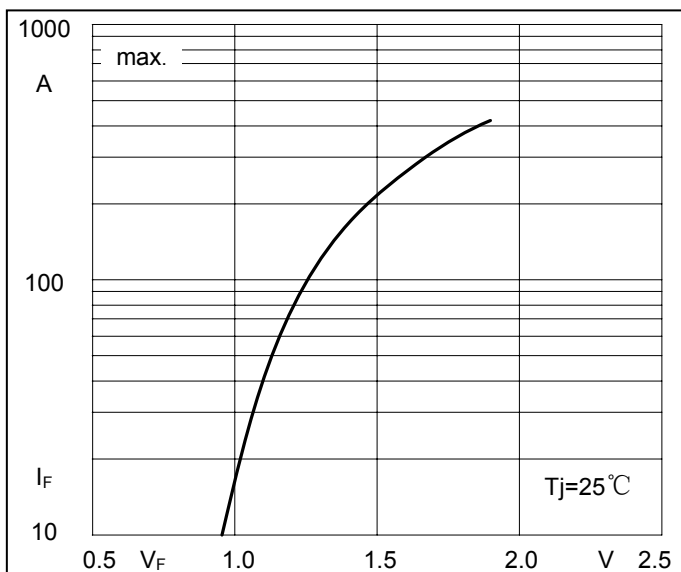


Fig5. Forward Characteristics

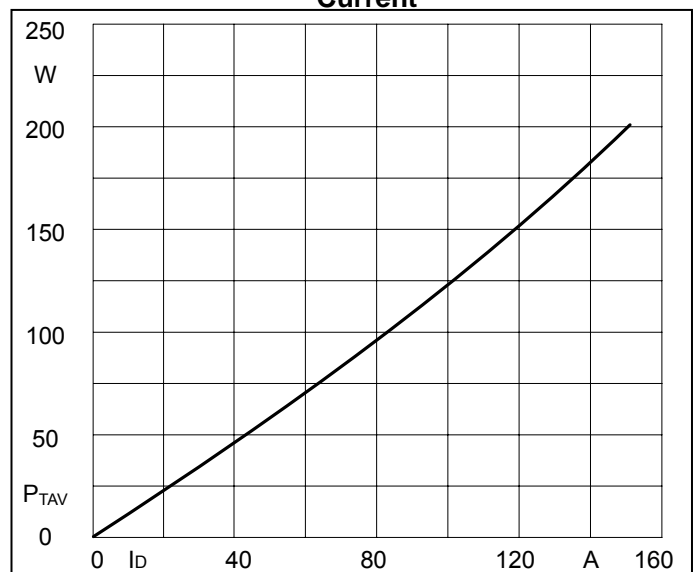


Fig6. SCR Power dissipation

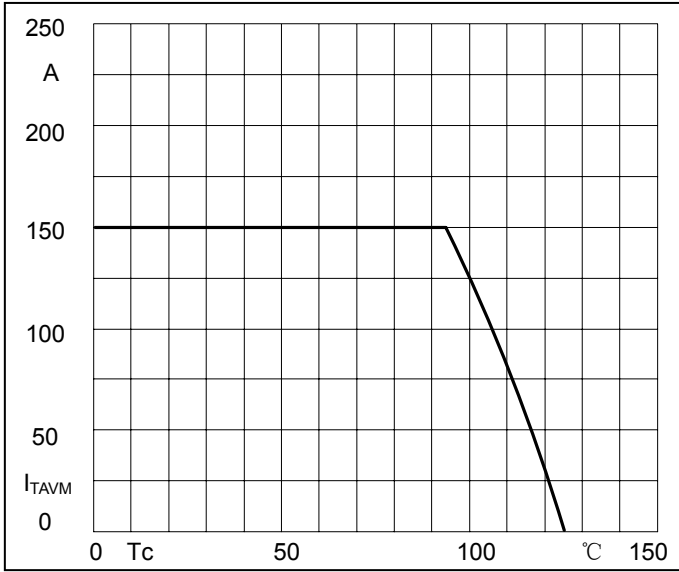


Fig7. SCR Forward Current Derating Curve

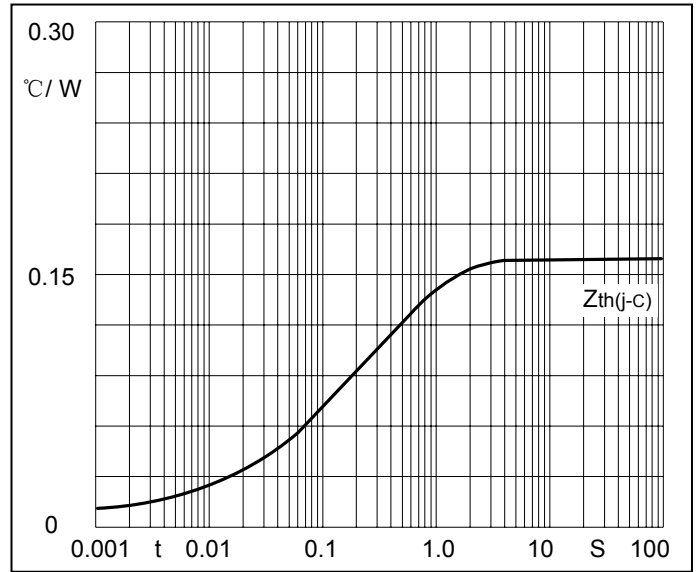


Fig8. SCR Transient thermal impedance

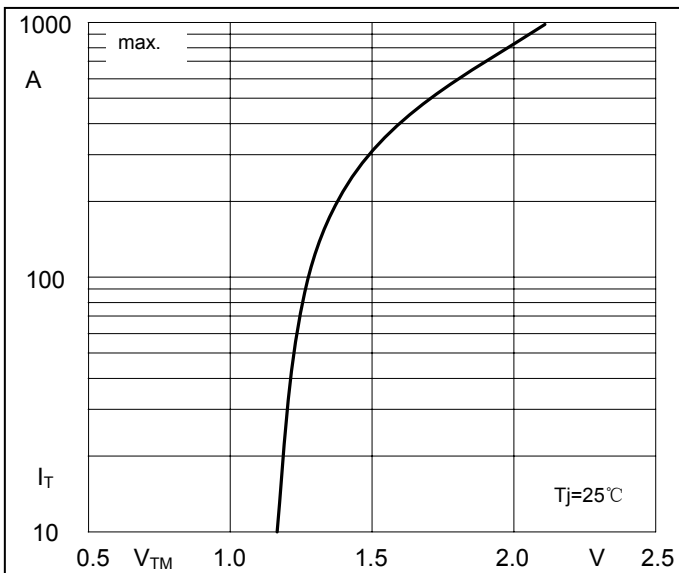


Fig9. SCR Forward Characteristics

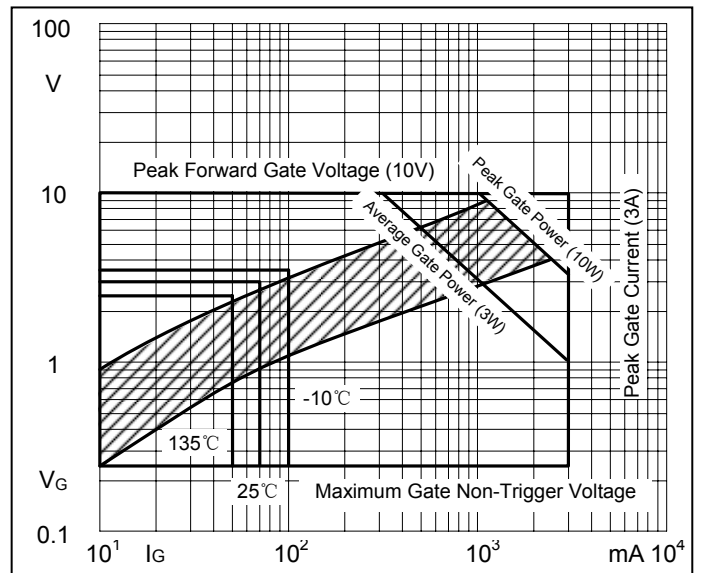


Fig10. Gate trigger Characteristics

Package Outline Information

