

FCD4N60

N-Channel SuperFET® MOSFET

600 V, 3.9 A, 1.2 Ω

Features

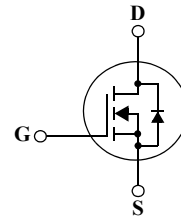
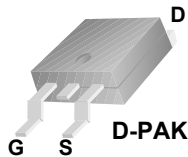
- 650V @T_J = 150°C
- Typ. R_{DS(on)} = 1.0 Ω
- Ultra Low Gate Charge (Typ. Q_g = 12.8 nC)
- Low Effective Output Capacitance (Typ. C_{oss,eff} = 32 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter	FCD4N60	Unit
V _{DSS}	Drain to Source Voltage	600	V
I _D	Drain Current	-Continuous (T _C = 25°C)	3.9
		-Continuous (T _C = 100°C)	2.5
I _{DM}	Drain Current	- Pulsed (Note 1)	11.7
V _{GSS}	Gate to Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	128	mJ
I _{AR}	Avalanche Current (Note 1)	3.9	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P _D	Power Dissipation	(T _C = 25°C)	50
		- Derate above 25°C	0.4
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCD4N60	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	2.5	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max	83	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD4N60	FCD4N60TM	D-PAK	380mm	16m	2500
FCD4N60	FCD4N60TF	D-PAK	380mm	16m	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.6	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 3.9\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	-	1.0	1.2	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.0\text{ A}$ (Note 4)	-	3.2	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	415	540	pF
C_{oss}	Output Capacitance		-	210	275	pF
C_{riss}	Reverse Transfer Capacitance		-	19.5	-	pF
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	12	16	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	32	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 3.9\text{ A}$ $R_G = 25\ \Omega$	-	16	45	ns
t_r	Turn-On Rise Time		-	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		-	36	85	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	-	30	70
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\text{ V}, I_D = 3.9\text{ A},$ $V_{GS} = 10\text{ V}$	-	12.8	16.6	nC
Q_{gs}	Gate to Source Gate Charge		-	2.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4, 5)	-	7.1	-

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	3.9	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	11.7	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	277	-	ns
Q_{rr}	Reverse Recovery Charge		(Note 4)	-	2.07	-

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 1.9\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega, \text{Starting } T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3.9\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

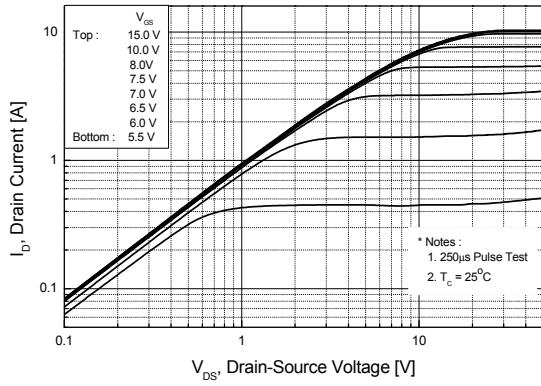


Figure 2. Transfer Characteristics

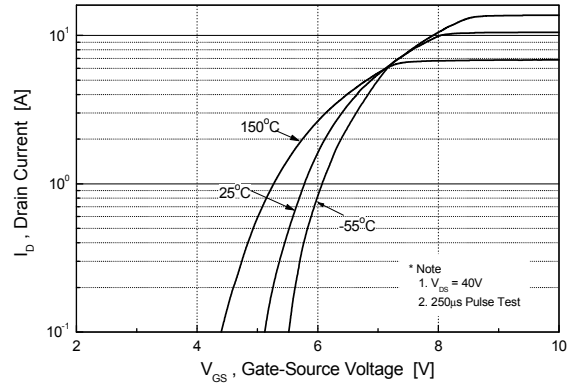


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

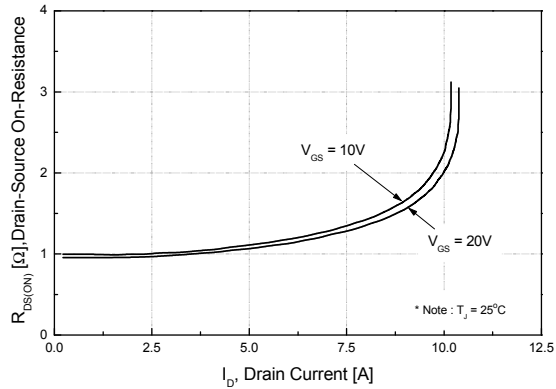


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

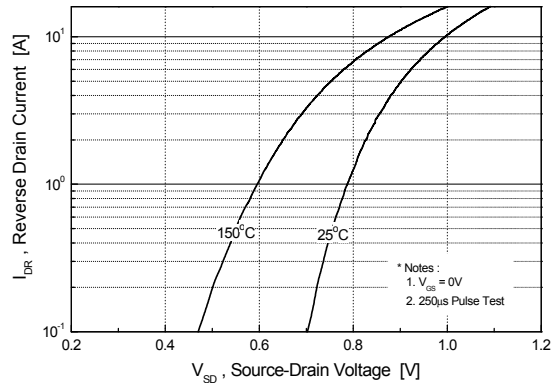


Figure 5. Capacitance Characteristics

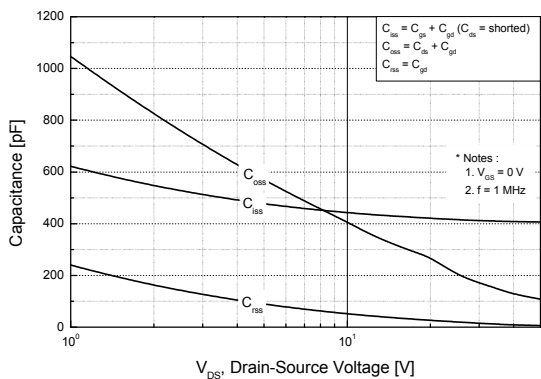
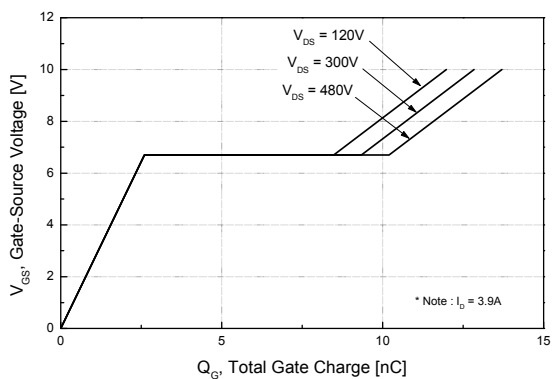


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

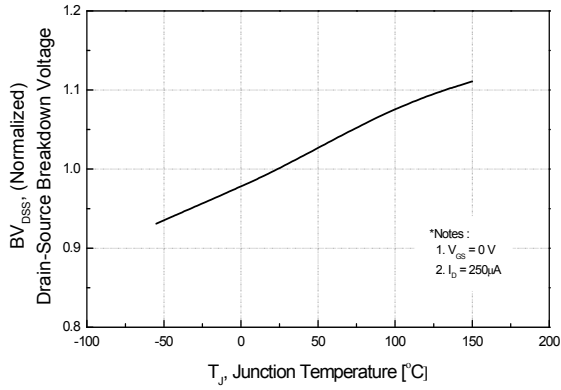


Figure 8. On-Resistance Variation vs. Temperature

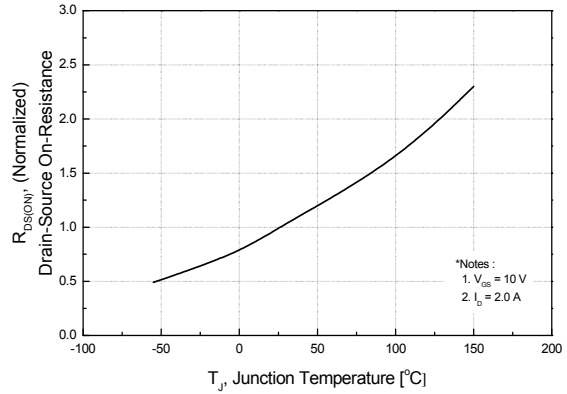


Figure 9. Maximum Safe Operating Area

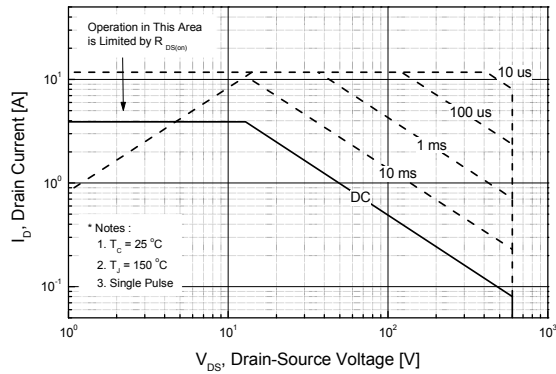


Figure 10. Maximum Drain Current vs. Case Temperature

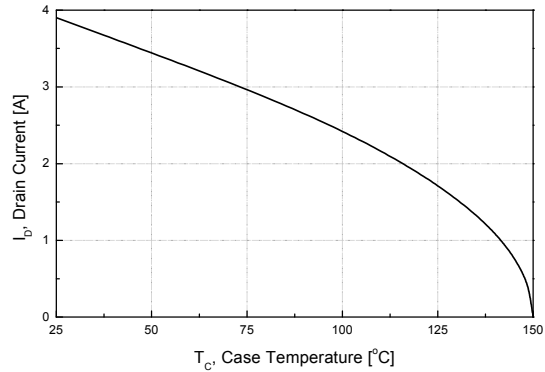
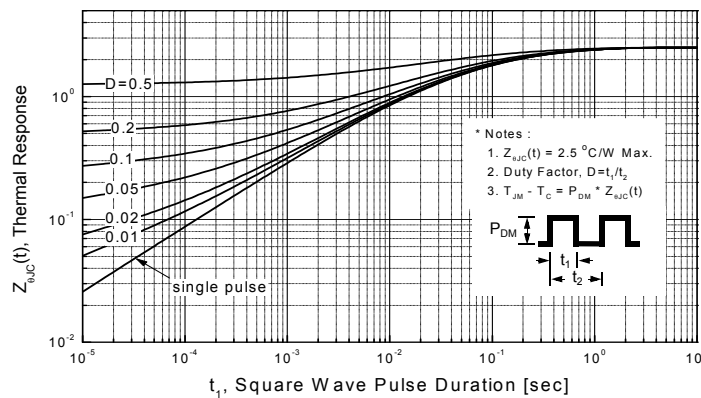
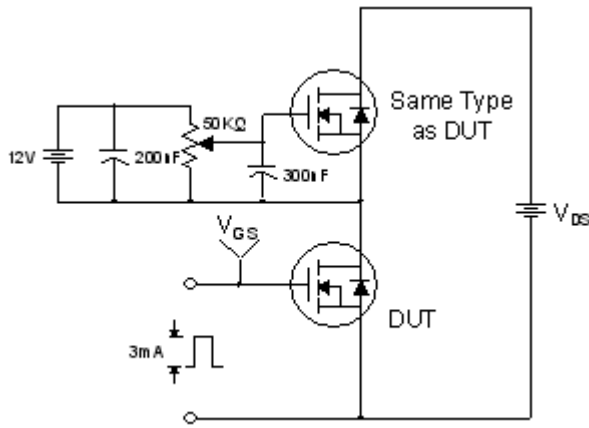


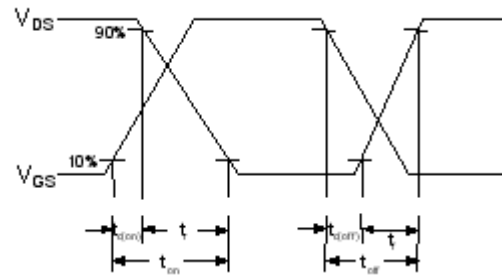
Figure 11-1. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



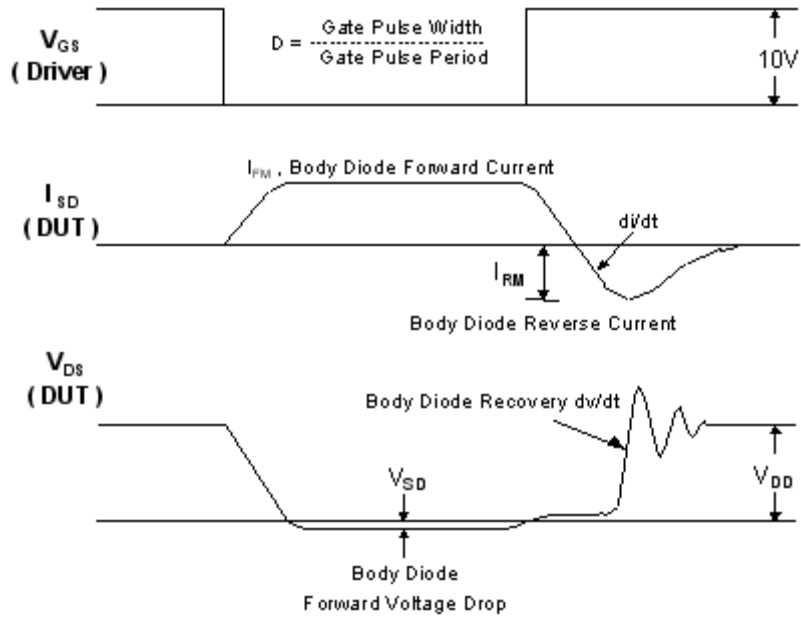
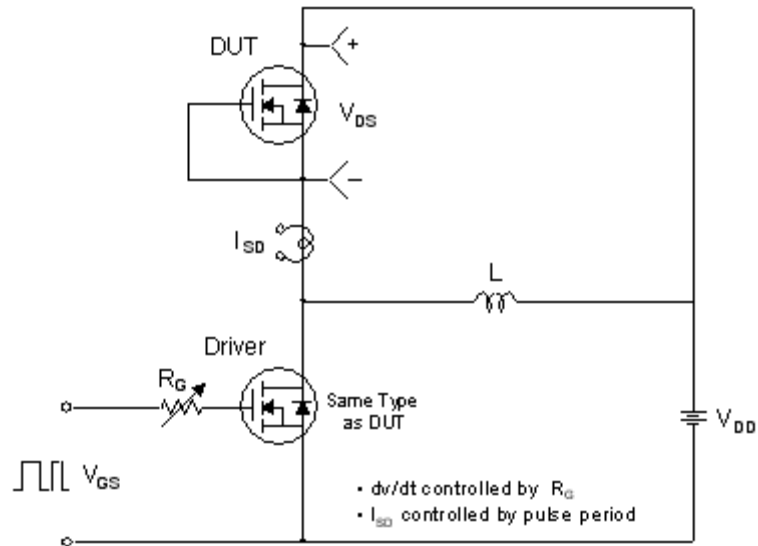
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

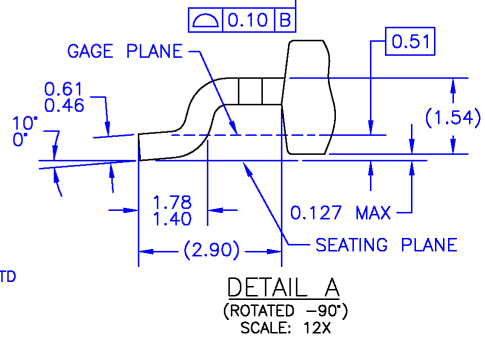
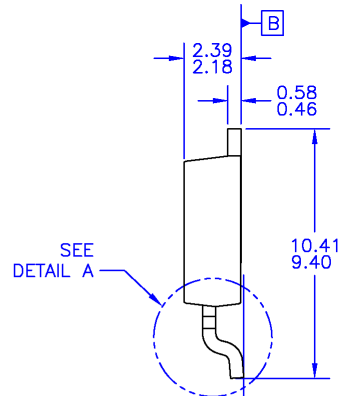
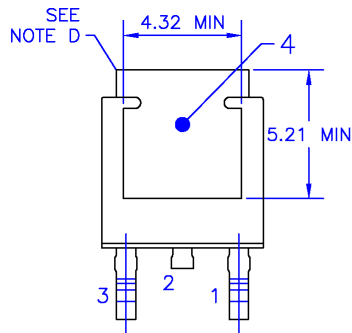
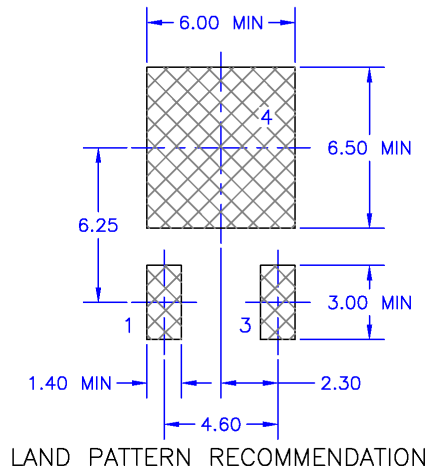
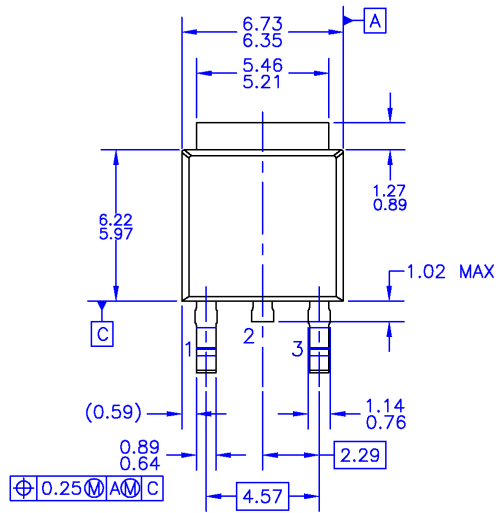


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D-PAK




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters



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| AccuPower™ | F-PFST™ | PowerXS™ | SYSTEM GENERAL®* |
| AX-CAP®* | FRFET® | Programmable Active Droop™ | TinyBoost™ |
| BitSiC™ | Global Power Resource™ | QFET® | TinyBuck™ |
| Build it Now™ | Green Bridge™ | QS™ | TinyCalc™ |
| CorePLUS™ | Green FPS™ | Quiet Series™ | TinyLogic® |
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Datasheet Identification	Product Status	Definition
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