

DF6F6.8MCTC

1. Applications

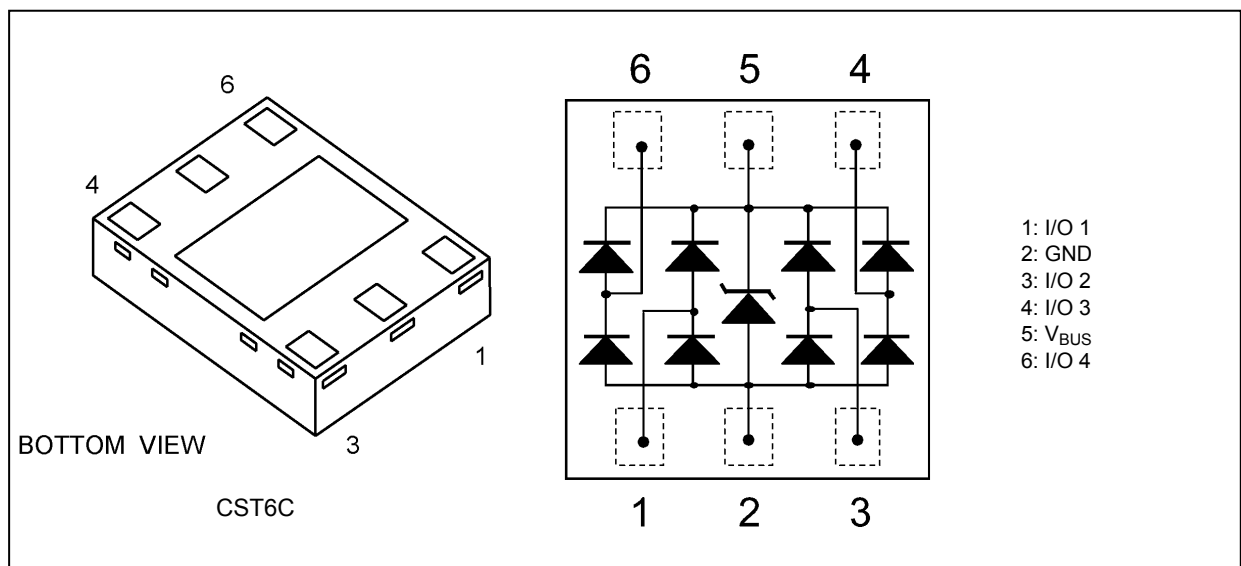
- ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

2. Features

- (1) ESD protection for up to 4 high-speed data lines and 1 Bus line.
- (2) Ultra compact packaging for easy configuration in any ESD protection circuits.
- (3) Low Input/output-to-ground capacitance: $C_{T-GND}(1) = 0.6 \text{ pF (typ.)}$.

3. Packaging and Internal Circuit Pin Assignment



4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Note	Rating	Unit
Junction temperature	T _j		150	°C
Storage temperature	T _{stg}		-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Electrical Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}		—	—	—	5.0	V
Reverse breakdown voltage	$V_{BR(1)}$		$I_R = 5\text{ mA}$ (Between I/O - GND pins)	6.0	—	—	
	$V_{BR(2)}$		$I_R = 5\text{ mA}$ (Between V_{BUS} - GND pin)	6.8	—	—	
Reverse current	$I_R(1)$		$V_{RWM} = 5\text{ V}$ (Between I/O - GND pins)	—	—	0.5	μA
	$I_R(2)$		$V_{RWM} = 5\text{ V}$ (Between V_{BUS} - GND pin)	—	—	0.5	
Input/output-to-ground capacitance	$C_{t-GND(1)}$	Note 1	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (Between I/O - GND pins)	—	0.6	1.0	pF
	$C_{t-GND(2)}$		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (Between V_{BUS} - GND pin)	—	67	—	
Input/output-to-ground capacitance difference	ΔC_{t-GND}		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (Between I/O - GND pins)	—	0.01	—	
Total capacitance	C_t		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (Between I/O - I/O pins)	—	0.3	—	

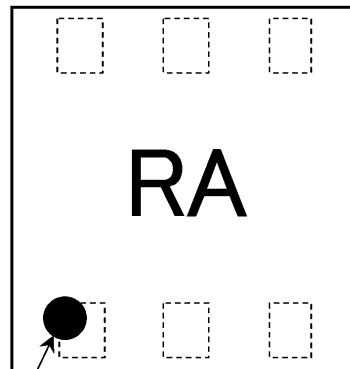
Note1: Guaranteed by design.

6. Guaranteed ESD Protection (Note)

Test Condition	ESD Protection
IEC61000-4-2 (Contact discharge)	$\pm 8\text{ kV}$

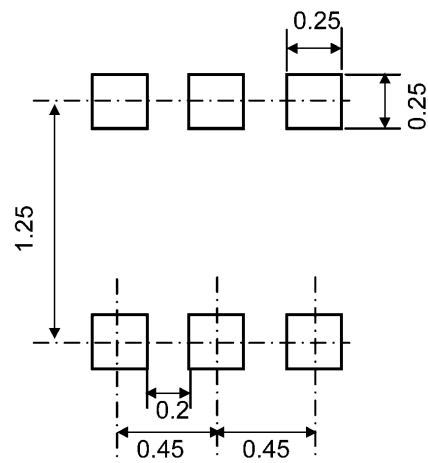
Note: Criterion: No damage to devices.

7. Marking



Pin #1 Mark
Fig. 7.1 Marking

Marking Code	Part Number
RA	DF6F6.8MCTC

8. Land Pattern Dimensions for Reference Only**Fig. 8.1 Land Pattern Dimensions for Reference Only (Unit: mm)**

9. Characteristics Curves (Note)

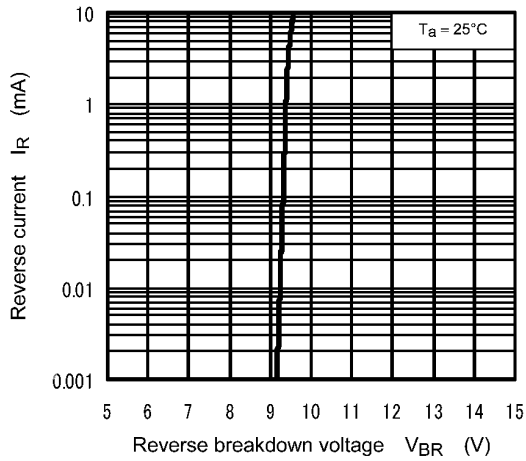


Fig. 9.1 $I_R - V_{BR}$
(Between I/O - GND pins)

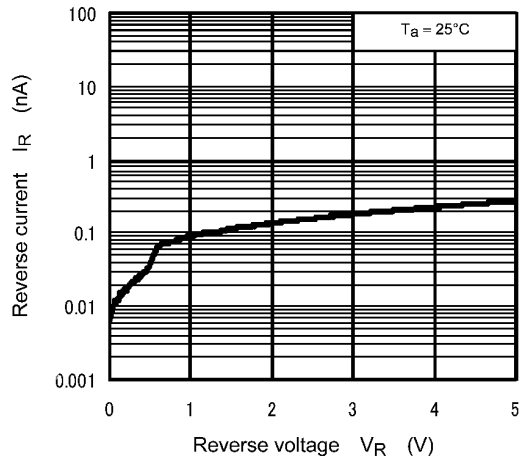


Fig. 9.2 $I_R - V_R$
(Between I/O - GND pins)

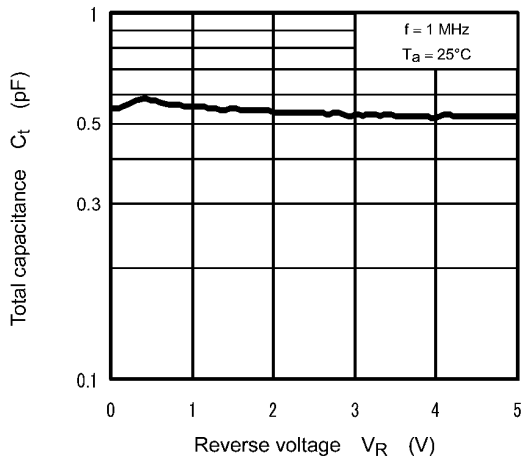


Fig. 9.3 $C_t - V_R$
(Between I/O - GND pins)

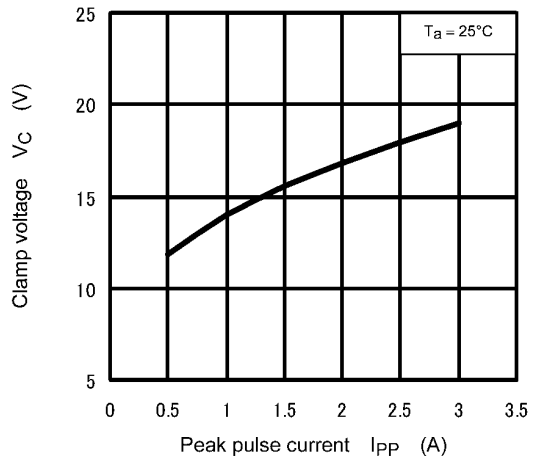
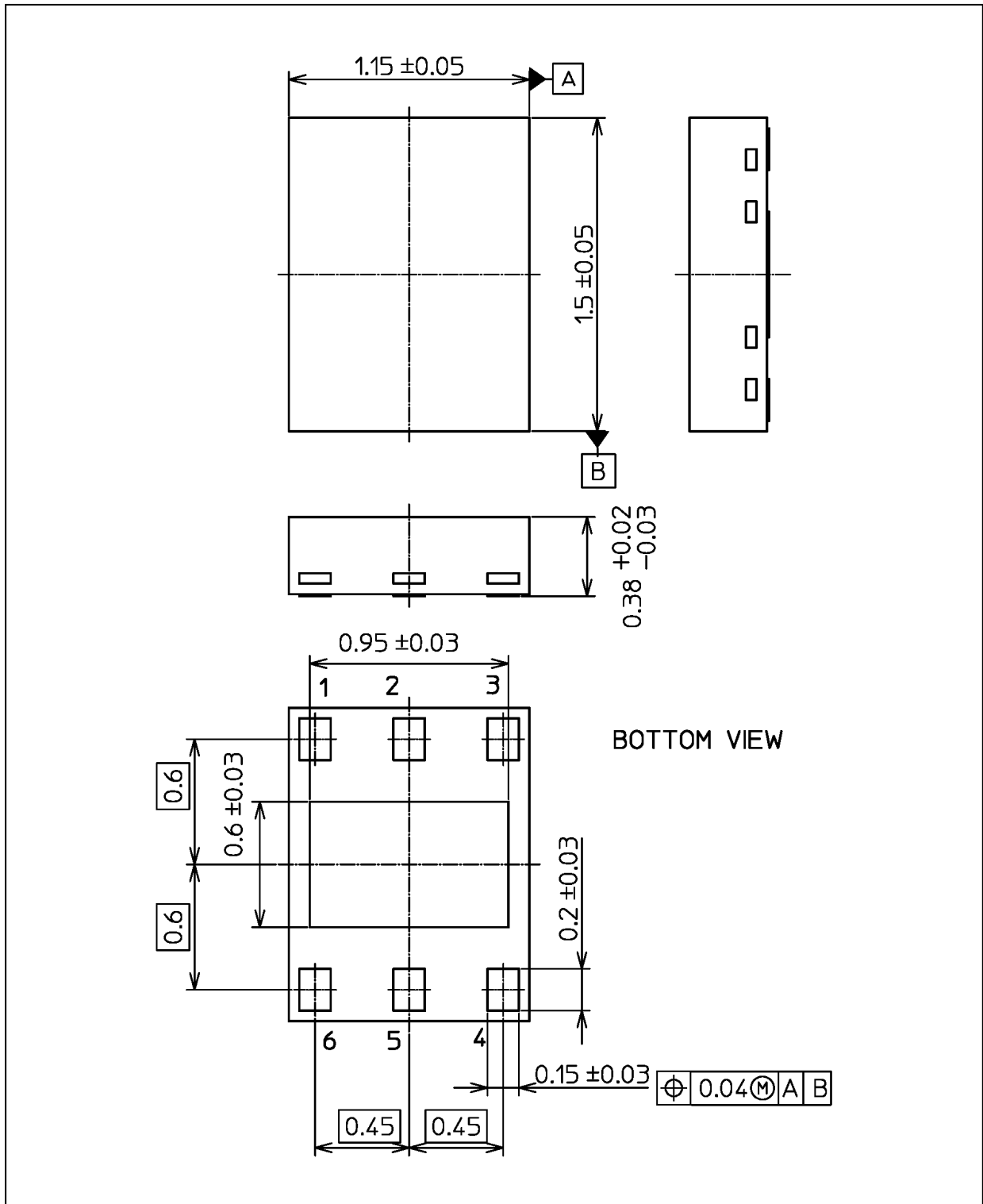


Fig. 9.4 $V_C - I_{PP}$
(Between I/O - GND pins)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 2.0 mg (typ.)

Package Name(s)
Nickname: CST6C

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