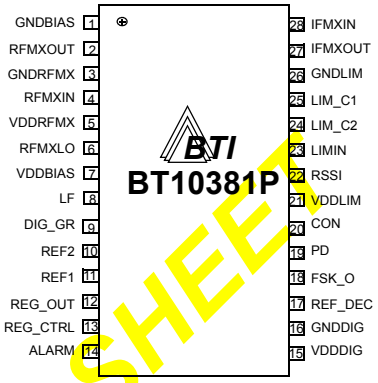
100 - 400MHz POCSAG PAGER RECEIVER IC

Features

- High Performance Integrated 100-400MHz Pager Receiver IC
- Low power consumption
- Wide operating frequency range
- Wide frequency offset and deviation range
- Fully POCSAG compatible Digital FSK receiver for 1200bps
- Power on/off mode selectivity
- High Sensitivity and Wide Dynamic range
- Ambient temperature range (-40°C to +85°C)
- 28 Pin TSSOP package



Applications

- Pager Receivers (POCSAG)
- Wireless Communication Products
- Telemetry Receivers

Description

The BT10381P is a fully integrated, high-performance, low-power, CMOS monolithic RF receiver designed specifically for wide area digital paging systems. The BT10381P employs a direct FM Non-Return-to-Zero (NRZ) Frequency Shift Keying (FSK) digital demodulation scheme. The receiver design is based on dual conversion of the input RF signal to the baseband signal by on-chip mixers. The BT10381P includes an on-chip RF Downconversion Mixer, IF Downconversion Mixer, Limiter/RSSI block, Digital FSK Demodulator, FSK Reference PLL, a low battery indicator, and an on-chip +1V Regulator. The BT10381P requires a DC supply voltage of +2.7V.

Ordering Information

BT10381P POCSAG Pager Receiver IC

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Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	Ta=25°C	2.4	2.7	3.0	V
Supply Current	@ 2.7V Power Supply		1.69		mA
Stand-by current				<200	µA

Parameters	Min	Typ	Max	Unit
RF Downconversion Mixer				
Input RF Frequency	100	280	400	MHz
Output IF Frequency		21.4		MHz
Gain		8.5		dB
Input IP3		-14.5		dBm
1dB compression point		-29		dBm
Noise figure		15.9		dB
Input impedance		150		Ω
Output impedance		1.5		kΩ
IF Downconversion Mixer				
Input frequency		21.4		MHz
Output frequency		454.4		kHz
Gain		27.7		dB
Input IP3		-36		dBm
1dB compression point		-51.5		dBm
RSSI				
Dynamic Range		50		dB
2-Level Digital FSK Demodulator				
Output		1		bit
PLL Charge Pump output current		210		uA
Regulator				
Regulator output voltage	0.92	0.99	1.01	V

Pin Table

Pin #	Parameter	I/O	Description
Power and Ground Pins			
3	GNDRFMX	-	Ground to RF Mixer
1	GNDBIAS	-	Ground to PTAT bias
26	GNDLIM	-	Ground to Limiter/RSSI block
16	GNDDIG	-	Ground to Digital blocks
9	DIG_GR	-	Ground to Digital Guard Ring
5	VDDRFMX		Power supply to RF Mixer
21	VDDLIM	-	Power supply to Limiter/RSSI block
7	VDDBIAS	-	Power supply to PTAT bias

15	VDDDIG	-	Power supply to Digital blocks
Receiver Pins			
4	RFMXIN	I	Input to the RF mixer
6	RFMXLO	I	VCO clock input for the RF mixer
2	RFMXOUT	O	RF Mixer Output signal
28	IFMXIN	I	Input to the IF mixer
27	IFMXOUT	O	Output of the IF mixer
23	LIMIN	I	Input to the Limiter
25 / 24	LIM_C1 / LIM_C2	I	External tuning capacitors for the Limiter
22	RSSI	O	RSSI output to the MPU
Digital FSK Demodulator Pins			
18	FSK_O	O	Digital FSK Demodulator Output pin to the Decoder
17	REF_DEC	I	FSK Reference Clock signal from the Decoder
20	CON	I	FSK Control signal from the Decoder
10 / 11	REF2 / REF1	I	XTAL Reference Frequency Input pins
8	LF	O	Output of the Charge Pump to the External Loop Filter
Power Control & Voltage Regulator Pins			
19	PD	I	Power down/Battery Save pin
13	REG_CRTL	I	Voltage Regulator Control
12	REG_OUT	O	+1V Regulator Output
14	ALARM	O	Low Battery Alarm

Detailed Pin Descriptions

RECEIVER PINS:

RFMXIN (Pin *4*)
Input to the RF Mixer
Input to the RF Downconversion Mixer from the external RF SAW filter. This pin should be matched with the output impedance requirement of the RF SAW filter (150W). It is necessary to have a tau matching scheme for this pin to provide a ground path for one side of the internal single-to-differential scheme (*see Application Circuit*).

RFMXOUT (Pin *2*)
IF Output signal of the RF Mixer
Single-ended output of the RF Downconversion Mixer which interfaces with the external 21.4MHz XTAL filter. Matching is required between this pin and the 21.4MHz XTAL filter's input impedance of 1.5kW.

RFMXLO (Pin *6*)
VCO/Clock Input to the RF Mixer
This pin provides the clock input to the RF Downconversion Mixer from the external RF VCO. This pin has a high input impedance. Matching is optional but recommended.

VDDRFMX (Pin *5*) and GNDRFMX (Pin *3*)
RF Mixer Power Supply and Ground
VDDRFMX and GNDRFMX are the +2.7V power supply and ground for the RF Mixer block.

IFMXIN (Pin *28*)
Input to the IF Mixer
This pin is the input to the IF Downconversion Mixer from the external 21.4MHz XTAL filter. This pin should be matched with the 1.5kW output impedance of the 21.4MHz XTAL filter.

IFMXOUT (Pin *27*)
Output from the IF Mixer
Output from the IF Downconversion Mixer which presents a nominal 1.5kW output resistance and interfaces directly to the external 455kHz bandpass filter.

VDDBIAS (Pin *7*) and GNDBIAS (Pin 1)
PTAT Bias Power Supply and Ground
VDDBIAS and GNDBIAS are the +2.7V power supply and ground for the PTAT Bias block.

LIMIN (Pin *23*)
Input to the Limiter
Input to the Limiter block from the external 455kHz bandpass filter. This pin is matched with the 1.5kW output impedance of the 455kHz bandpass filter.

LIM_C1/LIM_C2 (Pins *25 and 24*)
External Tuning capacitors for the Limiter
External capacitors connect these pins to ground to tune the on-chip Limiter feedback.

RSSI (Pin *22*)
RSSI Output to the Decoder
A resistor to ground is connected to this pin to output a DC voltage level signal that is proportional to the received signal strength. The output range of the RSSI is 0.5V to 2.5V and increases with increasing signal strength (*see Application Information for more details*).

VDDLIM (Pin *21*) and GNDLIM (Pin *26*)
Limiter/RSSI block Power Supply and Ground
VDDLIM and GNDLIM are the +2.7V power supply and ground for the Limiter/RSSI block.

FSK DEMODULATOR PINS:

FSK_O (Pin *18*)
Digital FSK Digital Demodulator Output to the Decoder
Output pin of the FSK Digital Demodulator which detects the 2 input tones. This pin directly connects to a POCSAG Decoder chip.

REF_DEC (Pin *17*)
FSK Reference Clock signal from the Decoder
This pin receives the clock signal for the 2-Level FSK digital demodulator from a POCSAG Decoder chip. The clock synchronizes the output signal at FSK_O with the off-chip POCSAG Decoder chip.

CON (Pin *20*)
FSK Control signal from the Decoder
This pin receives the Control signal from a POCSAG Decoder chip for the FSK Demodulator. Depending on the signals at CON, the BT10381P will be in one of 2 modes: Acquisition or Hold mode.

REF1 / REF2 (Pins *11 and 10*)
PLL Reference Frequency Input
REF1 and REF2 connect to an external 20.945MHz crystal. These pins provide the clock signals for the IFMx and FSK sections of the BT10381P.

LF (Pin *8*)
Loop Filter Output
This pin provides the PLL/Charge Pump output signal required for the external Loop Filter. An RC network from this pin to ground is used to establish the PLL bandwidth.

VDDDIG (Pin *15*) and GNDDIG (Pin *16*)
Digital block Power Supply and Ground
VDDDIG and GNDDIG are the +2.7V power supply and ground for the FSK and internal PLL sections.

POWER SAVING PINS:

PD (Pin *19*)
Power Down pin
This pin controls the power down function of the BT10381P. A HIGH signal turns the circuit *on* while a LOW signal turns the circuit *off*.

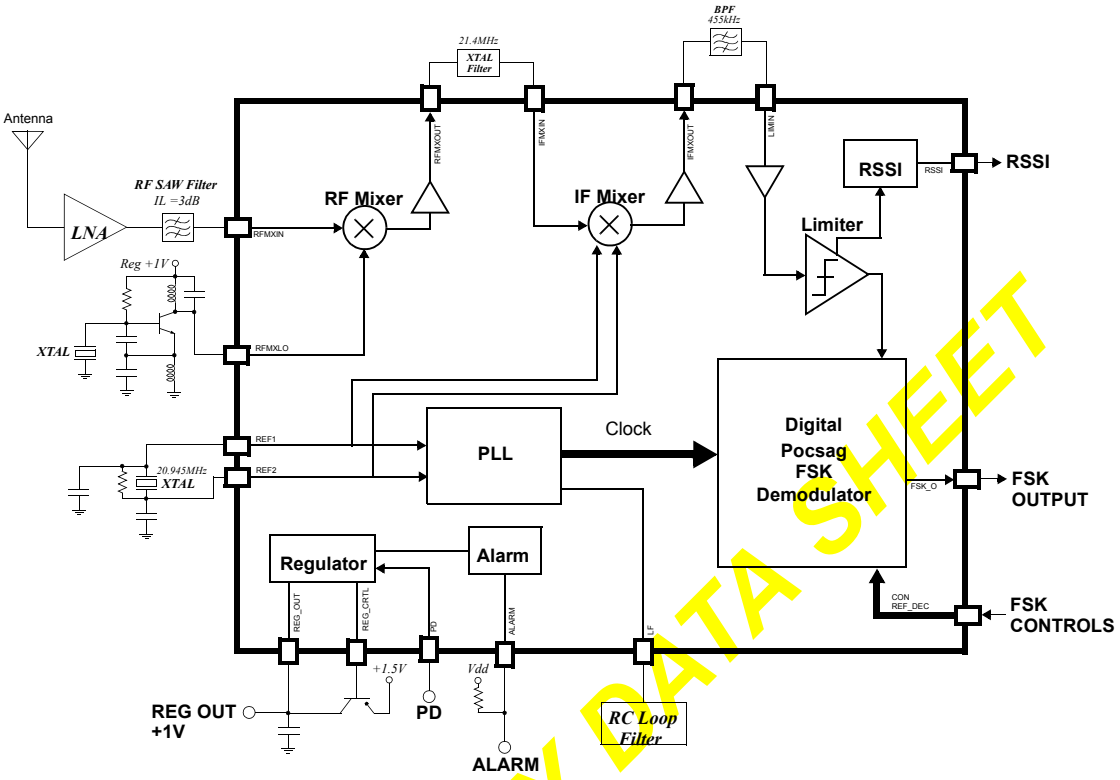
REG_OUT (Pin *12*)
Output of on-chip regulator
This is the output feedback pin for the on-chip +1V regulator. This must be connected to an external PNP pass transistor as shown in the APPLICATION CIRCUIT.

ALARM (Pin *14*)
Low Battery Alarm
Indicator for a +1.1V low battery signal. This output becomes HIGH to indicate deterioration of the battery. A pull-up resistor must be connected to this pin because it is an open-collector output.

REG_CRTL (Pin *13*)
Control of on-chip regulator
External transistor control terminal for the regulator. Connect an external PNP pass transistor to this terminal as shown in the APPLICATION CIRCUIT.

DIG_GR (Pin *9*)
Ground for the Digital Guard Ring
DIG_GR is the ground pin for the Digital Guard Ring.

Block Diagram



Application Information

The BT10381P has all of the required blocks to build an integrated Pager RF Front-end receiver. The BT10381P can be used over a wide frequency range of 120MHz to 300MHz, but it is optimized to work in the 278MHz - 282MHz range.

RF Mixer Block

The BT10381P RF Mixer is driven by the off-chip VCO to downconvert the RF frequency to the 21.4MHz IF frequency. The output of the mixer drives the 1.5kW input impedance of a 21.4MHz off-chip XTAL filter.

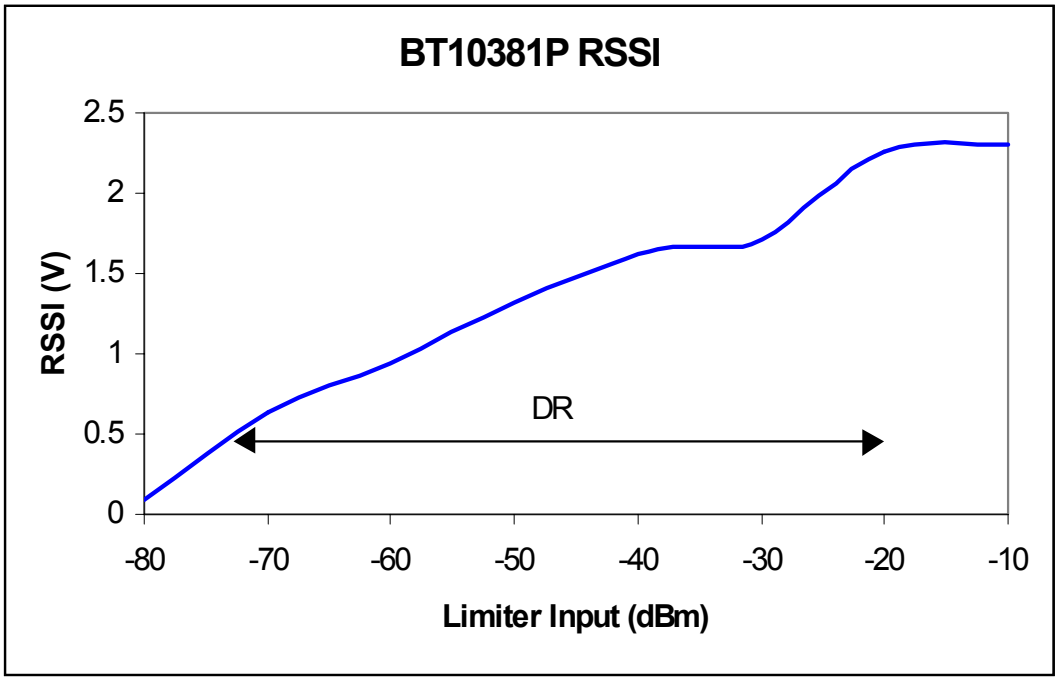
IF Mixer Block

The IF Mixer of the BT10381P downconverts the 21.4MHz IF frequency to 455kHz and requires an external 20.945MHz XTAL for its clock signals.

An external 455kHz bandpass filter is used after the IF Mixer to further suppress the image and improve the linearity of the downconverted IF signal.

Limiter/RSSI Block

The Limiter/RSSI block of the BT10381P is used to indicate the strength of the incoming (received) signal as well as to generate a hard limited output for the digital circuitry in the Digital Demodulator. The RSSI circuit has a DC level output with a 50dB dynamic range (*see graph*).



FSK Block

The FSK Digital Demodulator receives the input signal from the Limiter stage and the clock signal from the external 20.945MHz XTAL to generate the 1-bit data output required by an external POCSAG Decoder.

To guarantee proper operation of the FSK Digital Demodulator, the toleration frequency, f_T, must not exceed the greatest frequency deviation (Dfmax, which is 4.5 kHz) from the nominal frequency. The toleration frequency is calculated with the following equation:

$$RFfreq * Xtaltolerance = f_T < \Delta fmax$$

where: *RFfreq* is the incoming RF signal to the RF mixer
Xtal tolerance is the sum of the crystal tolerances of the RFVCO XTAL, measured in PPM.

The off-chip reference crystal tolerances are the sum of all crystal tolerances, including the frequency stability of the reference temperature, temperature vs. frequency stability, and aging (all measured in PPM). The sum of these tolerances (for RFVCO XTAL) should not exceed ± 10 PPM. To achieve greater flexibility with the crystal tolerances, the frequency stability error about the reference temperature can be eliminated by manually tuning the crystal used for the RF mixer to its nominal frequency. Then the remaining tolerances must not exceed ± 10 PPM.

The FSK has an internal PLL which is used to provide a 454.4 kHz reference frequency for the Digital FSK to demodulate the incoming Limiter output signal. The 20.945 MHz off-chip crystal provides the reference frequency for the PLL. The on-chip PLL uses a voltage controlled ring oscillator and a fixed divider. An off-chip RC loop filter is converted to pin LF. Further, the 20.945MHz off-chip XTAL is recommended but not limited to ±10ppm to guarantee proper operation of the FSK.

The internal PLL locks to 454.4 kHz, which serves as a reference frequency for the Digital FSK to demodulate the incoming limiter output signal. The demodulated signals are detected and converted into a 1-bit digital output. The 1-bit digital output is given to the decoder via the pin FSK_O.

Pin CON is used to control the mode of the FSK. This signal comes from the external POCSAG decoder. Pin REF_DEC takes the decoder clock as an input. This clock is used to synchronize the FSK 1-Bit output data with the external POCSAG decoder clock.

The FSK can either be in tracking mode or hold mode. The mode is controled by pin CON. When CON = High, then the FSK is tracking. When CON = Low then it is in the hold mode.

The recommended usage of BT10381P is shown in *Figure 1*.

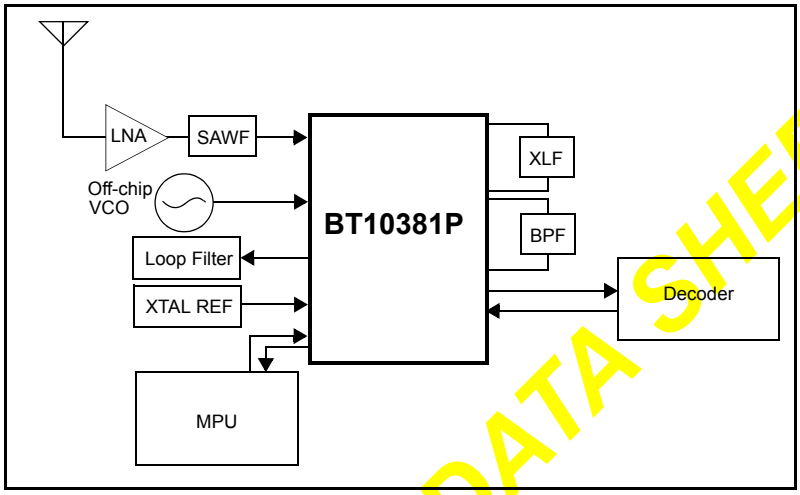
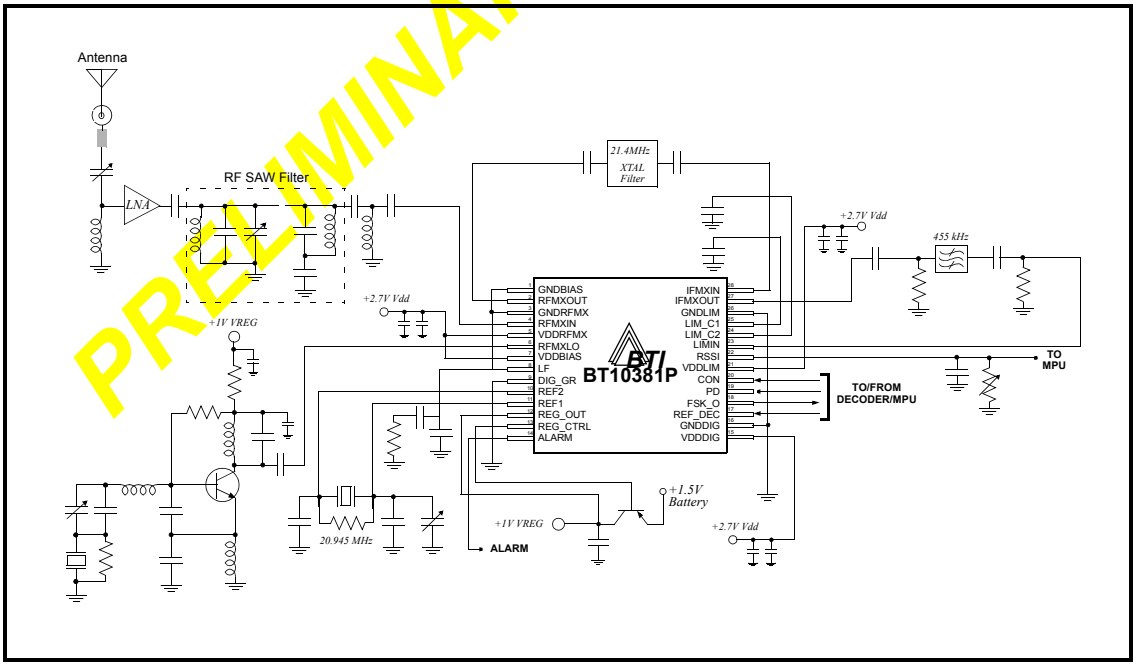
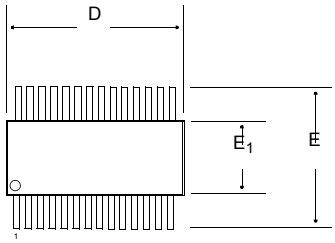


Figure 1. Recommended Usage of the BT10381P.

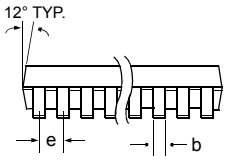
Application Circuit



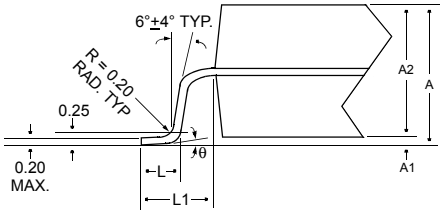
Package Dimensions



Top View



Side View



28L TSSOP Package

Lead Count		28L
Dimensions	**Tolerance**	
A	Max.	1.20
A1		0.05 Min/0.10 Max
A2	± 0.125	0.925
D	± 0.10	9.70
E	± 0.15	6.40
E1	± 0.10	4.40
L	+0.15/-0.10	0.60
L1	+0.15/-0.10	1.00
e	± 0.15	0.65
b		0.19 Min/0.30 Max
θ	± 4°	4°

Package dimensions in mm.

Appendix A: Reference Design System Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Radio Frequency Input					
RF input sensitivity	BER,3%;±4.5kHz (FSK); data rate 1200bits/s; SNR=4.5dB; NF=4.0dB T_{amb}=25°		-130		dBm
Adjacent channel selectivity	T_{amb} = 25°C T_{amb} = -10 to +70°C	60 60	65 -	- -	dB
IF filter channel imbalance		-	-	2	dB
Co-channel rejection	Fc ± 300Hz	-	4	6	dB
Spurious immunity		55			dB
Intermodulation immunity		55			dB
Blocking immunity	Δf > ±1MHz	75	82	-	dB
Deviation range (3dB degradation in sensitivity)		±TBD	±4.5	±TBD	kHz
Receiver turn-on time				5	ms