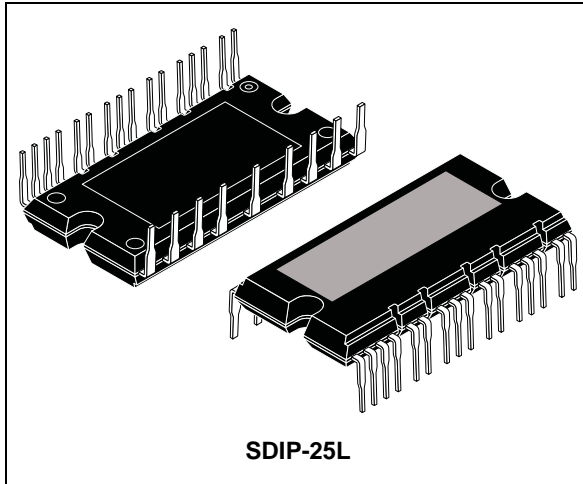


SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter - 14 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machines

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Features

- IPM 14 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shut down function
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 Vrms/min
- 4.7 kΩ NTC for temperature control
- UL recognized : UL1557 file E81734

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPS14K60T-H	GIPS14K60T-H	SDIP-25L	Tube

Contents

- 1 Internal block diagram and pin configuration 3**
- 2 Electrical ratings 5**
 - 2.1 Absolute maximum ratings 5
 - 2.2 Thermal data 6
- 3 Electrical characteristics 7**
 - 3.1 Control part 9
 - 3.1.1 NTC thermistor 11
 - 3.2 Waveforms definitions 12
- 4 Applications information 13**
 - 4.1 Recommendations 14
- 5 Package mechanical data 15**
- 6 Revision history 19**

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

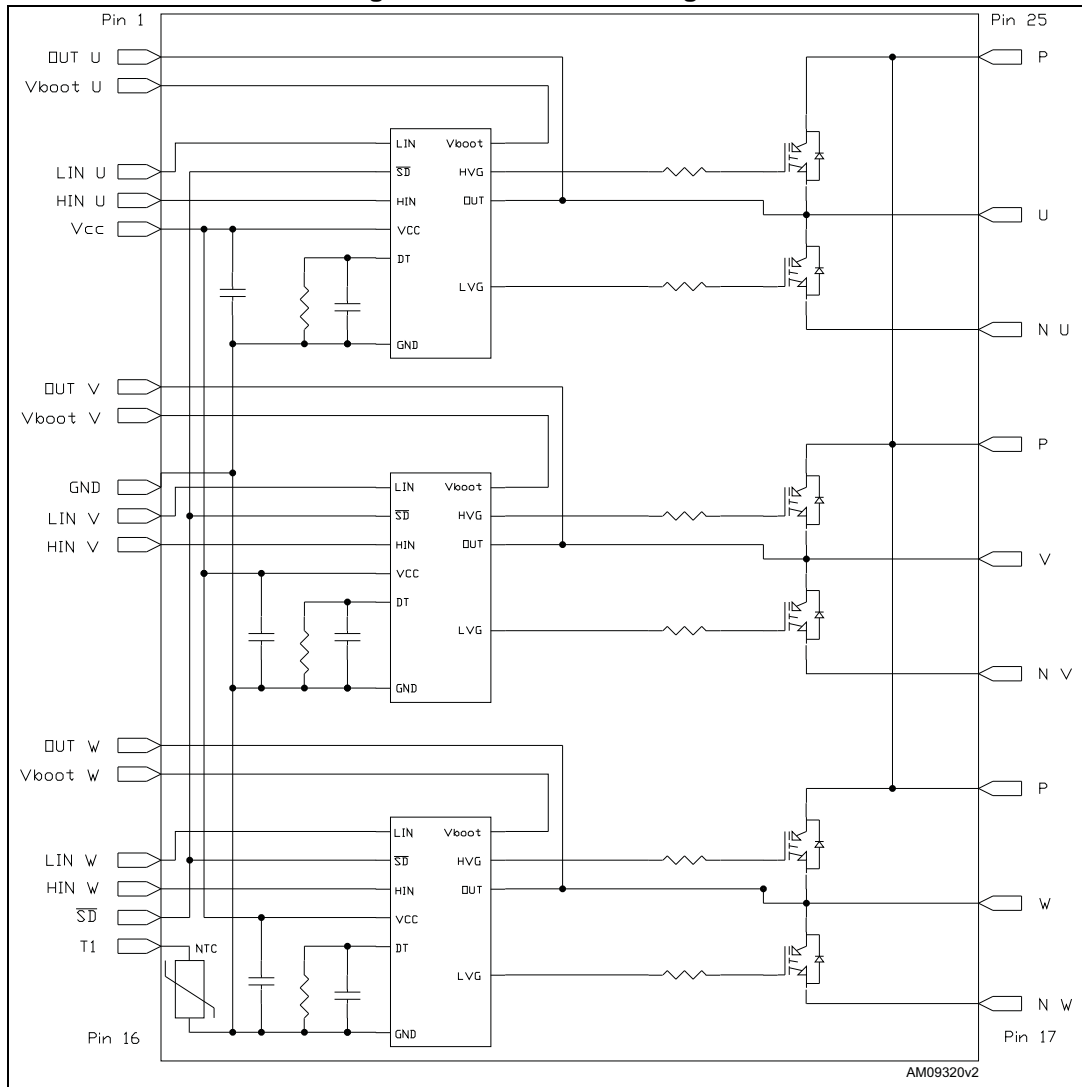
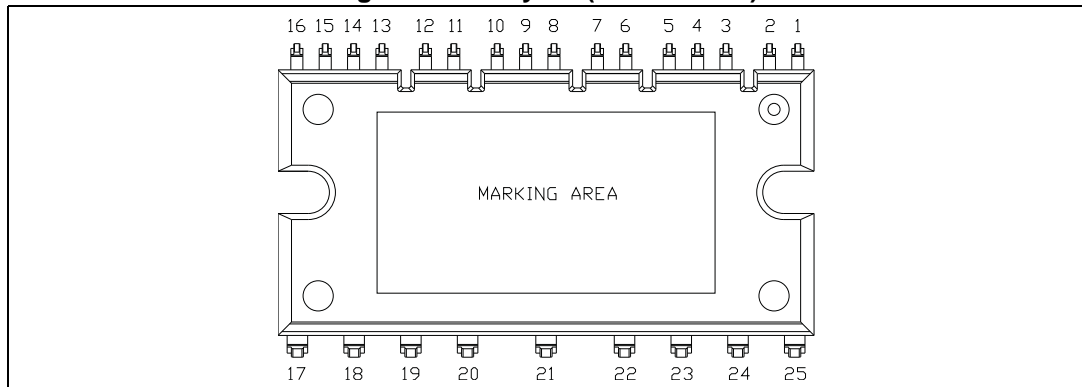


Table 2. Pin description

Pin n°	Symbol	Description
1	OUT _U	High side reference output for U phase
2	V _{boot U}	Bootstrap voltage for U phase
3	LIN _U	Low side logic input for U phase
4	HIN _U	High side logic input for U phase
5	V _{CC}	Low voltage power supply
6	OUT _V	High side reference output for V phase
7	V _{boot V}	Bootstrap voltage for V phase
8	GND	Ground
9	LIN _V	Low side logic input for V phase
10	HIN _V	High side logic input for V phase
11	OUT _W	High side reference output for W phase
12	V _{boot W}	Bootstrap voltage for W phase
13	LIN _W	Low side logic input for W phase
14	HIN _W	High side logic input for W phase
15	SD	Shut down logic input (active low)
16	T1	NTC thermistor terminal
17	N _W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N _V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N _U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U , N_V , N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U , N_V , N_W	500	V
V_{CES}	Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C^{(2)}$	Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$	14	A
$\pm I_{CP}^{(3)}$	Each IGBT pulsed collector current	30	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25^\circ\text{C}$	42	W
t_{scw}	Short-circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_j = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN(1)} = 5\text{ V}$	5	μs

1. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$.
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature.

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 21$	$V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied between HIN , LIN and GND	- 0.3	15	V
V_{SD}	Open drain voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$)	2500	V
T_C	Module case operation temperature	-40 to 125	$^\circ\text{C}$
T_J	Power chips operating junction temperature	-40 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT max.	3.0	°C/W
	Thermal resistance junction-case single diode max.	5.5	°C/W

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 5\text{ V}$, $I_C = 7\text{ A}$	-	2.1	2.5	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 5\text{ V}$, $I_C = 7\text{ A}$, $T_J = 125\text{ °C}$	-	1.8		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$ $V_{CC} = V_{boot} = 15\text{ V}$	-		150	μA
V_F	Diode forward voltage	($V_{IN}^{(1)} = 0$ "logic state"), $I_C = 7\text{ A}$	-		2.1	V
Inductive load switching time and energy						
t_{on}	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 7\text{ A}$ (see Figure 4)	-	270	-	ns
$t_{c(on)}$	Crossover time (on)		-	130	-	
t_{off}	Turn-off time		-	520	-	
$t_{c(off)}$	Crossover time (off)		-	140	-	
t_{rr}	Reverse recovery time		-	130	-	
E_{on}	Turn-on switching losses		-	150	-	μJ
E_{off}	Turn-off switching losses		-	110	-	

1. Applied between HIN_i , LIN_i and GND for $i = U, V, W$.

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

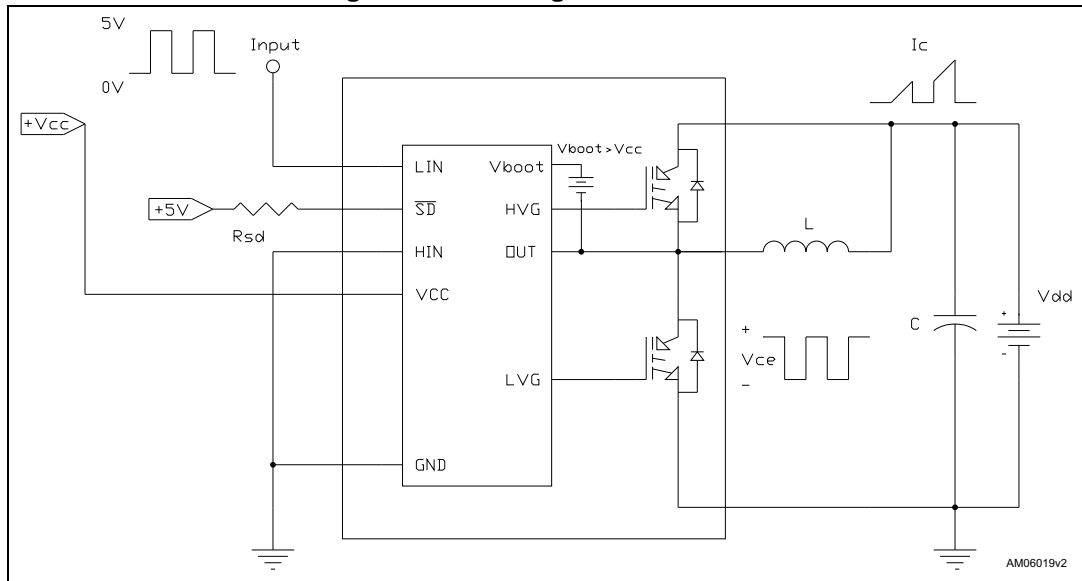
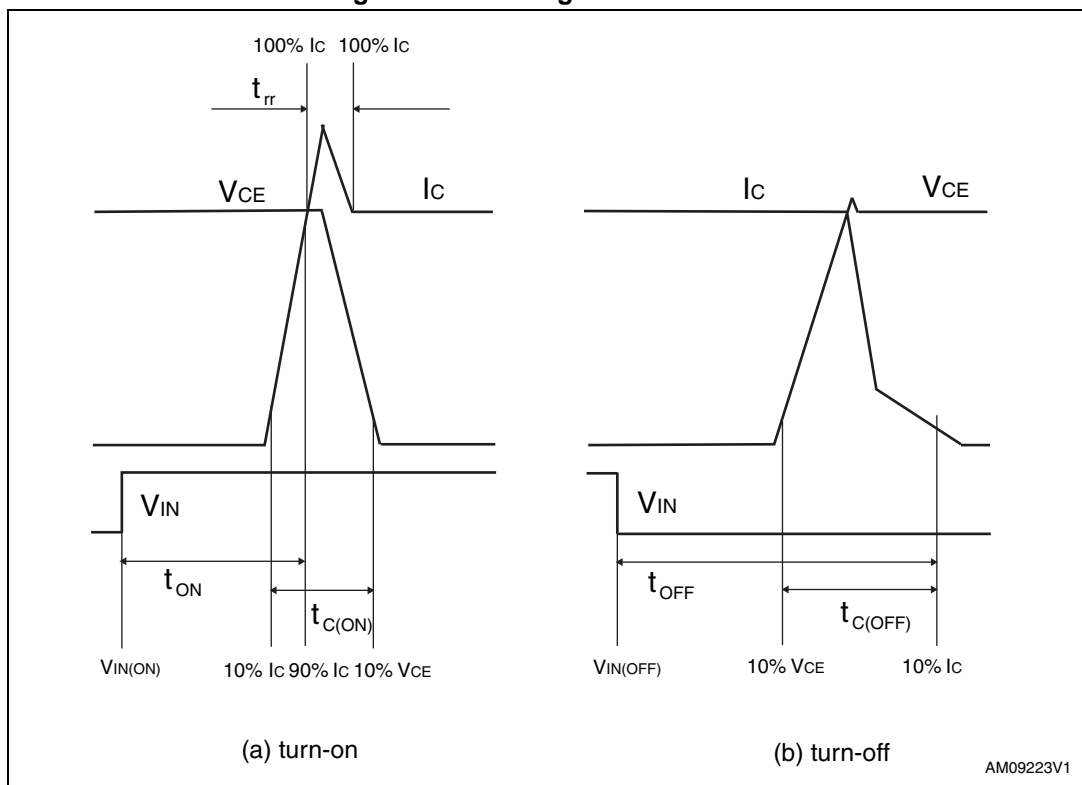


Figure 4. Switching time definition



Note: Figure 4 "Switching time definition" refers to HIN, LIN inputs (active high).

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ $\overline{SD} = 5\text{ V}$; LIN = 0 V; $H_{IN} = 0$			450	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; LIN = 0 V $H_{IN} = 0$			3.5	mA

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	$V_{BS} = 9\text{ V}$ $\overline{SD} = 5\text{ V}$; LIN = 0 $H_{IN} = 5\text{ V}$		70	110	μA
I_{QBS}	V_{BS} quiescent current	$V_{BS} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; LIN = 0 $H_{IN} = 5\text{ V}$		200	300	μA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage		0.8		1.1	V
V_{ih}	High logic level voltage		1.9		2.25	V
I_{HINh}	HIN logic "1" input bias current	HIN = 15 V	20	40	100	μA
I_{HINl}	HIN logic "0" input bias current	HIN = 0 V			1	μA
I_{LINh}	LIN logic "1" input bias current	LIN = 15 V	20	40	100	μA
I_{LINl}	LIN logic "0" input bias current	LIN = 0 V			1	μA
I_{SDh}	\overline{SD} logic "0" input bias current	$\overline{SD} = 15\text{ V}$	30	120	300	μA
I_{SDl}	\overline{SD} logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	μA
Dt	Dead time	see Figure 9		600		ns

Table 11. Shut down characteristics ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{sd}	Shut down to high / low side driver propagation delay	$V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0$ to 3.3 V	50	125	200	ns

Table 12. Truth table

Condition	Logic input (V_I)			Output	
	SD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1 "logic state" low side direct driving	H	H	L	H	L
1 "logic state" high side direct driving	H	L	H	L	H

Note: X: don't care

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching frequency ⁽¹⁾

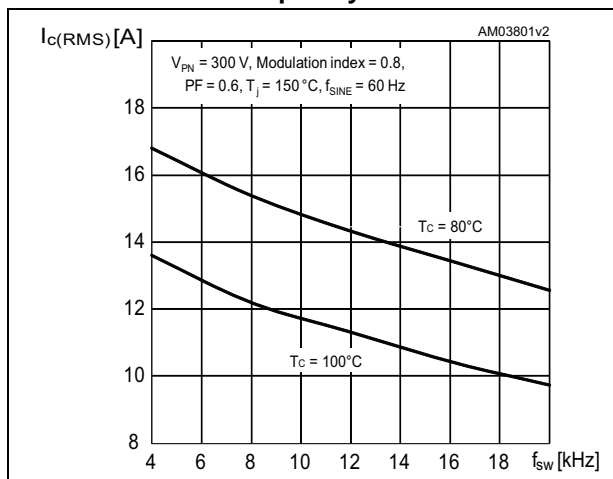
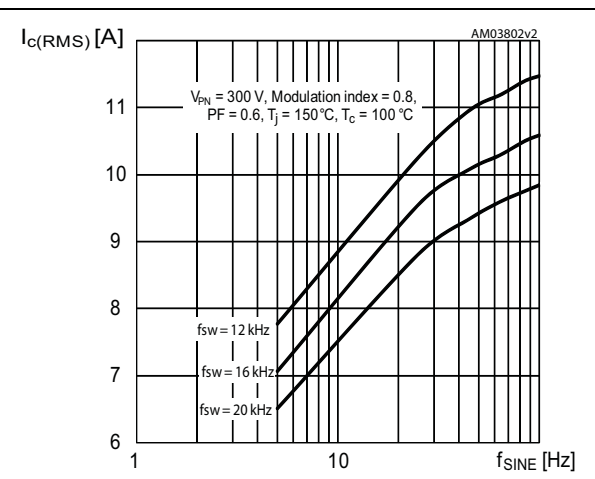


Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{SINE} ⁽¹⁾



1. Simulated curves refer to typical IGBT parameters and maximum R_{thJC} .



3.1.1 NTC thermistor

Table 13. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R ₂₅	Resistance	T = 25°C		4.7		kΩ
R ₁₂₅	Resistance	T = 125°C		160		Ω
B	B-constant	T = 25°C to 85°C		3950		K
T	Operating temperature		-40		150	°C

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B \left(\frac{1}{T} - \frac{1}{298} \right)}$$

Where T are temperatures in Kelvins

Figure 7. NTC resistance vs. temperature

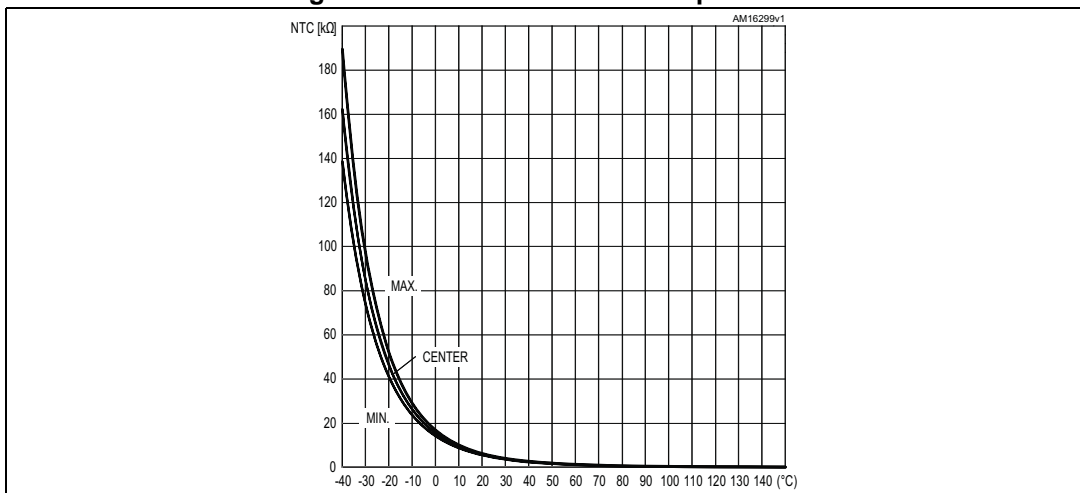
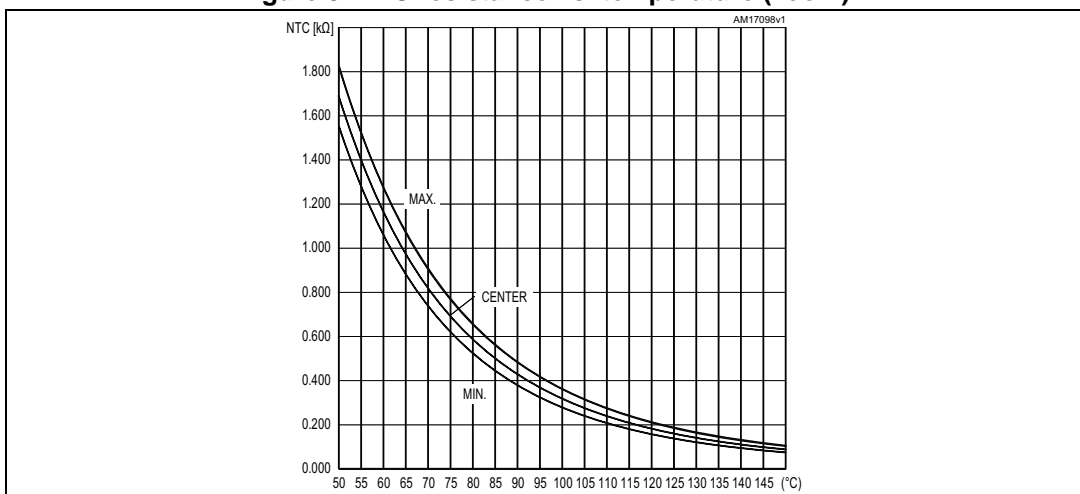
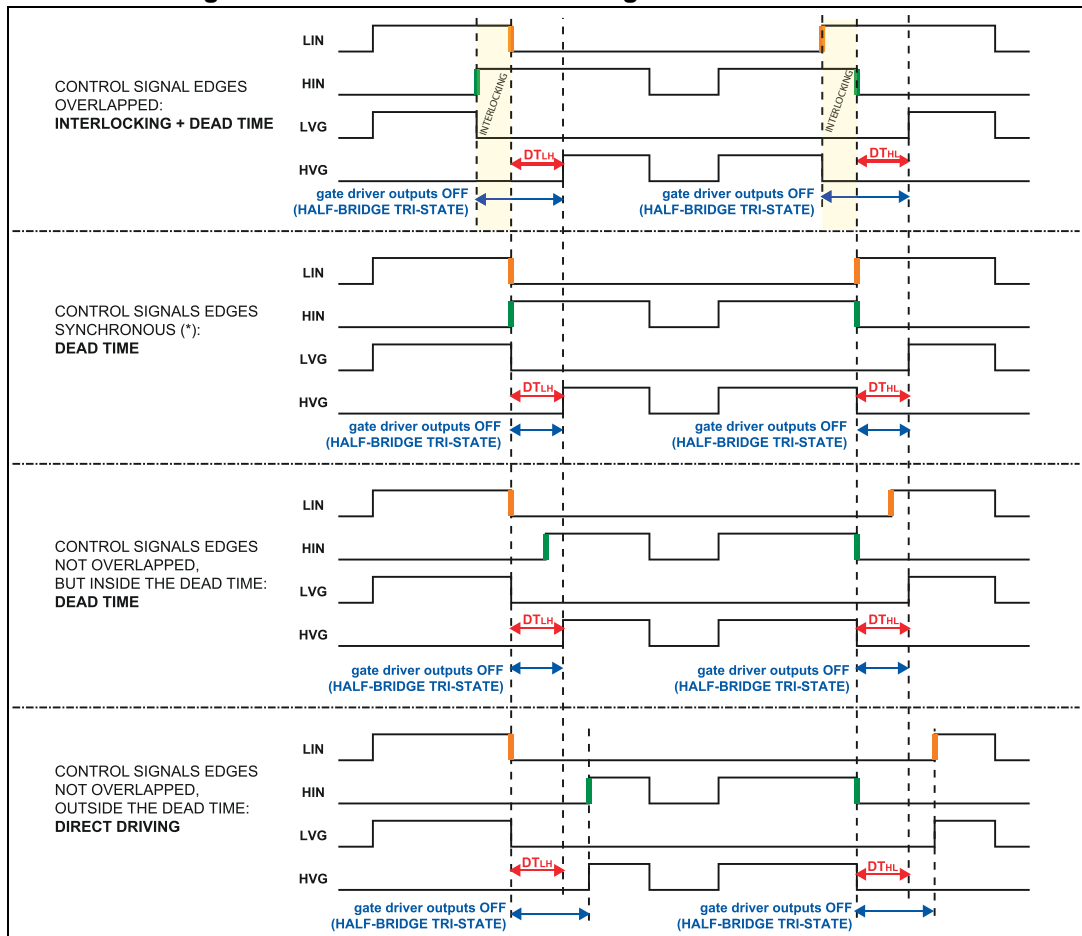


Figure 8. NTC resistance vs. temperature (zoom)



3.2 Waveforms definitions

Figure 9. Dead time and interlocking waveform definitions



4.1 Recommendations

- Input signals HIN, LIN are active high logic. A 375 kΩ (typ.) pull down resistor is built-in for each input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The \overline{SD} signal should be pulled up to 5 V / 3.3 V with an external resistor.

Table 14. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply voltage	Applied between P-Nu, Nv, Nw		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC} -GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi} - OUT_i for $i = U, V, W$	13		18	V
t_{dead}	Blanking time to prevent arm-short	For each input signal	1			μs
f_{PWM}	Pwm input signal	-40°C < T_c < 100°C -40°C < T_j < 125°C			20	kHz
T_c	Case operation temperature				100	°C

For further details refer to AN3338.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 15. SDIP-25L mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.83	25.23	25.63
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	6.30	6.50	6.70
D		33.30	
D1		5.55	
E		11.20	
E1		1.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

Figure 11. SDIP-25L drawing dimensions data

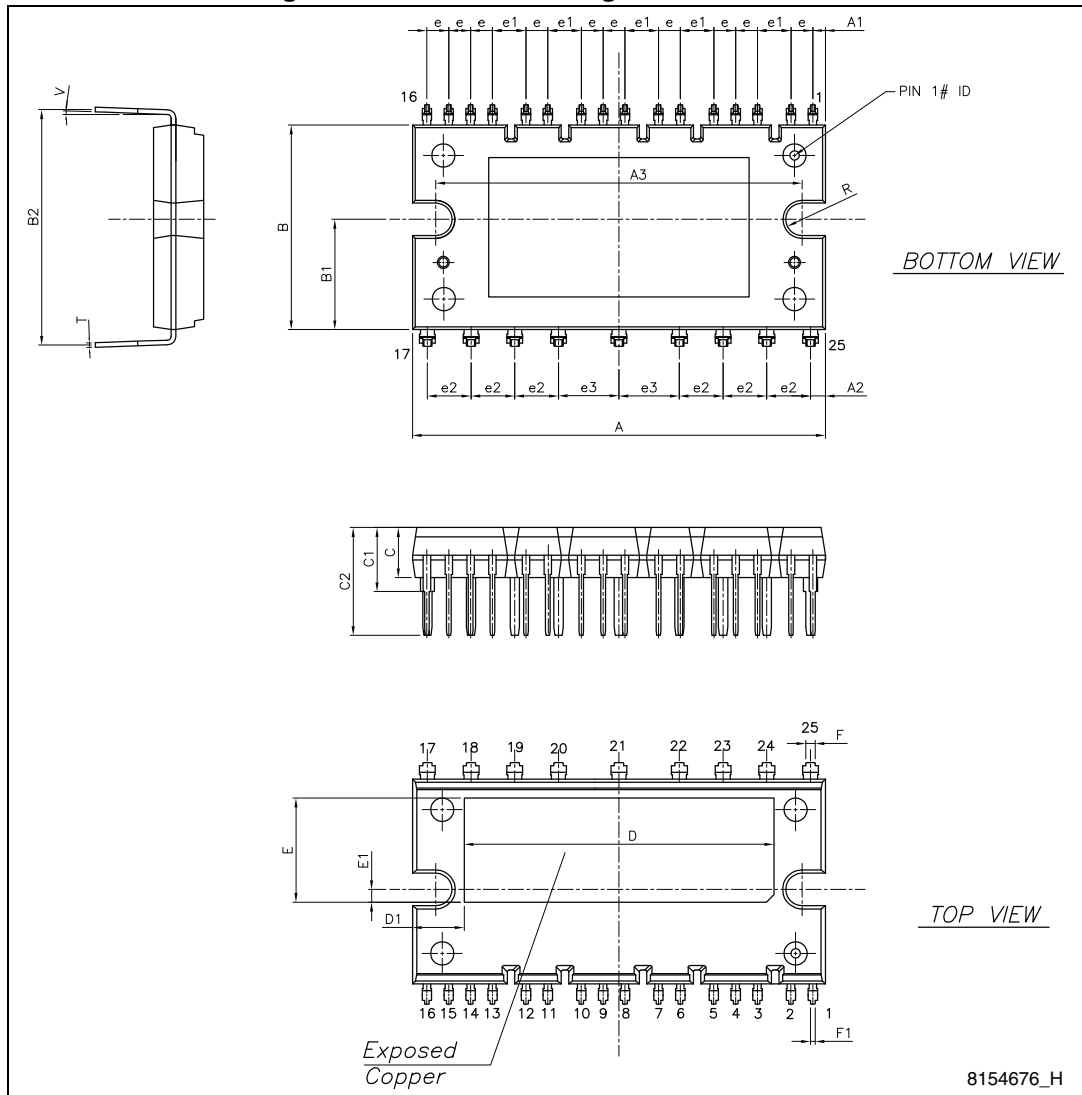


Figure 12. Packaging specifications of SDIP-25L package

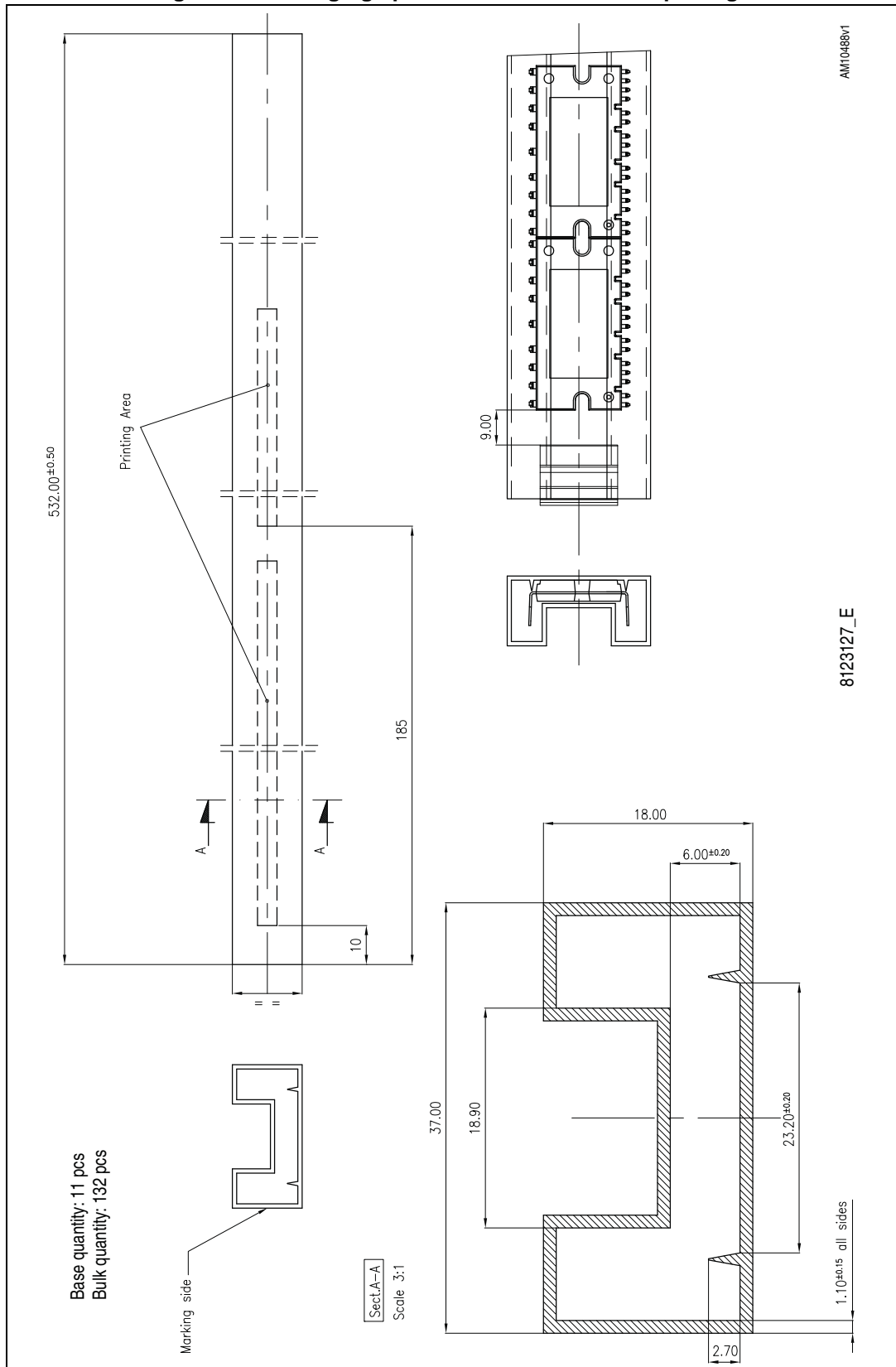
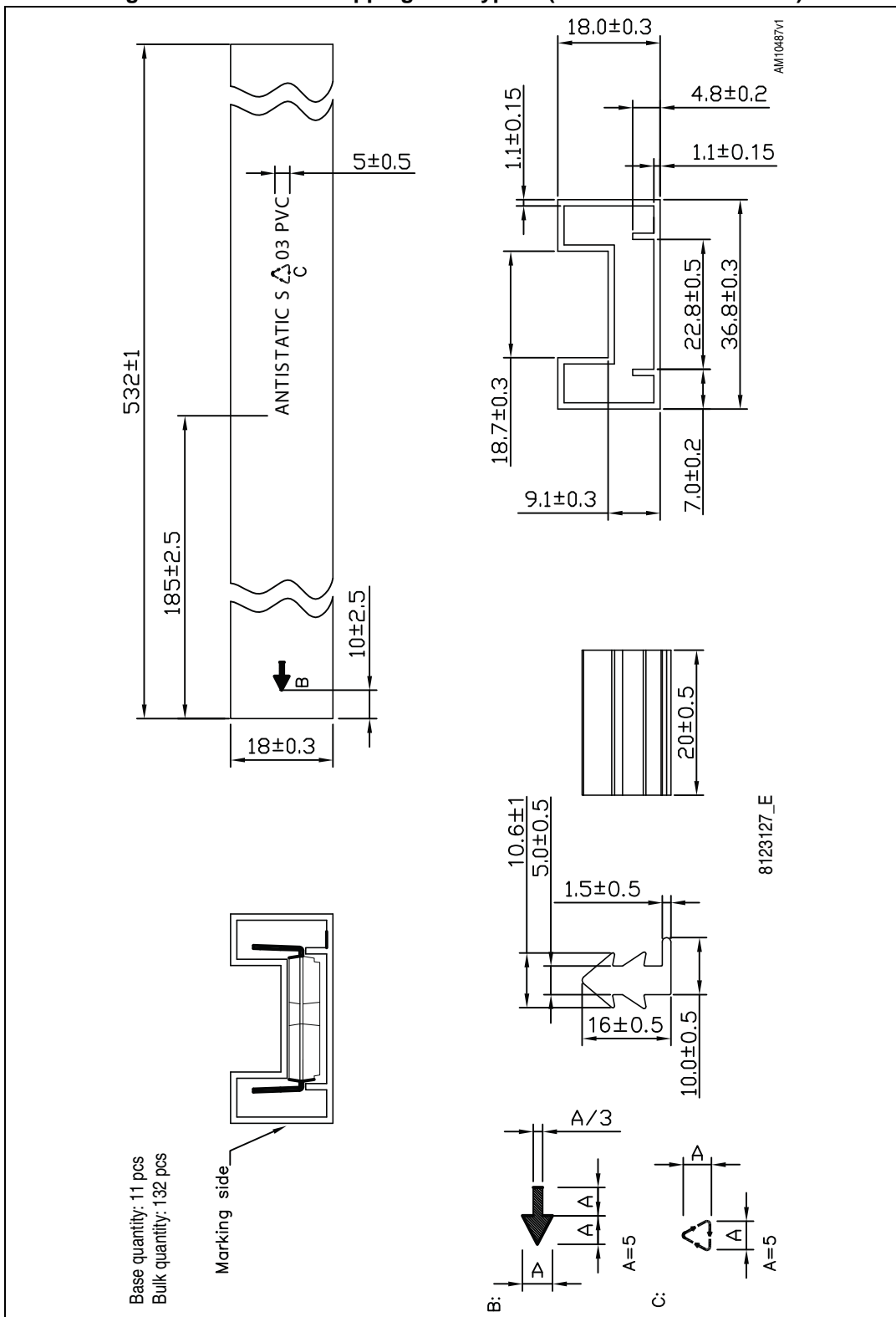


Figure 13. SDIP-25L shipping tube type B (dimensions are in mm.)



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
08-Apr-2013	1	Initial release.
15-Apr-2014	2	Document status promoted from preliminary to production data. Updated Figure 2: Pin layout (bottom view) .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com