DashDSP® 64-Lead Flash and ROM Memory Mixed-Signal DSP with Enhanced Analog Front End

ADMC(F)340

TARGET APPLICATIONS

Refrigerator and Air Conditioner Compressors, Washing Machines
Industrial Variable Speed Drives, HVAC

MOTOR TYPES

Permanent Magnet Synchronous Motors (PMSM), Brushless DC Motors (BDCM), AC Induction Motors (ACIM), Switched Reluctance Motors (SRM)

FEATURES

20 MHz Fixed-Point DSP Core
- Single Cycle Instruction Execution (50 ns)
- ADSP-21xx Family Code Compatibility
- Independent Computational Units
  - ALU
  - Multiplier/Accumulator
  - Barrel Shifter
- Multifunction Instructions
- Single Cycle Context Switch
- Powerful Program Sequencer
  - Zero Overhead Looping
  - Conditional Instruction Execution
- 2 Independent Data Address Generators

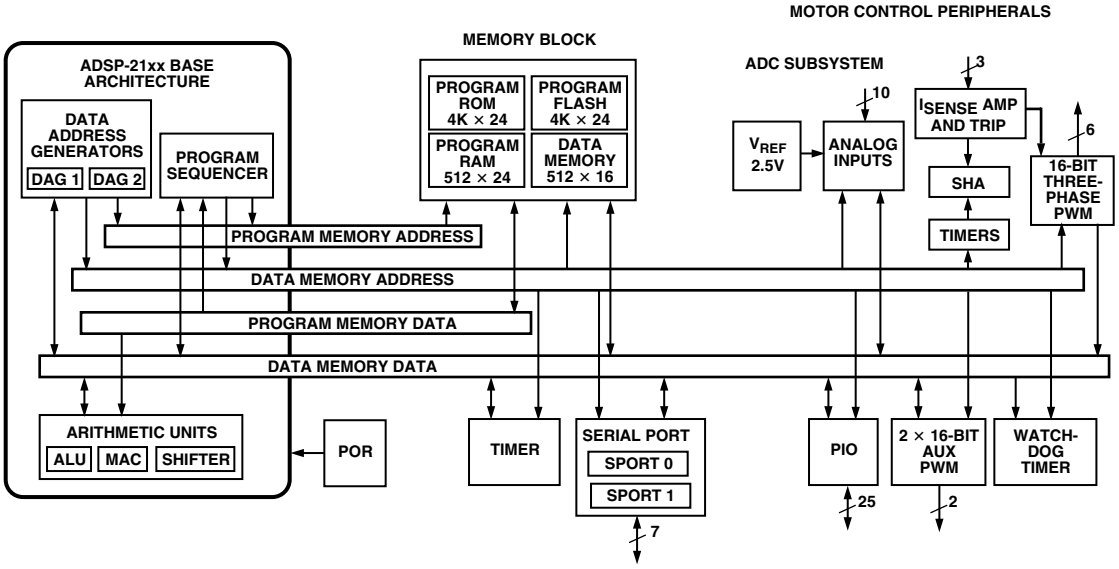
Memory Configuration
- 512 × 16-Bit Data Memory RAM
- 512 × 24-Bit Program Memory RAM
- 4K × 24-Bit Program Memory ROM
- 4K × 24-Bit Total Program FLASH Memory (ADMCF340 only)

3 Independent FLASH Memory Sectors
- 3584 × 24 Bit, 256 × 24 Bit, 256 × 24 Bit

Low Cost Pin Compatible ROM Option
16-Bit Watchdog Timer
Programmable 16-Bit Internal Timer with Prescaler
2 Double Buffered Serial Ports with SPI Mode Support
Integrated Power-On Reset Function
3-Phase 16-Bit PWM Generation Unit
- 16-Bit Center-Based PWM Generator
- Programmable PWM Pulsewidth
- Edge Resolution of 50 ns
- Programmable Narrow Pulse Deletion
- 153 Hz Minimum Switching Frequency
- Double/Single Update Mode Control
- Individual Enable and Disable for Each PWM Output
- High Frequency Chopping Mode for Transformer-Coupled Gate Drives

(continued on page 8)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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ANALOG-TO-DIGITAL CONVERTER (V_{DD} = 5%, GND = 0 V. For ADMCF340, T_A = –40°C to +85°C. For ADMC340, T_A = –40°C to +125°C. CLKIN = 10 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Signal Input	0.3		3.5	V	VAUX0, VAUX1, VAUX2
Resolution[1]			12	Bits	
Linearity Error[2]		3	4	Bits	
Zero Offset[3]	–32	0	+7	mV	
Comparator Delay		600		ns	
ADC High Level Input Current[2]			10	µA	V_{IN} = 3.5 V
ADC Low Level Input Current[2]	–10			µA	V_{IN} = 0.0 V

NOTES
[1]Resolution varies with PWM switching frequency (double update mode) 78.1 kHz = 8 bits, 4.9 kHz = 12 bits.
[2]2.44 kHz sample frequency, VAUX0, VAUX1, VAUX2.
[3]Extrapolated point outside of operating range. 2.44 kHz sample frequency.

Specifications subject to change without notice.

I_{SENSE} AMPLIFIER–TRIP

Parameter	Min	Typ	Max	Unit	Conditions/Comments
I_{SENSE} Signal Operating Range	–400		+400	mV	
I_{SENSE} Gain	–2.6	–2.51	–2.34	%	V_{IN} = –400 mV to +400 mV
I_{SENSE} Gain Channel Matching			5.5	%	V_{IN} = –400 mV to +400 mV
I_{SENSE} Gain Stability[1]		0.8		%	V_{IN} = –400 mV to +400 mV
I_{SENSE} Linearity[2]	8	9		Bits	
I_{SENSE} Internal Offset Voltage[2]	1.68	1.87	2.1	V	
I_{SENSE} Internal Offset Stability[2]		2.1		%	
I_{SENSE} Signal-to-Noise Ratio (SNR)[3]		51		dB	
I_{SENSE} Signal-to-Noise Ratio Less Distortion		54		dB	
(SNR)[3]		–40		dB	
I_{SENSE} Total Harmonic Distortion[3]		–53		dB	
I_{SENSE} Input Current	–200		+10	µA	V_{IN} = –400 mV to +400 mV
I_{SENSE} Input Resistance		11.5		kΩ	
TRIP Threshold Low	–690		–430	mV	
TRIP Threshold High	+430		+690	mV	
TRIP Minimum Pulsewidth[4]		5		µs	

NOTES
[1]Variation of gain with V_{DD} and temperature.
[2]V_{IN} = –400 mV to +400 mV.
[3]f_{IN} = 1 kHz sine wave, V_{IN} = –400 mV to +400 mV, f_S = 4 kHz.
[4]High or low TRIP threshold.

Specifications subject to change without notice.

CURRENT SOURCE[1]

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Programming Resolution			3	Bits	
Tuned Current[2]	91	100	109	µA	

NOTES
[1]For ADC calibration.
[2]0.3 V to 3.5 V I_{CONST} voltage.

Specifications subject to change without notice.

VOLTAGE REFERENCE

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Voltage Level (V_{REF})	2.44	2.50	2.55	V	–40°C to +85°C (ADMCF340 only)
	2.44	2.50	2.55	V	–40°C to +125°C (ADMC340 ROM only)
Drift		110		ppm/°C	

Specifications subject to change without notice.

POWER-ON RESET

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Reset Threshold	3.20	3.65	4.10	V	
Hysteresis		100		mV	
Reset Active Timeout Period		3.2*		ms	

*2^{16} CLKOUT cycles.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions/Comments
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2			V	
V_{IL}	Low Level Input Voltage[1]			1.75	V	
V_{IH}	High Level Input Voltage	2.60			V	
V_{OL}	Low Level Output Voltage[2]			0.4	V	I_{OL} = 2 mA
V_{OL}	Low Level Output Voltage[3]			0.8	V	I_{OL} = 2 mA
V_{OH}	High Level Output Voltage	4			V	I_{OH} = 0.5 mA
I_{IL}	Low Level Input Current RESET Pin[4]	–100			µA	V_{IN} = 0 V
I_{IL}	Low Level Input Current	–10			µA	V_{IN} = 0 V
I_{IH}	High Level Input Current RESET Pin[4]			30	µA	V_{IN} = V_{DD}
I_{IH}	High Level Input Current[5]			100	µA	V_{IN} = V_{DD}
I_{IH}	High Level Input Current			10	µA	V_{IN} = V_{DD}
I_{OZH}	High Level Three-State Leakage Current[6]			100	µA	V_{IN} = V_{DD}
I_{OZL}	Low Level Three-State Leakage Current[6]	–10			µA	V_{IN} = 0 V
I_{DD}	Supply Current (Idle)[7]			35	mA	V_{DD} = 5.25 V (ADMC340 only)
I_{DD}	Supply Current (Dynamic)[7]			60	mA	V_{DD} = 5.25 V (ADMC340 only)
I_{DD}	Supply Current (Idle)[7]			55	mA	V_{DD} = 5.25 V (ADMCF340 only)
I_{DD}	Supply Current (Dynamic)[7]			135	mA	V_{DD} = 5.25 V (ADMCF340 only)

NOTES
[1]PWMPOL and $\overline{\text{PWMSR}}$ pins only.
[2]Output pins PORTA0–PORTA8, PORTB0–PORTB15, AH, AL, BH, BL, CH, CL.
[3]XTAL pin.
[4]Internal pull-up, $\overline{\text{RESET}}$.
[5]Internal pull-down, $\overline{\text{PWMTRIP}}$, PORTA0–PORTA8, PORTB0–PORTB15.
[6]Three-stateable pins, DT1, RFS0, TFS0, SCLK1.
[7]Outputs not switching.

Specifications subject to change without notice.

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals				
Signal T_{CK} is defined as 0.5 t_{CKIN}. The ADMC(F)340 uses an input clock with a frequency equal to half the instruction rate; a 10 MHz input clock (which is equivalent to 100 ns) yields a 50 ns processor cycle (equivalent to 20 MHz). When T_{CK} values are within the range of 0.5 t_{CKIN} period, they should be substituted for all relevant timing parameters to obtain specification value as in the following example: $t_{CKH} = 0.5\ T_{CK} - 10\ ns = 0.5 \times 50\ ns - 10\ ns = 15\ ns$				
Timing Requirements:				
t_{CKIN}	CLKIN Period	100	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	0.5 T_{CK} – 10		ns
t_{CKH}	CLKOUT Width High	0.5 T_{CK} – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	5 T_{CK}*		ns
PWM Shutdown Signals				
Timing Requirement:				
t_{PWMTPW}	$\overline{\text{PWMTRIP}}$ Width Low	T_{CK}		ns

*Applies after power-up sequence is complete.

Specifications subject to change without notice.

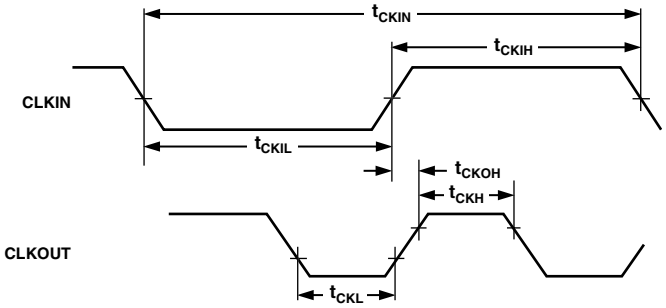


Figure 1. Clock Signals

TIMING PARAMETERS

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	100		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	15		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	20		ns
t_{SCP}	$SCLK_{IN}$ Width	40		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	0.25 T_{CK}	0.25 T_{CK} + 20	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		30	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		30	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{SCDD}	SCLK High to DT Disable		30	ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		25	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		30	ns

Specifications subject to change without notice.

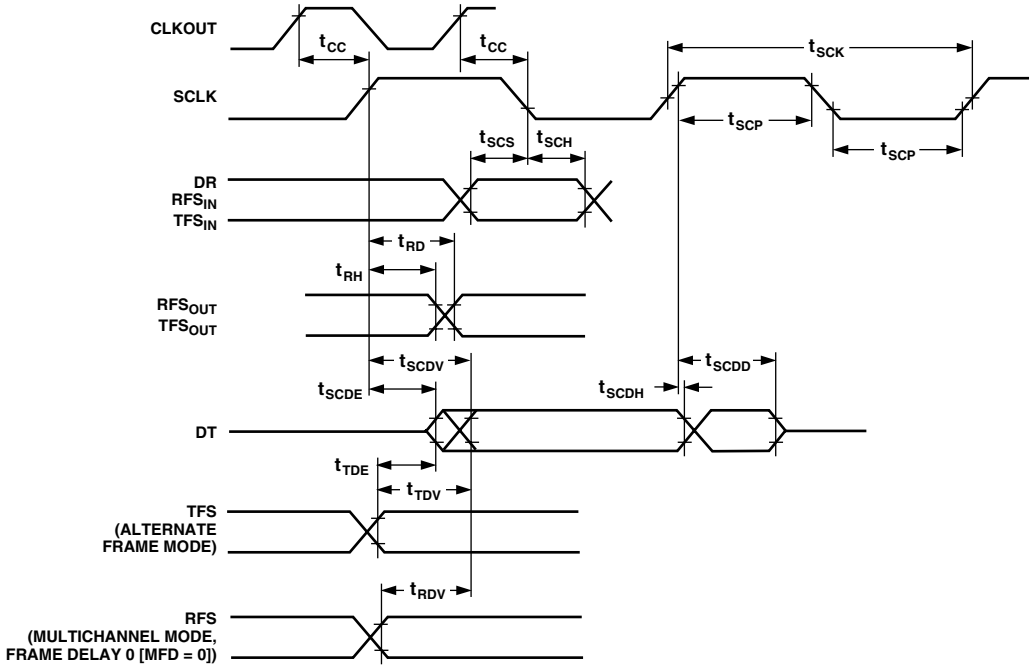


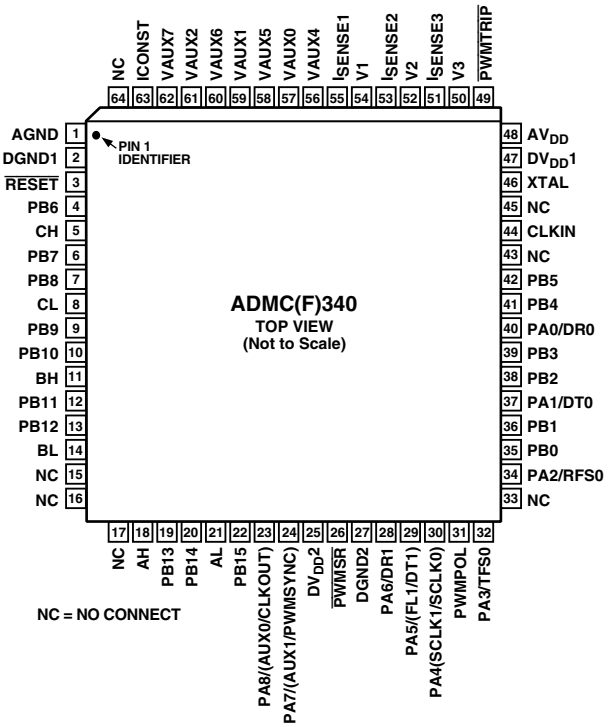
Figure 2. Serial Port Timing

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) . . . . . –0.3 V to +7.0 V
Supply Voltage (AV_{DD}) . . . . . –0.3 V to +7.0 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
ADMC340 Operating Temperature
Range (Ambient) . . . . . –40°C to +85°C
ADMC340 Operating Temperature
Range . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Instruction Rate	Package Description	Package Option
ADMC(F)340BST	–40°C to +85°C	20 MHz	64-Lead Thin Plastic Quad Flatpack (LQFP)	ST-64
ADMC(F)340-EVALKIT	N/A	N/A	Development Tool Kit	
ADMC340VST-XXX-XXXX	–40°C to +125°C	20 MHz	64-Lead LQFP	ST-64

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADMC(F)340 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Pin Type	Pin No.	Mnemonic	Pin Type
1	AGND	GND	33	NC	No Connect
2	DGND1	GND	34	PA2/RFS0	D_I/O
3	$\overline{\text{RESET}}$	D_IN	35	PB0	D_I/O
4	PB6	D_I/O	36	PB1	D_I/O
5	CH	D_OUT	37	PA1/DT0	D_I/O
6	PB7	D_I/O	38	PB2	D_I/O
7	PB8	D_I/O	39	PB3	D_I/O
8	CL	D_OUT	40	PA0/DR0	D_I/O
9	PB9	D_I/O	41	PB4	D_I/O
10	PB10	D_I/O	42	PB5	D_I/O
11	BH	D_OUT	43	NC	No Connect
12	PB11	D_I/O	44	CLKIN	D_I/O
13	PB12	D_I/O	45	NC	No Connect
14	BL	D_OUT	46	XTAL	A_OUT
15	NC	No Connect	47	$DV_{DD}1$	SUP
16	NC	No Connect	48	AV_{DD}	SUP
17	NC	No Connect	49	$\overline{\text{PWMTRIP}}$	D_IN
18	AH	D_OUT	50	V3	A_IN
19	PB13	D_I/O	51	I_{SENSE3}	A_IN
20	PB14	D_I/O	52	V2	A_IN
21	AL	D_OUT	53	I_{SENSE2}	A_IN
22	PB15	D_I/O	54	V1	A_IN
23	PA8/(AUX0/CLKOUT)	D_I/O	55	I_{SENSE1}	A_IN
24	PA7/(AUX1/PWMSYNC)	D_I/O	56	VAUX4	A_IN
25	$DV_{DD}2$	SUP	57	VAUX0	A_IN
26	$\overline{\text{PWMSR}}$	D_IN	58	VAUX5	A_IN
27	DGND2	GND	59	VAUX1	A_IN
28	PA6/DR1	D_I/O	60	VAUX6	A_IN
29	PA5/(FL1/DT1)	D_I/O	61	VAUX2	A_IN
30	PA4/(SCLK1/SCLK0)	D_I/O	62	VAUX7	A-IN
31	PWMPOL	D-IN	63	ICONST	A_OUT
32	PA3/TFS0	D_I/O	64	NC	No Connect

PA is the abbreviation of PORTA; PB is the abbreviation of PORTB.

(continued from page 1)

External $\overline{\text{PWMTRIP}}$ Pin
Switched Reluctance Motor Mode Selection Pin
PWM Polarity Selection Pin
Integrated 13-Channel ADC Subsystem
3 Bipolar I_{SENSE} Inputs with Programmable Sample-and-Hold Amplifier and Overcurrent Protection (Usable as 3 Dedicated Analog Inputs)
3 Simultaneous Converting Voltage Inputs
7 Muxed Auxiliary Analog Inputs
Internal Voltage Reference (2.5 V)
Acquisition Synchronized to PWM Switching Frequency
25-Lead Digital I/O Port
Bit Configurable as Input or Output
Change of State Interrupt Support
2 16-Bit Auxiliary PWM Timers
Synthesized Analog Output
Programmable Frequency
0% to 100% Duty Cycle
2 Programmable Operation Modes
Independent Mode/Offset Mode

GENERAL DESCRIPTION

The ADMC(F)340 is a low cost, single-chip DSP-based controller suitable for permanent magnet synchronous, ac induction, switched reluctance, and brushless dc motors. The ADMC(F)340 integrates a 20 MHz, fixed-point DSP core with a complete set of motor control and system peripherals for fast, efficient development of motor controllers.

The DSP core of the ADMC(F)340 is completely code compatible with the ADSP-21xx DSP family and combines three computational units, data address generators, and a program sequencer. The computational units comprise an ALU, a multiplier/accumulator (MAC), and a barrel shifter. There are special instructions for bit manipulation, multiplication (x squared), biased rounding, and global interrupt masking. The system peripherals are the power-on reset circuit (POR), the watchdog timer, and two synchronous serial ports. The serial ports are configurable and double buffered, with hardware support for UART, SCI, and SPI port emulation. The ADMC(F)340 provides 512 × 24-bit program memory RAM, 4K × 24-bit program memory ROM, 4K × 24-bit program FLASH memory, and 512 × 16-bit data memory RAM. The user code will be stored and executed from the flash memory. The program and data memory RAM can be used for dynamic data storage or can be loaded through the serial port from an external device as in other ADMCxx family parts. The program memory ROM contains a monitor function as well as useful routines for erasing, programming, and verifying the flash memory.

The motor control peripherals of the ADMC(F)340 provide a 12-bit analog data acquisition system with 13 analog input channels, three dedicated I_{SENSE} functions (combining internal amplification, sampling, and overcurrent PWM shutdown features), and an internal voltage reference. In addition, a three-phase, 16-bit, center-based PWM generation unit can be used to produce high accuracy PWM signals with minimal processor overhead. The ADMC(F)340 also contains two 16-bit auxiliary PWM timers and 25 lines of programmable digital I/O.

Several functions, such as the auxiliary PWM and the serial communication ports, are multiplexed with the nine PORTA (9, PIO) programmable input/output (PIO) pins. The other 16 programmable digital I/O pins are dedicated. The pin functions can be independently selected to allow maximum flexibility for different applications.

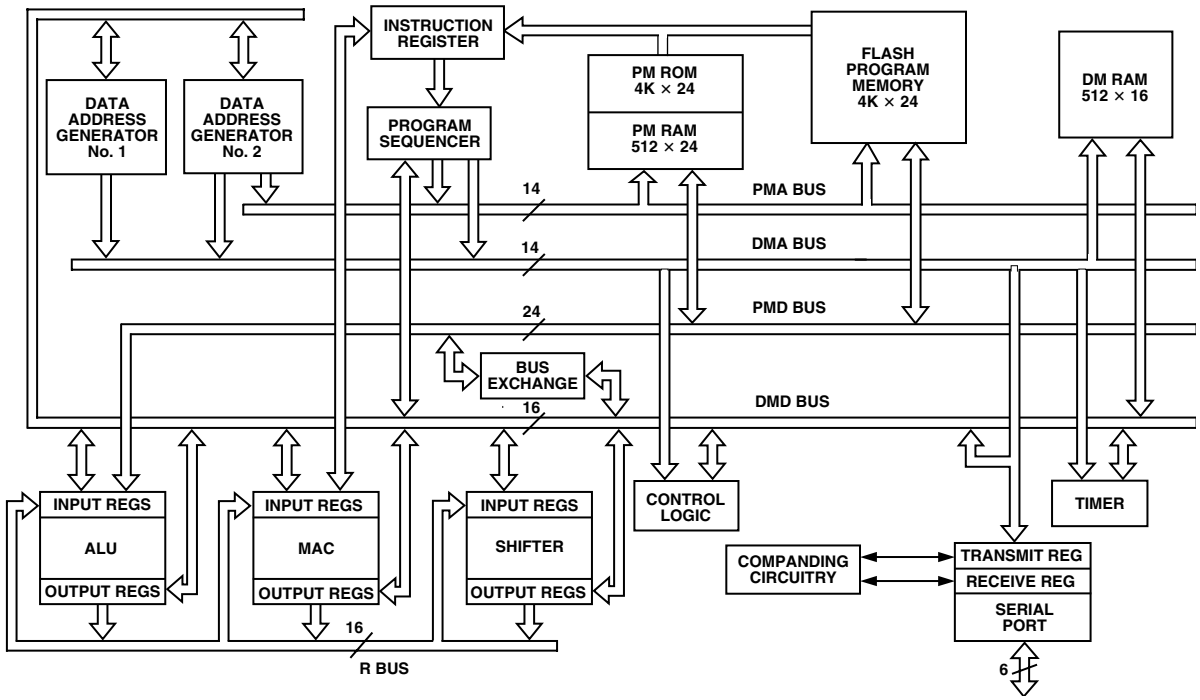


Figure 3. DSP Core Block Diagram

DSP CORE ARCHITECTURE OVERVIEW

Figure 3 is an overall block diagram of the DSP core of the ADMC(F)340. The flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle (50 ns with a 10 MHz CLKIN), the DSP core can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This all takes place while the processor continues to:

- Receive and transmit through the serial ports
- Decrement the interval timer
- Generate three-phase PWM waveforms for a power inverter
- Generate two signals using the 16-bit auxiliary PWM timers
- Acquire four analog signals
- Decrement the watchdog timer

The processor contains three independent computational units: the arithmetic and logic unit (ALU), the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations as well as provides support for division primitives. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive-exponent operations. The shifter can be used to efficiently implement numeric format control, including floating-point representations. The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps and subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADMC(F)340 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from data memory and program memory. Each DAG maintains and updates four address pointers (I registers). Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value in one of four modify (M) registers. A length value may be associated with each pointer (L registers) to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to and from on-chip memory. DAG1 generates only data memory addresses and provides an optional bit-reversal capability. DAG2 may generate either program or data memory addresses but has no bit-reversal capability. Efficient data transfer is achieved with the use of five internal buses:

- Program memory address (PMA) bus
- Program memory data (PMD) bus
- Data memory address (DMA) bus
- Data memory data (DMD) bus
- Result (R) bus

Program memory can store both instructions and data, permitting the ADMC(F)340 to fetch two operands in a single cycle—one from program memory and one from data memory. The ADMC(F)340 can fetch both an operand from on-chip program memory and the next instruction in the same cycle. The ADMC(F)340 writes data from its 16-bit registers to the 24-bit program memory by using the PX Register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed into the PX Register.

The ADMC(F)340 can respond to a number of distinct DSP core and peripheral interrupts. The DSP interrupts comprise a serial port receive interrupt, a serial port transmit interrupt, a timer interrupt, and two software interrupts. Additionally, the motor control peripherals include two PWM interrupts and a PIO interrupt.

The serial port (SPORT0) provides a complete synchronous serial interface with optional companding in hardware and a wide variety of framed and unframed data transmit and receive modes of operation. SPORT0 and SPORT1 can generate an internal programmable serial clock or accept an external serial clock.

A programmable interval counter is also included in the DSP core and can be used to generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every n processor cycle, where n – 1 is a scaling value stored in the 8-bit TSCALE Register. When the value of the counter reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADMC(F)340 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Each instruction is executed in a single 50 ns processor cycle (for a 10 MHz CLKIN). The ADMC(F)340 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development. For further information on the DSP core, refer to the *ADSP-2100 Family User's Manual*, Third Edition, with particular reference to the ADSP-2171.

SERIAL PORTS

The ADMC(F)340 incorporates two synchronous serial ports (SPORT1 and SPORT0) for serial communication and multiprocessor communication. SPORT1 is primarily intended for the interfacing of the debugging tools and/or code booting from an external serial memory.

The following is a brief list of capabilities of the ADMC(F)340 SPORTs:

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame synchronization signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data-word lengths from three bits to 16 bits and provide optional A-law and μ-law companding according to ITU (formerly CCITT) recommendation G.711.
- SPORTs' receive and transmit sections can generate unique interrupts on completing a data-word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data-word. An interrupt is generated after a data buffer transfer.

- SPORT0 has one pin, SCLK0, shared with SPORT1. During a boot phase (SPORT1 Boot Mode enabled by a bit in the MODECTRL Register), the serial clock of SPORT1 is externally available. The serial clock of SPORT0 is externally available when the SPORT1 is configured in UART Mode.
- SPORT0 can be configured as a SPI Port (master mode only). Refer to Table XI for more information. The clock phase and polarity are programmable through the MODECTRL Register. Refer to Table XI for pin configuration.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24-word or 32-word time division multiplexed serial bit stream.
- SPORT1 is the default port for program/data memory boot loading and for the development tools interface. The DT1/FL1 pin can be configured as the SROM/E^2 PROM reset signal.

The ADMC(F)340 is available in a 64-lead LQFP package.

PIN FUNCTION DESCRIPTION

Table I. Pin List

Pin Group Name	No. of Pins	Input/ Output	Function
PWMPOL	1	I	PWM Polarity
$\overline{\text{PWMSR}}$	1	I	PWM Switched Reluctance Mode
$\overline{\text{RESET}}$	1	I	Processor Reset Input
SPORT1[1]	2	I/O	Serial Port 1 Pins (DT1/FL1, DR1)
SPORT0[1]	5	I/O	Serial Port 0 Pins (DT0, DR0, RFS0, TFS0, SCLK1/ SCLK0[2])
CLKOUT[1]	1[1]	I/O	Processor Clock Output
CLKIN, XTAL	2	I/O	External Clock or Quartz Crystal Connection Point
PORTA0–PORTA8[1]	9	I/O	Digital I/O Port Pins
PORTB0–PORTB15	16	I/O	Digital I/O Port Pins
AUX0–AUX1[1]	2	O	Auxiliary PWM Outputs
AH-CL	6	O	PWM Outputs
$\overline{\text{PWMTRIP}}$	1	I	PWM Trip Signal
V1 to V3	3	I	I_{SENSE} Inputs
I_{SENSE1} to I_{SENSE3}	3	I	Analog Inputs
VAUX0-VAUX7	7	I	Auxiliary Analog Inputs
ICONST	1	O	ADC Constant Current Source
DV_{DD}	3	I	Power Supply
AV_{DD}	3	I	Power Supply
GND	3	I	Ground

NOTES
[1]Multiplexed pins, individually selectable through PORTA_SELECT and PORTA_DATA Registers.
[2]SCLK1/SCLK0 multiplexed signals, selectable through MODECTRL Register Bit 4.

INTERRUPT OVERVIEW

The ADMC(F)340 can respond to 34 different interrupt sources with minimal overhead, seven of which are internal DSP core interrupts and 27 of which are from the motor control peripherals. The seven DSP core interrupts are SPORT1 receive (or $\overline{\text{IRQ0}}$) and transmit (or $\overline{\text{IRQ1}}$), SPORT0 receive and transmit, the internal timer, and two software interrupts. The motor control peripheral interrupts are the 25 programmable I/Os and two from the PWM (PWMSYNC pulse and $\overline{\text{PWMTRIP}}$). All motor control interrupts are multiplexed into the DSP core through the peripheral $\overline{\text{IRQ2}}$ interrupt. The interrupts are internally prioritized and individually maskable. A detailed description of the entire interrupt system of the ADMC(F)340 is presented in the Interrupt Control section, which follows the detailed descriptions of each peripheral block.

MEMORY MAP

The ADMC(F)340 has two distinct memory types: program and data. In general, program memory contains user code and coefficients, while the data memory is used to store variables and data during program execution. Three kinds of program memory are provided on the ADMC(F)340: RAM, ROM, and FLASH. The motor control peripherals are memory mapped into a region of the data memory space starting at 0x2000. The complete program and data memory maps are given in Tables II and III, respectively.

Table II. Program Memory Map

Address Range	Memory Type	Function
0x0000–0x002F	RAM	Internal Vector Table
0x0030–0x01FF	RAM	User Program Memory
0x0200–0x07FF		Reserved
0x0800–0x17FF	ROM	Reserved Program Memory
0x1800–0x1FFF		Reserved
0x2000–0x20FF	FLASH	User Program Memory Sector 0
0x2100–0x21FF	FLASH	User Program Memory Sector 1
0x2200–0x2FFF	FLASH	User Program Memory Sector 2
0x3000–0x3FFF		Reserved

Table III. Data Memory Map

Address Range	Memory Type	Function
0x0000–0x1FFF		Reserved
0x2000–0x20FF		Memory Mapped Registers
0x2100–0x37FF		Reserved
0x3800–0x39FF	RAM	User Data Memory
0x3A00–0x3BFF	RAM	Reserved
0x3C00–0x3FFF		Memory Mapped Registers

FLASH MEMORY SUBSYSTEM

The ADMC(F)340 has 4K × 24-bit user-programmable, nonvolatile flash memory. A flash programming utility is provided with the development tools and performs the basic device programming operations: erase, program, and verify.

The flash memory array is portioned into three asymmetrically sized sectors of 256 words, 256 words, and 3,584 words, labeled Sector 0, Sector 1, and Sector 2, respectively. These sectors are mapped into external program memory address space.

Four flash memory interface registers are connected to the DSP. These 16-bit registers are mapped into the register area of data memory space. They are named Flash Memory Control Register (FMCR), Flash Memory Address Register (FMAR), Flash Memory Data Register Low (FMDRL), and Flash Memory Data Register High (FMDRH). These registers are diagrammed beginning with Figure 21. They are used by the flash memory programming utility. The user program may read these registers but should not modify them directly. The flash programming utility provides a complete interface to the flash memory.

Note that from the point of view of 2171 core, the flash memory is placed externally. It means the core accesses them through an external memory interface that multiplexes the program memory and data memory buses into a single external bus. Therefore, if more than one external transfer must be made in the same instruction, there will be at least one overhead cycle required.

Special Flash Registers

The flash module has four nonvolatile 8-bit registers called Special Flash Registers (SFRs) that are accessible independently of the main flash array via the flash programming utility. These registers are for general-purpose, nonvolatile storage. When erased, the Special Flash Registers contain all 0s. To read Special Flash Registers from the user program, call the read_reg routine contained in the ROM. Refer to the *ADMCF34x DSP Motor Controller Developers' Reference Manual* for an example.

Boot-from-Flash Code

A security feature is available in the form of a code that when set causes the processor to execute the program in flash memory at power-up or reset. In this mode, the flash programming utility and debugger are unable to communicate with the ADMC(F)340. Consequently, the contents of the flash memory can be neither programmed nor read.

The boot-from-flash code may be set via the flash programming utility when the user's program is thoroughly tested and loaded into flash program memory at Address 0x2200. The user's program must contain a mechanism for clearing the boot-from-flash code if reprogramming the flash memory is desired. The only way to clear boot-from-flash is from within the user program, by calling the flash_init or auto_erase_reg routines that are included in the ROM. The user program must be signaled in some way to call the necessary routine to clear the boot-from-flash code. An example would be to detect a high level on a PIO pin during startup initialization and then call the flash_init or auto-erase-reg routine. The flash_init routine will erase the entire user program in flash memory before clearing the boot-from-flash code, thus ensuring the security of the user program. If security is not a concern, the auto_erase_reg routine can be used to clear the boot-from-flash code while leaving the user program intact.

Refer to the *ADMCF34x DSP Motor Controller Developers' Reference Manual* for further instructions and an example of using the boot-from-flash code.

FLASH PROGRAM BOOT SEQUENCE

On power-up or reset, the processor begins instruction execution at Address 0x0800 of internal program ROM. The ROM monitor program that is located there checks the boot-from-flash code. If that code is set, the processor jumps to location 0x2200 in external flash program memory, where it expects to find the user's application program.

If the boot-from-flash code is not set, the monitor attempts to boot from an external device as described in the *ADMCF34x DSP Motor Controller Developers' Reference Manual.*

SYSTEM INTERFACE

Figure 4 shows a basic system configuration for the ADMC(F)340 with an external crystal.

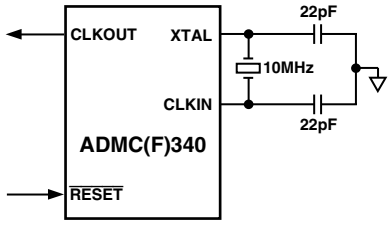


Figure 4. Basic System Configuration

Clock Signals

The ADMC(F)340 can be clocked either by a crystal or a TTL compatible clock signal. For normal operation, the CLKIN input cannot be halted, changed during operation, or operated below the specified minimum frequency. If an external clock is used, it should be a TTL compatible signal running at half the instruction rate. The signal is connected to the CLKIN pin of the ADMC(F)340. In this mode, with an external clock signal, the XTAL pin must be left unconnected. The ADMC(F)340 uses an input clock with a frequency equal to half the instruction rate; a 10 MHz input clock yields a 50 ns processor cycle (which is equivalent to 20 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction rate that is indicated by the CLKOUT signal when enabled.

Because the ADMC(F)340 includes an on-chip oscillator feedback circuit, an external crystal may be used instead of a clock source, as shown in Figure 2. The crystal should be connected across the CLKIN and XTAL pins with two capacitors (see Figure 2). A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. A clock output signal (CLKOUT) is generated by the processor at the processor's cycle rate of twice the input frequency.

Reset

The ADMC(F)340 DSP core and peripherals must be correctly reset when the device is powered up to ensure proper unitization. The ADMC(F)340 contains an integrated power-on-reset (POR) circuit that provides a complete system reset on power-up and power-down. The POR circuit monitors the voltage on the ADMC(F)340 V_{DD} pin and holds the DSP core and peripherals in reset while V_{DD} is less than the threshold voltage level, V_{RST}. When this voltage is exceeded, the ADMC(F)340 is held in reset for an additional 2^{16} DSP clock cycles (T_{RST} in Figure 5). During this time (T_{RST}), the supply voltage must reach the recommended operating condition. On power-down, when the voltage on the V_{DD} pin falls below $V_{RST} - V_{HYST}$, the ADMC(F)340 will be reset. Also, if the external $\overline{RESET}$ pin is actively pulled low at any time after power-up, a complete hardware reset of the ADMC(F)340 is initiated.

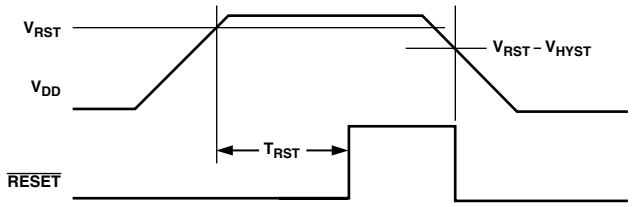


Figure 5. Power-On Reset Operation

The ADMC(F)340 sets all internal stack pointers to the empty stack condition, masks all interrupts, clears the MSTAT Register, and performs a full reset of all the motor control peripherals. Following a power-up, it is possible to initiate a DSP core and motor control peripheral reset by pulling the $\overline{RESET}$ pin low. The $\overline{RESET}$ signal must be the minimum pulsewidth specification, t_{RSP}. Following the reset sequence, the DSP core starts executing code from the internal PM ROM located at 0x0800.

DSP Control Registers

The DSP core has a system control register, SYSCNTL, memory-mapped at DM (0x3FFF). SPORT1 must be configured as a serial port by setting Bit 10. SPORT0 and SPORT1 are enabled by setting Bit 11 and Bit 12.

The DSP core has a wait state control register, MEMWAIT, memory-mapped at DM (0x3FFE). The default value of this register is 0xFFFF. For proper operation of the ADMC(F)340, this register must always contain the value 0x8000. This value sets the minimum access time to the program memory.

The configurations of both the SYSCNTL and MEMWAIT Registers of the ADMC(F)340 are shown in Figure 30.

THREE-PHASE PWM CONTROLLER

Overview

The PWM generator block of the ADMC(F)340 is a flexible, programmable, three-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a three-phase voltage source inverter for ac induction motors (ACIM) or permanent magnet synchronous motors (PMSM). In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of electronically commutated motors (ECM), brushless dc motors (BDCM), or switched reluctance motors (SRM).

The six PWM output signals consist of three high side drive signals (AH, BH, and CH) and three low side drive signals (AL, BL, and CL). The switching frequency, dead time, and minimum pulsewidths of the generated PWM patterns are programmable using, respectively, the PWMTM, PWMDT, and PWMPD Registers. In addition, three registers (PWMCHA, PWMCHB, and PWMCHC) control the duty cycles of the three pairs of PWM signals.

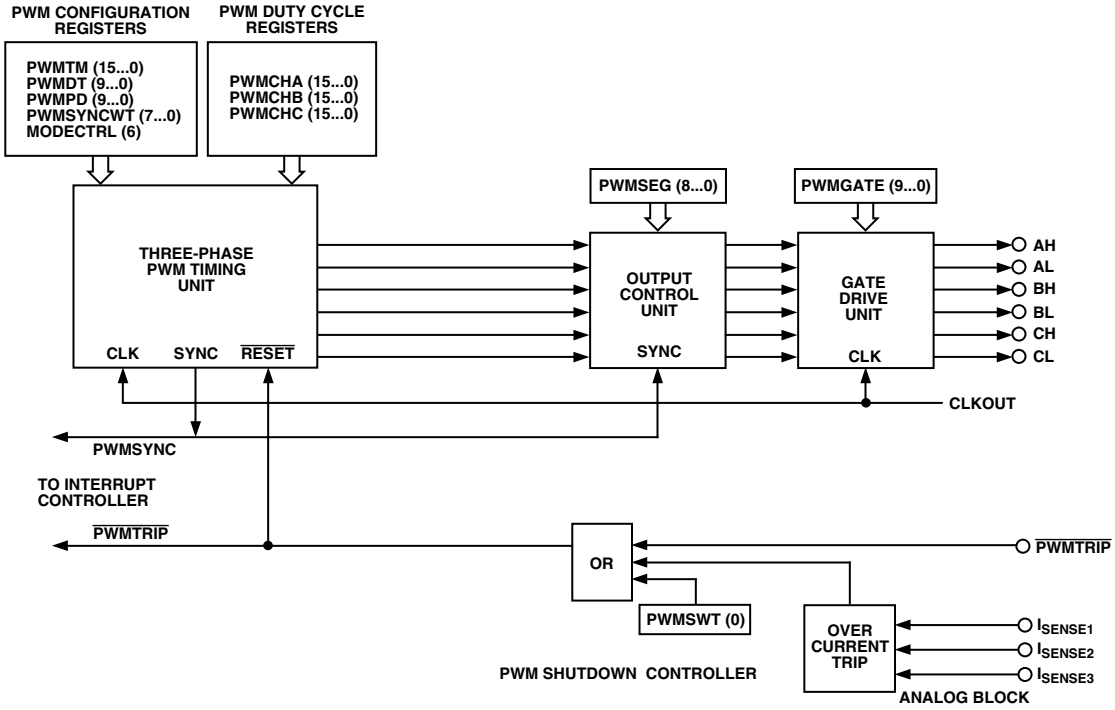


Figure 6. Overview of the PWM Controller of the ADMC(F)340

Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMSEG Register. In addition, three control bits of the PWMSEG Register permit crossover of the two signals of a PWM.

In Crossover Mode, the high side PWM signals are diverted to the complementary low side output and low side signals are diverted to the corresponding high side output.

In many applications, there is a need to provide an isolation barrier in the gate-drive circuits that turn on the power devices of the inverter. In general, there are two common isolation techniques: optical isolation using optocouplers and transformer isolation using pulse transformers. The PWM controller of the ADMC(F)340 permits mixing the output PWM signals with a high frequency chopping signal to permit an easy interface to such pulse transformers. The features of this gate-drive chopping mode can be controlled by the PWMGATE Register. There is an 8-bit value within the PWMGATE Register that directly controls the chopping frequency. In addition, high frequency chopping can be independently enabled for the high side and the low side outputs using separate control bits in the PWMGATE Register.

The PWM generator is capable of operating in two distinct modes: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM duty cycle values is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters. This technique also permits the closed-loop controller to change the average voltage applied to the machine winding at a faster rate, allowing wider closed-loop bandwidths to be achieved. The operating mode of the PWM block (single or double update mode) is selected by a control bit in MODECTRL Register.

The PWM generator of the ADMC(F)340 also provides an internal signal that synchronizes the PWM switching frequency to the A/D operation. In single update mode, a PWMSYNC pulse is produced at the start of each PWM period. In double update mode, an additional PWMSYNC pulse is produced at the midpoint of each PWM period. The width of the PWMSYNC pulse is programmable through the PWMSYNCWT Register.

The PWM signals produced by the ADMC(F)340 can be shut off in a number of different ways. First, there is a dedicated asynchronous PWM shutdown pin, $\overline{\text{PWMTRIP}}$, which, when brought low, instantaneously places all six PWM outputs in the OFF state. In addition, PWM shutdown is initiated when the voltage on any of the three I_{SENSE} input pins exceed the trip thresholds (high or low). Because these two hardware shutdown mechanisms are asynchronous, and the associated PWM disable circuitry does not use clocked logic, the PWM will shut down even if the DSP clock is not running. The PWM system may also be shut down from software by writing to the PWMSWT Register.

Status information about the PWM system of the ADMC(F)340 is available to the user in the SYSSTAT Register. In particular, the status of $\overline{\text{PWMTRIP}}$ is available, as well as a status bit that indicates whether operation is in the first half or the second half of the PWM period.

A functional block diagram of the PWM controller is shown in Figure 6. The generation of the six output PWM signals on pins AH to CL is controlled by four important blocks:

- The three-phase PWM timing unit, which is the core of the PWM controller, generates three pairs of complemented and dead-time-adjusted center-based PWM signals.
- The output control unit allows the redirection of the outputs of the three-phase timing unit for each channel to either the high side or low side output. In addition, the output control unit allows individual enabling/disabling of each of the six PWM output signals.
- The GATE drive unit provides the high chopping frequency and its subsequent mixing with the PWM signals.
- The PWM shutdown controller manages the three PWM shutdown modes (via the $\overline{\text{PWMTRIP}}$ pin, the analog block, or the PWMSWT Register) and generates the correct $\overline{\text{RESET}}$ signal for the Timing Unit.
- The PWM controller is driven by a clock at the same frequency as the DSP instruction rate, CLKOUT, and is capable of generating two interrupts to the DSP core. One interrupt is generated on the occurrence of a PWMSYNC pulse, and the other is generated on the occurrence of any PWM shutdown action.

Three-Phase Timing Unit

The 16-bit three-phase timing unit is the core of the PWM controller and produces three pairs of pulsewidth modulated signals with high resolution and minimal processor overhead. There are four main configuration registers (PWMTM, PWMDT, PWMPD, and PWMSYNCWT) that determine the fundamental characteristics of the PWM outputs. In addition, the operating mode of the PWM (single or double update mode) is selected by Bit 6 of the MODECTRL Register. These registers, in conjunction with the three 16-bit duty cycle registers (PWMCHA, PWMCHB, and PWMCHC), control the output of the three-phase timing unit.

PWM Switching Frequency: PWMTM Register

The PWM switching frequency is controlled by the PWM period register, PWMTM. The fundamental timing unit of the PWM controller is $T_{CK} = 1/f_{CLKOUT}$, where f_{CLKOUT} is the CLKOUT frequency (DSP instruction rate). Therefore, for a 20 MHz CLKOUT, the fundamental time increment is 50 ns. The value written to the PWMTM Register is effectively the number of T_{CK} clock increments in half of a PWM period. The required *PWMTM* value is a function of the desired PWM switching frequency (f_{PWM}) and is given by:

$$PWMTM = \frac{f_{CLKOUT}}{2 \times f_{PWM}} = \frac{f_{CLKIN}}{f_{PWM}}$$

Therefore, the *PWM* switching period, T_S, can be written as:

$$T_S = 2 \times PWMTM \times T_{CK}$$

For example, for a 20 MHz CLKOUT and a desired PWM switching frequency of 10 kHz (T_S = 100 μs), the correct value to load into the *PWMTM* Register is:

$$PWMTM = \frac{20 \times 10^6}{2 \times 10 \times 10^3} = 1000 = 0x3E8$$

The largest value that can be written to the 16-bit PWMTM Register is 0xFFFF = 65,535, which corresponds to a minimum PWM switching frequency of:

$$f_{PWM,\min} = \frac{20 \times 10^6}{2 \times 65,535} = 153\ Hz$$

for a CLKOUT frequency of 20 MHz.

PWM Switching Dead Time: PWMDT Register

The second important PWM block parameter that must be initialized is the switching dead time. This is a short delay time introduced between turning off one PWM signal (e.g., AH) and turning on its complementary signal (e.g., AL). This short time delay is introduced to permit the power switch being turned off to completely recover its blocking capability before the complementary switch is turned on. This time delay prevents a potentially destructive short circuit condition from developing across the dc link capacitor of a typical voltage source inverter.

Dead time is controlled by the PWMDT Register. The dead time is inserted into the three pairs of PWM output signals. The dead time, T_D, is related to the value in the PWMDT Register by:

$$T_D = PWMDT \times 2 \times T_{CK} = 2 \times \frac{PWMDT}{f_{CLKOUT}}$$

Therefore, a *PWMDT* value of 0x00A (= 10) introduces a 1 μs delay between the turn-off of any PWM signal (e.g., AH) and the turn-on of its complementary signal (e.g., AL). The amount of the dead time can therefore be programmed in increments of 2 T_{CK} (or 100 ns for a 20 MHz CLKOUT). The PWMDT Register is a 10-bit register. For a CLKOUT rate of 20 MHz, its maximum value of 0x3FF (= 1023) corresponds to a maximum programmed dead time of:

$$\begin{aligned} T_{D\max} &= 1023 \times 2 \times T_{CK} \\ &= 1023 \times 2 \times 50 \times 10^{-9}\ sec \\ &= 102\ \mu s \end{aligned}$$

The dead time can be programmed to zero by writing 0 to the PWMDT Register.

PWM Operating Mode: MODECTRL and SYSSTAT Registers

The PWM controller of the ADMC(F)340 can operate in two distinct modes: single update mode and double update mode. The operating mode of the PWM controller is determined by the state of Bit 6 of the MODECTRL Register. If this bit is cleared, the PWM operates in the single update mode. Setting Bit 6 places the PWM in the double update mode. By default, following either a peripheral reset or power-on, Bit 6 of the MODECTRL Register is cleared. This means that the default operating mode is single update mode.

In single update mode, a single PWMSYNC pulse is produced in each PWM period. The rising edge of this signal marks the start of a new PWM cycle and is used to latch new values from the PWM configuration registers (PWMTM, PWMDT, PWMPD, and PWMSYNCWT) and the PWM duty cycle registers (PWMCHA, PWMCHB, and PWMCHC) into the three-phase timing unit. The PWMSEG Register is also latched into the output control unit on the rising edge of the PWMSYNC pulse. In effect, this means that the parameters of the PWM signals can be updated only once per PWM period at the start of each cycle. Thus, the generated PWM patterns are symmetrical centered around the midpoint of the switching period.

In double update mode, there is an additional PWMSYNC pulse produced at the midpoint of each PWM period. The rising edge of this new PWMSYNC pulse is again used to latch new values of the PWM configuration registers, duty cycle registers, and the PWMSEG Register. As a result, it is possible to alter both the characteristics (switching frequency, dead time, minimum pulsewidth, and PWMSYNC pulsewidth) and the output duty cycles at the midpoint of each PWM cycle. Consequently, it is possible to produce PWM switching patterns that are no longer symmetrical centered around the midpoint of the period (asymmetrical PWM patterns).

In the double update mode, operation in the first half or the second half of the PWM cycle is indicated by Bit 3 of the SYSSTAT Register. In double update mode, this bit is cleared during operation in the first half of each PWM period (between the rising edge of the original PWMSYNC pulse and the rising edge of the new PWMSYNC pulse, which is introduced in double update mode). Bit 3 of the SYSSTAT Register is set during the second half of each PWM period. If required, a user may determine the status of this bit during a PWMSYNC interrupt service routine.

The advantages of the double update mode are that lower harmonic voltages can be produced by the PWM process and wider control bandwidths are possible. However, for a given PWM switching frequency, the PWMSYNC pulses occur at twice the rate in the double update mode. Because new duty cycle values must be computed in each PWMSYNC interrupt service routine, there is a larger computational burden on the DSP in the double update mode.

Width of the PWMSYNC Pulse: PWMSYNCWT Register

The PWM controller of the ADMC(F)340 produces an internal PWM synchronization pulse at a rate equal to the PWM switching frequency in single update mode and at twice the PWM frequency in the double update mode. This PWMSYNC synchronizes the operation of the PWM unit with the A/D converter system. The width of this PWMSYNC pulse is programmable by the *PWMSYNCWT* Register. The width of the PWMSYNC pulse, $T_{PWMSYNC}$, is given by:

$$T_{PWMSYNC} = T_{CK} \times \left(PWMSYNCWT + 1\right)$$

which means that the width of the pulse is programmable from T_{CK} to 256 T_{CK} (corresponding to 50 ns to 12.8 μs for a CLKOUT rate of 20 MHz). Following a reset, the PWMSYNCWT Register contains 0x27 (= 39) so that the default PWMSYNC width is 2.0 μs.

PWM Duty Cycles: PWMCHA, PWMCHB, PWMCHC Registers

The duty cycles of the six PWM output signals are controlled by the three duty cycle registers, PWMCHA, PWMCHB, and PWMCHC. The integer value in the register PWMCHA controls the duty cycle of the signals on AH and AL. PWMCHB controls the duty cycle of the signals on BH and BL, and PWMCHC controls the duty cycle of the signals on CH and CL. The duty cycle registers are programmed in integer counts of the fundamental time unit, T_{CK}, and define the desired on-time of the high side PWM signal produced by the three-phase timing unit over half the PWM period. The switching signals produced by the three-phase timing unit are also adjusted to incorporate the programmed dead time value in the PWMDT Register.

The PWM is center-based. This means that in single update mode, the resulting output waveforms are symmetrical and centered in the PWMSYNC period. Figure 7 presents a typical PWM timing diagram illustrating the PWM-related registers' (PWMCHA, PWMTM, PWMDT, and PWMSYNCWT) control over the waveform timing in both half cycles of the PWM period. The magnitude of each parameter in the timing diagram is determined by multiplying the integer value in each register by T_{CK} (typically 50 ns). It may be seen in the timing diagram how dead time is incorporated into the waveforms by moving the switching edges away from the original values set in the PWMCHA Register.

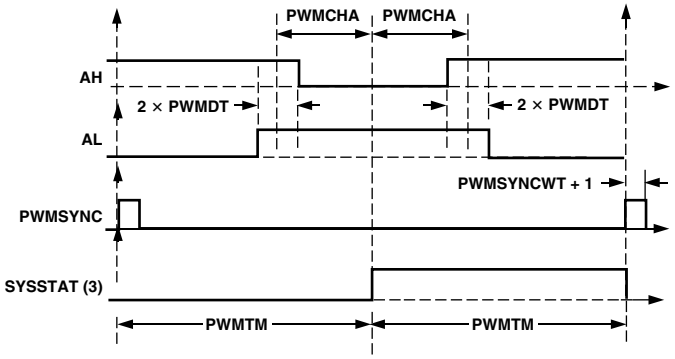


Figure 7. Typical PWM Outputs of Three-Phase Timing Unit in Single Update Mode

Each switching edge is moved by an equal amount (PWMDT × T_{CK}) to preserve the symmetrical output patterns. The PWMSYNC pulse, whose width is set by the PWMSYNCWT Register, is also shown. Bit 3 of the SYSSTAT Register indicates which half cycle is active. This can be useful in double update mode, to be discussed later in this data sheet.

The resultant on-times of the PWM signals shown in Figure 5 may be written as:

$$T_{AH} = 2 \times (PWMCHA - PWMDT) \times T_{CK}$$

$$T_{AL} = 2 \times (PWMTM - PWMCHA - PWMDT) \times T_{CK}$$

The corresponding duty cycles are:

$$d_{AH} = \frac{T_{AH}}{T_S} = \frac{PWMCHA - PWMDT}{PWMTM}$$

$$d_{AL} = \frac{T_{AL}}{T_S} = \frac{PWMTM - PWMCHA - PWMDT}{PWMTM}$$

Obviously, negative values of T_{AH} and T_{AL} are not permitted because the minimum permissible value is zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is T_S, corresponding to a 100% duty cycle.

The output signals from the timing unit for operation in double update mode are shown in Figure 8. This illustrates a completely general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. Of course, the same value for any or all of these quantities could be used in both halves of the PWM cycle. However, it can be seen that there is no guarantee that symmetrical PWM signals will be produced by the timing unit in this double update mode. Additionally, it is seen that the dead time is inserted into the PWM signals in the same way as in the single update mode.

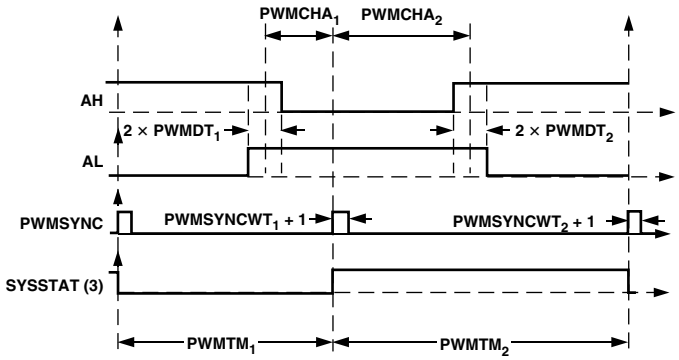


Figure 8. Typical PWM Outputs of Three-Phase Timing Unit in Double Update Mode

In general, the on-times of the PWM signals in double update mode are defined by:

$$T_{AH} = (PWMCHA_1 + PWMCHA_2 - PWMDT_1 - PWMDT_2) \times T_{CK}$$

$$T_{AL} = (PWMTM_1 + PWMTM_2 - PWMCHA_1 - PWMCHA_2 - PWMDT_1 - PWMDT_2) \times T_{CK}$$

$$d_{AH} = \frac{T_{AH}}{T_S}$$

$$= \frac{PWMCHA_1 + PWMCHA_2}{PWMTM_1 + PWMTM_2}$$

$$- \frac{PWMDT_1 + PWMDT_2}{PWMTM_1 + PWMTM_2}$$

$$d_{AL} = \frac{T_{AL}}{T_S}$$

$$= \frac{\left(PWMTM_1 + PWMTM_2 + PWMCHA_1\right)}{PWMTM_1 + PWMTM_2}$$

$$- \frac{\left(PWMCHA_2 + PWMDT_1 + PWMDT_2\right)}{PWMTM_1 + PWMTM_2}$$

Because of the completely general case in double update mode, the switching period is given by:

$$T_S = \left(PWNMTM_1 + PWMTM_2\right) \times T_{CK}$$

Again, the values of T_{AH} and T_{AL} are constrained to lie between zero and T_S.

PWM signals similar to those illustrated in Figures 7 and 8 can be produced on the BH, BL, CH, and CL outputs by programming the PWMCHB and PWMCHC Registers in a manner identical to that described for PWMCHA.

The PWM controller does not produce any PWM outputs until all of the PWMTM, PWMCHA, PWMCHB, and PWMCHC Registers have been written to at least once. After these registers have been written to, the counters in the three-phase timing unit are enabled. Writing to these registers also starts the main PWM timer. If, during initialization, the PWMTM Register is written to before the PWMCHA, PWMCHB, and PWMCHC Registers, the first PWMSYNC pulse (and interrupt if enabled) will be generated ($1.5 \times T_{CK} \times$ PWMTM) seconds after the initial write to the PWMTM Register in single update mode. In double update mode, the first PWMSYNC pulse will be generated ($T_{CK} \times$ PWMTM) seconds after the initial write to the PWMTM Register in single update mode.

Effective PWM Resolution

In single update mode, the same values of PWMCHA, PWMCHB, and PWMCHC are used to define the on-times in both half cycles of the PWM period. As a result, the effective resolution of the PWM generation process is 2 T_{CK} (or 100 ns for a 20 MHz CLKOUT) since incrementing one of the duty cycle registers by 1 changes the resultant on-time of the associated PWM signals by T_{CK} in each half period (or 2 T_{CK} for the full period).

In double update mode, improved resolution is possible since different values of the duty cycle registers are used to define the on-times in both the first and second halves of the PWM period. As a result, it is possible to adjust the on-time over the whole period in increments of T_{CK}. This corresponds to an effective PWM resolution of T_{CK} in double update mode (or 50 ns for a 20 MHz CLKOUT).

Table IV. Fundamental Characteristics of PWM Generation Unit of ADMC(F)340

16-BIT PWM TIMER

Parameter	Min	Typ	Max	Unit
Counter Resolution		16		Bits
Edge Resolution (Single Update Mode)		100		ns
Edge Resolution (Double Update Mode)		50		ns
Programmable Dead Time Range	0		102	µs
Programmable Dead Time Increments		100		ns
Programmable Pulse Deletion Range		0	51	µs
Programmable Pulse Deletion Increments		50		ns
PWM Frequency Range	153			Hz
PWMSYNC Pulsewidth (T_{CRST})	0.05		12.8	µs
Gate Drive Chop Frequency Range	0.02		5	MHz

Table V. Achievable PWM Resolution in Single and Double Update Modes

Resolution (Bit)	Single Update Mode PWM Frequency (kHz)	Double Update Mode PWM Frequency (kHz)
8	39.1	78.1
9	19.5	39.1
10	9.8	19.5
11	4.9	9.8
12	2.4	4.9

Minimum Pulsewidth: PWMPD Register

In many power converter switching applications, it is desirable to eliminate PWM switching pulses shorter than a certain width. It takes a finite time to both turn on and turn off modern power semiconductor devices. Therefore, if the width of any of the PWM pulses is shorter than some minimum value, it may be desirable to completely eliminate the PWM switching for that particular cycle.

The allowable minimum on-time for any of the six PWM outputs for half a PWM period that can be produced by the PWM controller may be programmed using the PWMPD Register. The minimum on-time is programmed in increments of T_{CK} so that the minimum on-time produced for any half PWM period, T_{MIN}, is related to the value in the *PWMPD* Register by:

$$T_{MIN} = PWMPD \times T_{CK}$$

A *PWMPD* value of 0x002 defines a permissible minimum on-time of 100 ns for a 20 MHz CLKOUT.

In each half cycle of the PWM, the timing unit checks the on-time of each of the six PWM signals. If any of the times are found to be less than the value specified by the PWMPD Register, the corresponding PWM signal is turned OFF for the entire half period, and its complementary signal is turned completely ON.

Consider the example where PWMTM = 200, PWMCHA = 5, PWMDT = 3, and PWMPD = 10 with a CLKOUT of 20 MHz, while operating in single update mode. For this case, the PWM switching frequency is 50 kHz and the dead time is 300 ns. The minimum permissible on-time of any PWM signal over one-half of any period is 500 ns. Clearly, for this example, the dead time adjusted on-time of the AH signal for one-half a PWM period is $(5 - 3) \times 50$ ns = 100 ns. Because this is less than the minimum permissible value, output AH of the timing unit will remain OFF (0% duty cycle). Additionally, the AL signal will be turned ON for the entire half period (100% duty cycle).

Output Control Unit: PWMSEG Register

The operation of the output control unit is managed by the 9-bit read/write PWMSEG Register. This register sets two distinct features of the output control unit that are directly useful in the control of ECM or BDCM.

The PWMSEG Register contains three crossover bits, one for each pair of PWM outputs. Setting Bit 8 of the PWMSEG Register enables the crossover mode for the AH/AL pair of PWM signals; setting Bit 7 enables crossover on the BH/BL pair of PWM signals; and setting Bit 6 enables crossover on the CH/CL pair of PWM signals. If crossover mode is enabled for any pair of PWM signals, the high side PWM signal from the timing unit (for example, AH) is diverted to the associated low side output of the output control unit so that the signal will ultimately appear at the AL pin. Of course, the corresponding low side output of the timing unit is also diverted to the complementary high side output of the output control unit so that the signal appears at Pin AH. Following a reset, the three crossover bits are cleared so that the crossover mode is disabled on all three pairs of PWM signals.

The PWMSEG Register also contains six bits (Bits 0 to 5) that can be used to individually enable or disable each of the six PWM outputs. If the associated bit of the PWMSEG Register is set, the corresponding PWM output is disabled regardless of the value of the corresponding duty cycle register. This PWM output signal will remain in the OFF state as long as the corresponding enable/disable bit of the PWMSEG Register is set. The PWM output enable function gates the crossover function. After a reset, all six enable bits of the PWMSEG Register are cleared, thereby enabling all PWM outputs by default.

In a manner identical to the duty cycle registers, the PWMSEG is latched on the rising edge of the PWMSYNC signal so that changes to this register only become effective at the start of each PWM cycle in single update mode. In double update mode, the PWMSEG Register can also be updated at the midpoint of the PWM cycle.

In the control of an ECM, only two inverter legs are switched at any time, and often the high side device in one leg must be switched ON at the same time as the low side driver in a second leg. Therefore, by programming identical duty cycles for two PWM channels (for example, let PWMCHA = PWMCHB) and setting Bit 7 of the PWMSEG Register to crossover the BH/BL pair of PWM signals, it is possible to turn ON the high side switch of Phase A and the low side switch of Phase B at the same time. In the control of an ECM, one inverter leg (Phase C in this example) is disabled for a number of PWM cycles. This disable may be implemented by disabling both the CH and CL PWM outputs by setting Bits 0 and 1 of the PWMSEG Register. This is illustrated in Figure 7, where it can be seen that both the AH and BL signals are identical, because PWMCHA = PWMCHB, and the crossover bit for Phase B is set. In addition, the other four signals (AL, BH, CH, and CL) have been disabled by setting the appropriate enable/disable bits of the PWMSEG Register. For the situation illustrated in Figure 9, the appropriate value for the PWMSEG Register is 0x00A7. In ECM operation, because each inverter leg is disabled for a certain period of time, the PWMSEG Register is changed based upon the position of the rotor shaft (motor commutation).

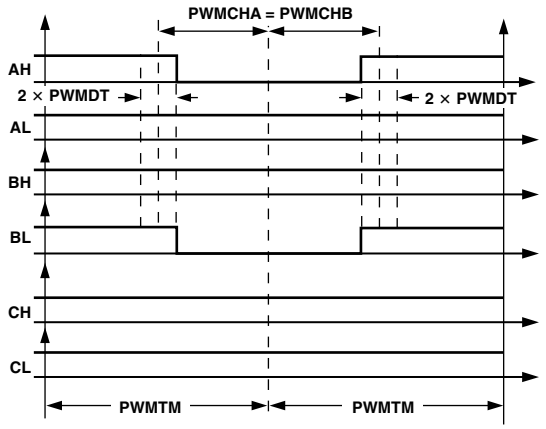


Figure 9. An example of PWM signals suitable for ECM control. PWMCHA = PWMCHB, BH/BL are a crossover pair. AL, BH, CH, and CL outputs are disabled. Operation is in single update mode.

Gate Drive Unit: PWMGATE Register

The gate drive unit of the PWM controller adds features that simplify the design of isolated gate drive circuits for PWM inverters. If a transformer-coupled power device gate drive amplifier is used, the active PWM signal must be chopped at a high frequency. The PWMGATE Register allows the programming of this high frequency chopping mode. The chopped active PWM signals may be required for the high side drivers only, for the low side drivers only, or for both the high side and low side switches. Therefore, independent control of this mode for both high side and low side switches is included with two separate control bits in the PWMGATE Register.

Typical PWM output signals with high frequency chopping enabled on both high side and low side signals are shown in Figure 10. Chopping of the high side PWM outputs (AH, BH, and CH) is enabled by setting Bit 8 of the PWMGATE Register. Chopping of the low side PWM outputs (AL, BL, and CL) is enabled by setting Bit 9 of the PWMGATE Register. The high chopping frequency is controlled by the 8-bit word (GDCLK) written to Bits 0 to 7 of the PWMGATE Register. The period and the frequency of this high frequency carrier are:

$$T_{CHOP} = \left[4 \times \left(GDCLK + 1\right)\right] \times T_{CK}$$

$$f_{CHOP} = \frac{f_{CLKOUT}}{\left[4 \times \left(GDCLK + 1\right)\right]}$$

The *GDCLK* value may range from 0 to 255, corresponding to a programmable chopping frequency rate from 19.5 kHz to 5 MHz for a 20 MHz CLKOUT rate. The gate drive features must be programmed before operation of the PWM controller and typically are not changed during normal operation of the PWM controller. Following a reset, by default, all bits of the PWMGATE Register are cleared so that high frequency chopping is disabled.

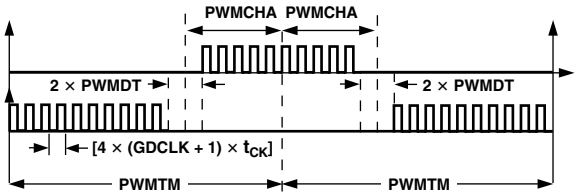


Figure 10. Typical PWM signals with high frequency gate chopping enabled on both high side and low side switches. (GDCLK is the integer equivalent of the value in Bits 0 to 7 of the PWMGATE Register.)

PWM Polarity Control, PWMPOL Pin

The polarity of the PWM signals produced at the output pins AH to CL may be selected in hardware by the PWMPOL pin. Connecting the PWMPOL pin to DGND selects active low PWM outputs, such that a low level is interpreted as a command to turn on the associated power device. Conversely, connecting the PWMPOL pin to V_{DD} selects active high PWM and the associated power devices are turned ON by a high level at the PWM outputs. There is an internal pull-up on the PWMPOL pin, so that if this pin becomes disconnected (or is not connected), active HI PWM will be produced. The level on the PWMPOL pin may be read from Bit 2 of the SYSSTAT Register, where a zero indicates a measured low level at the PWMPOL pin.

SWITCHED RELUCTANCE MODE

The PWM block of the ADMC(F)340 contains a switched reluctance (SR) mode that is controlled by the $\overline{\text{PWMSR}}$ pin. The switched reluctance mode is enabled by connecting the $\overline{\text{PWMSR}}$ pin to DGND. In this SR mode, the low side PWM signals from the three-phase timing unit assume permanently ON states, independent of the value written to the duty-cycle registers. The duty cycles of the high side PWM signals from the timing unit are still determined by the three duty cycle registers. Using the crossover feature of the output control unit, it is possible to divert the permanently ON PWM signals to either the high side or low side outputs. This mode is necessary because in the typical power converter configuration for switched or variable reluctance motors, the motor winding is connected between the two power switches of a given inverter leg. Therefore, in order to build up current in the motor winding, it is necessary to turn on both switches at the same time. Typical active low PWM signals during operation in SR mode are shown in Figure 8 for operation in double update mode. It is clear that the three low side signals (AL, BL, and CL) are permanently ON and the three high side signals are modulated in the usual manner so that the corresponding high side power switches are switched between the ON and OFF states. The SR mode can only be enabled by connecting the $\overline{\text{PWMSR}}$ pin to GND. There are no software means by which this mode can be enabled. There is an internal pull-up resistor on the $\overline{\text{PWMSR}}$ pin so that if this pin is left unconnected or becomes disconnected, the SR mode is disabled. Of course, the SR mode is disabled when the $\overline{\text{PWMSR}}$ pin is tied to V_{DD}.

PWM Shutdown

In the event of external fault conditions, it is essential that the PWM system be instantaneously shut down. Two methods of sensing a fault condition are provided by the ADMC(F)340. For the first method, a low level on the $\overline{\text{PWMTRIP}}$ pin initiates an instantaneous, asynchronous (independent of DSP clock) shutdown of the PWM controller. This places all six PWM outputs in the OFF state, disables the PWMSYNC pulse and associated interrupt signal, and generates a $\overline{\text{PWMTRIP}}$ interrupt signal. The $\overline{\text{PWMTRIP}}$ pin has an internal pull-down resistor so that even if the pin becomes disconnected, the PWM outputs will be disabled. The state of the $\overline{\text{PWMTRIP}}$ pin can be read from Bit 0 of the SYSSTAT Register.

The second method for detecting a fault condition is through the I_{SENSE} pins of the analog block of the ADMC(F)340. When the voltage at any of the I_{SENSE} pins exceeds the trip threshold (high or low), $\overline{\text{PWMTRIP}}$ will be internally pulled low. The negative edge of the internal $\overline{\text{PWMTRIP}}$ will generate a shutdown in the same manner as a negative edge on pin $\overline{\text{PWMTRIP}}$.

In addition, it is possible through software to initiate a PWM shutdown by writing to the 1-bit read/write PWMSWT Register (0x2061). Writing to this bit generates a PWM shutdown in a manner identical to the $\overline{\text{PWMTRIP}}$ or I_{SENSE} pins. Following a PWM shutdown, it is possible to determine if the shutdown was generated from hardware or software by reading the same PWMSWT Register. Reading this register also clears it.

Restarting the PWM after a fault condition is detected requires clearing the fault and reinitializing the PWM. Clearing the fault requires that $\overline{\text{PWMTRIP}}$ returns to a high state. After the fault has been cleared, the PWM can be restarted by writing to registers PWMTM, PWMCHA, PWMCHB, and PWMCHC. After the fault is cleared and the PWM Registers are initialized, internal timing of the three-phase timing unit will resume, and the new duty cycle values will be latched on the next rising edge of PWMSYNC.

PWM Registers

The configuration of the PWM Registers is described in Figure 22. The parameters of the PWM block are described in Table IV.

ADC OVERVIEW

The ADC of the ADMC(F)340 is based upon the single slope conversion technique. This approach offers an inherently monotonic conversion process within the noise and stability of its components, and there will be no missing codes.

The single slope technique has been adopted on the ADMC(F)340 for four channels that are simultaneously converted. Refer to Figure 11 for the functional schematic of the ADC. The main inputs (V1, V2, and V3) are directly connected to the ADC converter through three front end blocks. Figure 14 shows the block diagram of a single front end block. Each front end block has a bipolar current amplifier (gain = –2.5) designed to acquire the voltage on a current-sensing resistor, whose voltage can be either positive or negative with respect to the power supply ground rail.

The fourth channel has been configured with a serially connected 8-to-1 multiplexer. Table VI shows the multiplexer input selection codes. One of these auxiliary multiplexed channels is used to acquire the internal voltage reference (V_{REF}) for calibration purposes.

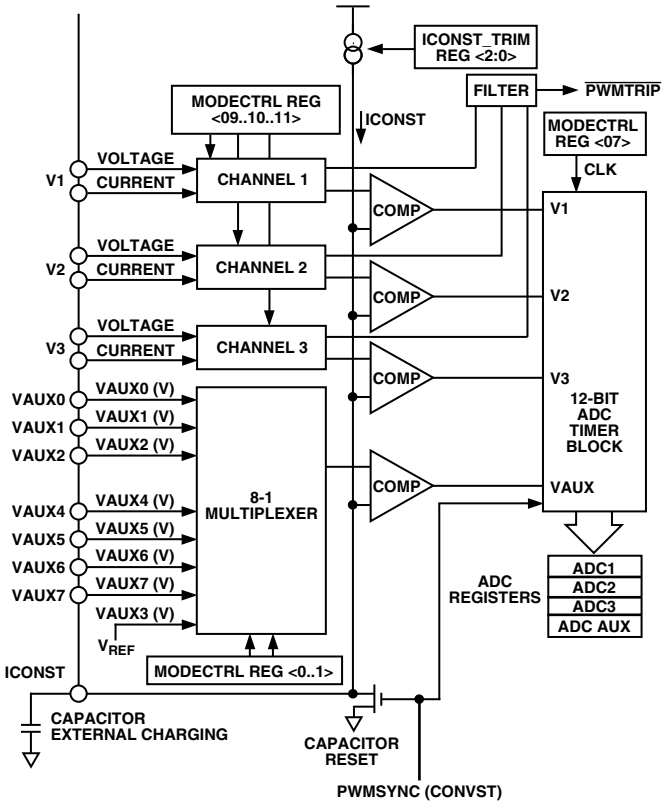


Figure 11. ADC Overview

Single Slope ADC Operations

Comparing each ADC input to a reference ramp voltage and timing the comparison of the two signals performs the conversion process. The actual conversion point is the time point intersection of the input voltage and the ramp voltage (V_C) as shown in Figure 12. This time is converted to counts by the 12-bit ADC Timer Block and is stored in the ADC registers. The ramp voltage used to perform the conversion is generated by driving a fixed current into an off-chip capacitor, where the capacitor voltage is:

$$V_C = \left(I/C\right) \times t$$

Following reset, V_C = 0 at t = 0. This reset and the start of the conversion process are initiated by the PWMSYNC pulse, as shown in Figure 12. The width of the PWMSYNC pulse is controlled by the PWMSYNCWT Register and should be programmed according to Figure 12 to ensure complete resetting.

In order to compensate for IC process manufacturing tolerances (and to adjust for capacitor tolerances), the current source of the ADMC(F)340 is software programmable. The software setting of the magnitude of the ICONST current generator is accomplished by selecting one of eight steps over approximately 20% current range.

Table VI. ADC Auxiliary Channel Selection

Select	MODECTRL(5) ADCMUX	MODECTRL(1) ADCMUX1	MODECTRL(0) ADCMUX0
VAUX0	0	0	0
VAUX1	0	0	1
VAUX2	0	1	0
VAUX3 Calibration (V_{REF})	0	1	1
VAUX4	1	0	0
VAUX5	1	0	1
VAUX6	1	1	0
VAUX7	1	1	1

Table VII. Port A Multiplexing

PORTA Pin	First Alternate Function (Peripheral)	Second Alternate Function (Peripheral)
PORTA8	AUX0 (Auxiliary PWM Output)	CLKOUT (System CLOCK)
PORTA7	AUX1 (Auxiliary PWM Output)	PWMSYNC (PWM)
PORTA6	DR1 (Data Receive SPORT1)	None
PORTA5	FL1 (Flag Out SPORT1)	DT1 (Data Transmit SPORT1)
PORTA4	SCLK1 (Serial Clock SPORT1)	SCLK0 (Serial Clock SPORT0)
PORTA3	TFS0 (Transmit Frame Sync SPORT0)	None
PORTA2	RFS0 (Receive Frame Sync SPORT0)	None
PORTA1	DT0 (Data Transmit SPORT0)	None
PORTA0	DR0 (Data Receive SPORT0)	None

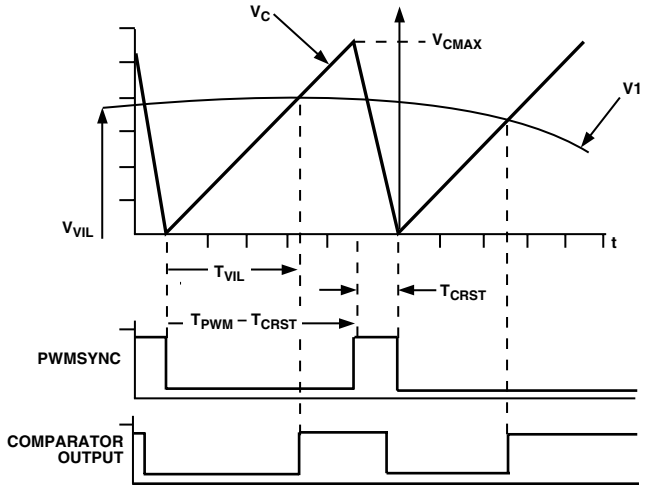


Figure 12. Analog Input Block Operation

The ADC system consists of four comparators and a single timer that may be clocked at either the DSP rate or half the DSP rate, depending on the setting of the ADCCNT bit (Bit 7) of the MODECTRL Register. When this bit is cleared, the timer counts at a slower rate of CLKIN. When this bit is set, the timer counts at CLKOUT or twice the rate of CLKIN. ADC1, ADC2, ADC3, and ADCAUX are the registers that capture the conversion times, which are the timer values when the associated comparator trips.

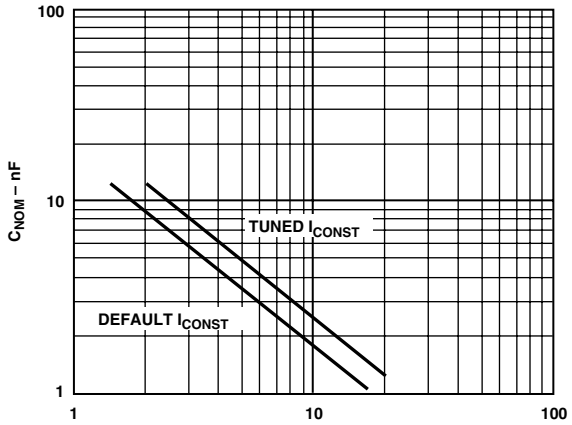


Figure 13. Timing Capacitor Selection

ADC Resolution

The ADC is intrinsically linked to the PWM block through the PWMSYNC pulse controlling the ADC conversion process. Because of this link, the effective resolution of the ADC is a function of both the PWM switching frequency and the rate at which the ADC counter timer is clocked. For a CLKOUT period of T_{CK} and a PWM period of T_{PWM}, the maximum count of the ADC is given by:

$$Max\ Count = \min\left(4095, \left(T_{PWM} - T_{CRST}\right) / 2\,T_{CK}\right)$$

$$for\ MODECTRL\ Bit\ 7 = 0$$

$$Max\ Count = \min\left(4095, \left(T_{PWM} - T_{CRST}\right) / T_{CK}\right)$$

$$for\ MODECTRL\ Bit\ 7 = 1$$

Where T_{PWM} is equal to the PWM period if operating in single update mode, or it is equal to half that period if operating in double update mode. For an assumed CLKOUT frequency of 20 MHz and PWMSYNC pulsewidth of 2.0 µs, the effective resolution of the ADC block is tabulated for various PWM switching frequencies in Table VIII.

Table VIII. ADC Resolution Examples

PWM Frequency (kHz)	MODECTRL[7] = 0 Max Count	MODECTRL[7] = 0 Effective Resolution	MODECTRL[7] = 1 Max Count	MODECTRL[7] = 1 Effective Resolution
2.4	4095	12	4095	12
4	2480	>11	4095	12
8	1230	>10	2460	>11
18	535	>9	1070	>10
25	380	>8	760	>9

Programmable Current Source

The ADMC(F)340 has an internal current source that is used to charge an external capacitor, generating the voltage ramp used for conversion. The magnitude of the output of the current source circuit is subject to manufacturing variations and can vary from one device to the next. Therefore, the ADMC(F)340 includes a programmable current source whose output can always be tuned to within 5% of the target 100 µA. A 3-bit register, ICONST_TRIM, allows the user to make this adjustment. The output current is proportional to the value written to the register: 0x0 produces the minimum output, and 0x7 produces the maximum output. The default value of ICONST_TRIM after reset is 0x0.

Suggested implementations of the calibration routine are provided through Application Notes and code that can be found by visiting www.analog.com/motorcontrol.

Charging Capacitor Selection

The charging capacitor value is selected based on the sample (PWM) frequency desired. Too small a capacitor value will reduce the available resolution of the ADC by having the ramp voltage rise rapidly and convert too quickly, not utilizing all possible counts available in the PWM cycle. Too large a capacitor may not convert in the available PWM cycle returning 0x000. To select a charging capacitor, use Figure 13, select the sampling frequency desired, determine if the current source is to be tuned to a nominal 100 µA or left in the default (0x0 code) trim state, then determine the proper charge capacitor off the appropriate curve.

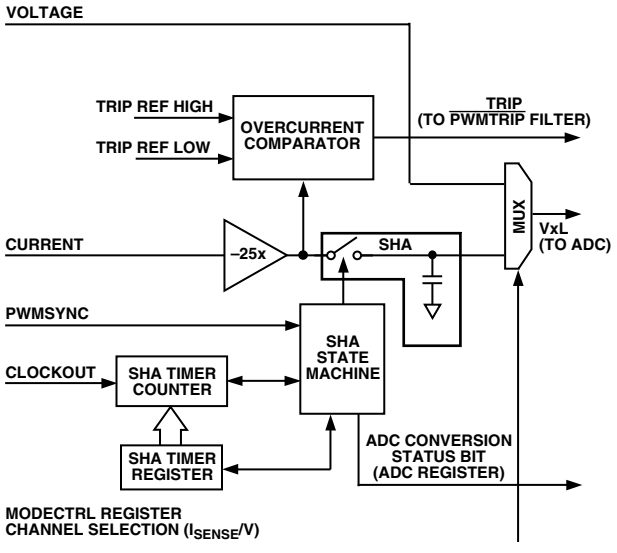


Figure 14. Analog Front End Block Diagram

Analog Front End

The main analog inputs of the ADMC(F)340 (I_{SENSE1} through I_{SENSE3}) are connected to the ADC converter through three front end blocks. Figure 14 shows the block diagram of a single analog front end.

Each analog front end has two analog inputs: voltage and current. A 2-to-1 multiplexer selects which input will be converted; the multiplexer selection is determined by the MODECTRL Register.

The current input (I_{SENSE}) is amplified through a bipolar amplifier (Gain –2.5). There is an output offset that matches the amplifier output signal range to the input signal range of the A/D converter. The amplifier has a built-in overcurrent and open circuit protection. The overcurrent protection shuts down the PWM block when the voltage at any of the I_{SENSE} pins exceeds the trip threshold (high or low). The open circuit protection shuts down the PWM block when any of the I_{SENSE} inputs is in high impedance (for example the current sense resistor or the current transducer is disconnected). The shut-down signals generated by the amplifiers are then OR-ed and filtered in order to avoid spurious trip caused by the switching of the power devices. The amplifier is followed by a sample-and-hold amplifier (SHA). The SHA time is user-programmable through the SHA Timer Register. The sampling time is set as a delay from the rising edge of the PWMSYNC signal and is calculated as:

$$T_{SAMPLE} = (SHA\_CNT + 2) \times T_{CK}$$

The SHA Timer Counter has a minimum reload value of 0x0003, which ensures a minimum settling time of the SHA output in case the user is programming the SHA Timer Register to a value smaller than 0x0003. This means that the sampling time is programmable from 5 T_{CK} to 65535 T_{CK} (corresponding to 250 ns to 3.28 ms for a CLKOUT rate of 20 MHz). The sampling time, however, is limited to the rising edge of the following PWMSYNC cycle. Each channel has an independent amplifier, SHA, and SHA timing unit/state machine. Figure 15 shows a conversion sequence of a single channel.

At the beginning of the cycle N (rising edge of PWMSYNC signal (1)), the Timer Counter is loaded with the value contained in the SHA_CNT Register. After the Timer Counter has been reloaded, it starts counting down at the CLKOUT rate; in this phase, the SHA state-machine forces the SHA in TRACK (sample) status.

When the counter reaches the value of 0x0000 (after the time T_{SAMPLE} from the rising edge of PWMSYNC), the SHA state-machine forces the SHA in HOLD status.

The conversion of the sampled value is then taking place in the cycle N + 1 (from (4) to (5)) in Figure 15 and the result of the conversion is available on the ADC Register at the cycle N + 2 (rising edge of PWMSYNC (5)).

On cycle N + 2, the reload value of the Timer Counter exceeds the period of the PWMSYNC signal. In this case, the SHA statemachine forces the SHA in HOLD status at the rising edge of PWMSYNC of the next cycle (7). The conversion then takes place on cycle N + 3 and the conversion result is available on the ADC Register at the cycle N + 4 (rising edge of PWMSYNC (9)).

During the acquire phase (the PWMSYNC cycle during the sampling of the input value), the conversion takes place. However, the value on the ADC Register is not considered valid. This condition is signaled by the ADC by setting the LSB of the ADC Register to high.

On cycle N + 4, at the rising edge of the PWMSYNC signal (9), the Timer Counter is reloaded with a value smaller than the PWMSYNC pulsewidth. In this case, the SHA samples within the PWMSYNC pulsewidth and the conversion takes place in the same PWMSYNC cycle (from (10) to (11)).

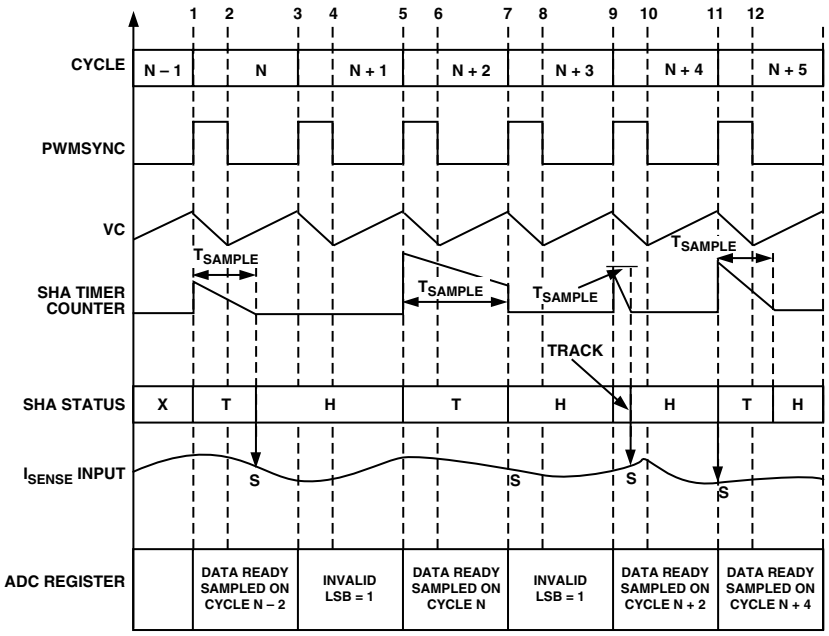


Figure 15. ADC Conversion Sequence of a Current Input

Table IX. Fundamental Characteristics of Auxiliary PWM Timer of ADMC(F)340

Parameter	Test Conditions	Min	Typ	Max	Unit
Resolution			16		Bits
PWM Frequency	10 MHz CLKIN	0.152			MHz

AUXILIARY PWM TIMERS

Overview

The ADMC(F)340 provides two variable frequency, variable duty cycle, 16-bit, auxiliary PWM outputs that are available at the AUX1 and AUX0 pins. When enabled, these auxiliary PWM outputs can be used to provide switching signals to other circuits in a typical motor control system such as power factor corrected front-end converters or other switching power converters. Alternatively, by adding a suitable filter network, the auxiliary PWM output signals can be used as simple single-bit digital-to-analog converters, which is shown in Figure 16. The auxiliary PWM system of the ADMC(F)340 can operate in two different modes: independent mode or offset mode. The operating mode of the auxiliary PWM system is controlled by Bit 8 of the MODECTRL Register. Setting Bit 8 of the MODECTRL Register places the auxiliary PWM system in the independent mode. In this mode, the two auxiliary PWM generators are completely independent and separate switching frequencies and duty cycles may be programmed for each auxiliary PWM output. In this mode, the 16-bit AUXTM0 Register sets the switching frequency of the signal at the AUX0 output pin. Similarly, the 16-bit AUXTM1 Register sets the switching frequency of the signal at the AUX1 pin. The fundamental time increment for the auxiliary PWM outputs is twice the DSP instruction rate (or 2 T_{CK}) and the corresponding switching periods are given by:

$$T_{AUX0} = 2 \times (AUXTM0 + 1) \times T_{CK}$$

$$T_{AUX1} = 2 \times (AUXTM1 + 1) \times T_{CK}$$

Since the values in both AUXTM0 and AUXTM1 can range from 0 to 0xFFFF, the achievable switching frequency of the auxiliary PWM signals may range from 152.59 Hz to 10 MHz for a CLKOUT frequency of 20 MHz. The on-time of the two auxiliary PWM signals is programmed by the two 16-bit *AUXCH*0 and *AUXCH*1 Registers, according to:

$$T_{ON,\ AUX0} = 2 \times (AUXCH0) \times T_{CK}$$

$$T_{ON,\ AUX1} = 2 \times (AUXCH1) \times T_{CK}$$

so that output duty cycles from 0% to 100% are possible. Duty cycles of 100% are produced if the on-time value exceeds the period value. Typical auxiliary PWM waveforms in independent mode are shown in Figure 17(a). When Bit 8 of the MODECTRL Register is cleared, the auxiliary PWM channels are placed in offset mode. In offset mode, the switching frequency of the two signals on the AUX0 and AUX1 pins are identical and controlled by AUXTM0 in a manner similar to that previously described for independent mode. In addition, the on-times of both the AUX0 and AUX1 signals are controlled by the AUXCH0 and AUXCH1 Registers as before.

However in this mode, the AUXTM1 Register defines the offset time from the rising edge of the signal on the AUX0 pin to that on the AUX1 pin according to:

$$T_{OFFSET} = 2 \times (AUXTM1 + 1) \times T_{CK}$$

For correct operation in this mode, the value written to the AUXTM1 Register must be less than the value written to the AUXTM0 Register. Typical auxiliary PWM waveforms in offset mode are shown in Figure 17(b). Again, duty cycles from 0% to 100% are possible in this mode.

In both operating modes, the resolution of the auxiliary PWM system is 16 bits only at the minimum switching frequency (AUXTM0 = AUXTM1 = 65535 in independent mode, AUXTM0 = 65535 in offset mode). Obviously, as the switching frequency is increased, the resolution is reduced.

Values can be written to the auxiliary PWM Registers at any time. However, new duty cycle values written to the AUXCH0 and AUXCH1 Registers only become effective at the start of the next cycle. Writing to the AUXTM0 or AUXTM1 Registers causes the internal timers to be reset to 0 and new PWM cycles to begin. By default following a reset, Bit 8 of the MODECTRL Register is cleared, thus enabling offset mode. In addition, the registers AUXTM0 and AUXTM1 default to 0xFFFF, corresponding to the minimum switching frequency and zero offset. The on-time registers AUXCH0 and AUXCH1 default to 0x0000.

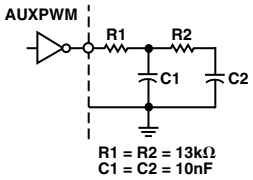
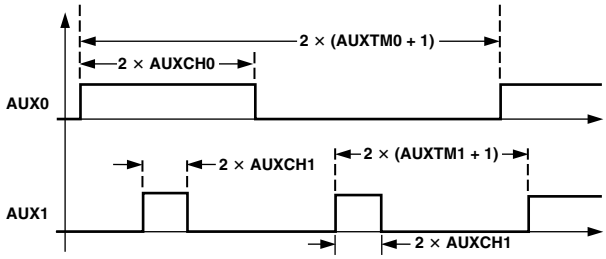


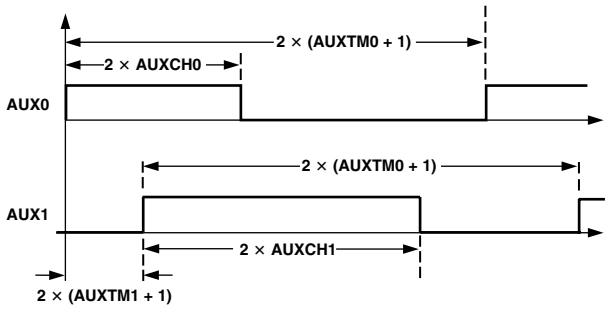
Figure 16. Auxiliary PWM Output Filter

Auxiliary PWM Interface, Registers, and Pins

The registers of the auxiliary PWM system are summarized in Figure 26.



17a. Typical Auxiliary PWM Signal (All Times in Increments of T_{CK}) – Independent Mode



17b. Typical Auxiliary PWM Signal (All Times in Increments of T_{CK}) – Offset Mode

WATCHDOG TIMER

The ADMC(F)340 incorporates a watchdog timer that can perform a full reset of the DSP and motor control peripherals in the event of a software error. The watchdog timer is enabled by writing a timeout value to the 16-bit WDTIMER Register. The timeout value represents the number of CLKIN cycles required for the watchdog timer to count down to zero. When the watchdog timer reaches zero, a full DSP core and motor control peripheral reset is performed. In addition, Bit 1 of the SYSSTAT Register is set so that after a watchdog reset, the ADMC(F)340 can determine that the reset was due to the timeout of the watchdog timer and not an external reset. Following a watchdog reset, Bit 1 of the SYSSTAT Register may be cleared by writing zero to the WDTIMER Register. This clears the status bit but does not enable the watchdog timer.

On reset, the watchdog timer is disabled and is enabled only when the first timeout value is written to the WDTIMER Register. To prevent the watchdog timer from timing out, the user must write to the WDTIMER Register at regular intervals (shorter than the programmed WDTIMER period value). On all but the first write to WDTIMER, the particular value written to the register is unimportant, since writing to WDTIMER simply reloads the first value written to this register.

PROGRAMMABLE DIGITAL INPUT/OUTPUT

The ADMC(F)340 has 25 programmable digital input/output (PIO) pins. These pins are organized in two separate ports: PORTA (nine pins) and PORTB (16 pins).

The nine pins of PORTA are multiplexed with other on-chip peripheral functions. PORTB has 16 pins that are dedicated to the digital I/O function only.

Each bit of PORTA can be individually selected as PIO or the alternate function through PORTA_SELECT Register. Bit 0 of PORTA_SELECT controls the operation of the PA0 Pin, Bit 1 controls the operation of PA1 and so on. Setting the appropriate bit in the PORTA_SELECT Register causes the corresponding pin to be configured as PIO. Clearing the bit selects the alternate function of the corresponding pin. Following a power-on or reset, all bits of PORTA_SELECT are set such that PIO functionality is selected. The second alternate function of PA7 is selected by Bit 14 of the PORTA_SELCT Register. The second alternate function of PA8 is selected by Bit 15 of the PORTA_SELECT Register. The second alternate function of PA4 and PA5 is selected by Bit 4 of MODECTRL Register (SPORT1 Mode: Boot/UART).

When a pin is operating as PIO, its direction can be set through the corresponding bit of the data direction register (PORTA_DIR or PORTB_DIR).

Clearing any bit of the data direction register configures the corresponding PIO as input while setting the bit configures the PIO as output.

Following a power-on or reset, all bits or PORTA_DIR and PORTB_DIR are cleared, configuring all the PIO lines as inputs.

The data of the PIOs is controlled by the data registers (PORTA_DATA and PORTB_DATA). These registers can be used to read data from those PIOs configured as input and write data to those configured as outputs.

Each PIO can be individually programmed to be an interrupt source by setting the corresponding bit of the interrupt enable register (PORTA_INTEN and PORTB_INTEN). To generate an interrupt, the corresponding bit on the data register (PORTA_DATA and PORTB_DATA) must change state (high-to-low or low-to-high transition). The transition can be on the corresponding pin (PIO configured as input) or by writing into the corresponding bit of the data register (PIO configured as output).

Following a change of state on the data register on a PIO configured as interrupt source, the corresponding bit is set in the flag register (PORTA_FLAG and PORTB_FLAG) and a common PIO interrupt is generated.

Reading the flag register, it is possible to determine which PIO has generated the interrupt. Reading the flag register automatically clears all the bits of the register. Following a power-on or reset, all bits of the interrupt enable registers are cleared (no interrupt enabled).

Each PIO line has an internal pull-down resistor so that following a power-on or reset all the PIO lines will be read as logic lows if left unconnected.

Once a pin has been selected as PIO function, it can be set as input, output, and interrupt source (either configured as input or output).

PIO Registers

The configuration of all registers of the PIO system is shown at the end of the data sheet.

INTERRUPT CONTROL

The ADMC(F)340 can respond to 34 different interrupt sources with minimal overhead. Seven of these interrupts are internal DSP core interrupts and 27 are from the on-chip peripherals. The seven DSP core interrupts are SPORT0 receive and transmit, SPORT1 receive (or IRQ0) and transmit (or IRQ1), the internal timer, and two software interrupts. The Motor Control interrupts are the 25 PIOs and two from the PWM block (PWMSYNC pulse and $\overline{\text{PWMTRIP}}$). All the on-chip peripherals' interrupts are multiplexed into the DSP core via the peripheral $\overline{\text{IRQ2}}$ interrupt. They are also internally prioritized and individually maskable. The start address in the interrupt vector table for the ADMC(F)340 interrupt sources is shown in Table X. The interrupts are listed from highest priority to the lowest priority. The PWMSYNC interrupt is triggered by a low-to-high transition on the PWMSYNC pulse. The $\overline{\text{PWMTRIP}}$ interrupt is triggered on a high-to-low transition on the $\overline{\text{PWMTRIP}}$ pin. A PIO interrupt is detected on any change of state (high-to-low or low-to-high) on the PIO lines.

The entire interrupt control system of the ADMC(F)340 is configured and controlled by the IFC, IMASK, and ICNTL Registers of the DSP core and the IRQFLAG Register for the PWMSYNC

and $\overline{\text{PWMTRIP}}$ interrupts and PORTA_FLAG Register for the PIO interrupts.

Table X. Interrupt Vector Addresses

Interrupt Source	Interrupt Vector Address
$\overline{\text{PWMTRIP}}$	0x002C (Highest Priority)
Peripheral Interrupt ($\overline{\text{IRQ2}}$)	0x0004
PWMSYNC	0x000C
PIO	0x0008
Software Interrupt 1	0x0018
Software Interrupt 0	0x001C
SPORT0 Transmit Interrupt	0x0010
SPORT0 Receive Interrupt	0x0014
SPORT1 Transmit Interrupt (or $\overline{\text{IRQ1}}$)	0x0020
SPORT1 Receive Interrupt (or $\overline{\text{IRQ0}}$)	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt Masking

Interrupt masking (or disabling) is controlled by the IMASK Register of the DSP core. This register contains individual bits that must be set to enable the various interrupt sources. If any peripheral interrupt is to be enabled, the $\overline{\text{IRQ2}}$ interrupt enable bit (Bit 9) of the IMASK Register must be set. The configuration of the IMASK Register of the ADMC(F)340 is shown in Figure 29.

Interrupt Configuration

The IFC and ICNTL Registers of the DSP core control and configure the interrupt controller of the DSP core. The IFC Register is a 16-bit register that may be used to force and/or clear any of the eight DSP interrupts. Bits 0 to 7 of the IFC Register may be used to clear the DSP interrupts while Bits 8 to 15 can be used to force a corresponding interrupt. Writing to Bits 11 and 12 in IFC is the only way to create the two software interrupts. The ICNTL Register is used to configure the sensitivity (edge or level) of the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts and to enable/disable interrupt nesting. Setting Bit 0 of ICNTL configures the $\overline{\text{IRQ0}}$ as edge-sensitive, while clearing the bit configures it for level-sensitive. Bit 1 is used to configure the $\overline{\text{IRQ1}}$ interrupt and Bit 2 is used to configure the $\overline{\text{IRQ2}}$ interrupt. It is recommended that the $\overline{\text{IRQ2}}$ interrupt always be configured for level-sensitive since this ensures that no peripheral interrupts are lost. Setting Bit 4 of the ICNTL Register enables interrupt nesting. The configuration of both IFC and ICNTL Registers is shown in Figure 29.

INTERRUPT OPERATION

Following a reset, the ROM code on the ADMC(F)340 must copy a default interrupt vector table into program memory RAM from Addresses 0x0000 to 0x002F. Since each interrupt source has a dedicated four-word space in this vector table, it is possible to code short interrupt service routines (ISR) in place. Alternatively, it may be necessary to insert a JUMP instruction to the appropriate start address of the interrupt service routine if more memory is required for the ISR. When an interrupt occurs, the program sequencer ensures that there is no latency (beyond synchronization delay) when processing unmasked interrupts. In the case of the Timer, SPORT0, SPORT1, and software interrupts, the interrupt controller automatically jumps to the appropriate location in the interrupt vector table. At this point, a JUMP instruction to the appropriate ISR is required. Motor control peripheral interrupts are slightly different. When a peripheral interrupt is detected, a bit is set in the IRQFLAG Register for PWMSYNC and $\overline{\text{PWMTRIP}}$ or in the PORTA_FLAG Register for a PIO interrupt, and the $\overline{\text{IRQ2}}$ line is pulled low until all pending interrupts are acknowledged. The DSP software must determine the source of the interrupts by reading the IRQFLAG register. If more than one interrupt occurs simultaneously, the higher priority interrupt service routine is executed. Reading the IRQFLAG Register clears the $\overline{\text{PWMTRIP}}$ and PWMSYNC bits and acknowledges the interrupt, thus allowing further interrupts when the ISR exits. A user's PIO interrupt service routine must read the PORTA_FLAG Register to determine which PIO port is the source of the interrupt. Reading Register PORTA_FLAG clears all bits in the registers and acknowledges the interrupt, thus allowing further interrupts after the ISR exits. The configuration of all these registers is shown in Figure 29.

SYSTEM CONTROLLER

The system controller block of the ADMC(F)340 performs the following functions:

1. Manages the interface and data transfer between the DSP core and the motor control peripherals
2. Handles interrupts generated by the motor control peripherals and generates a DSP core interrupt signal $\overline{\text{IRQ2}}$
3. Controls the ADC multiplexer select lines
4. Enables $\overline{\text{PWMTRIP}}$ and PWMSYNC interrupts
5. Controls the multiplexing of the SPORT1 and SPORT0 pins
6. Controls the PWM single/double update mode
7. Controls the ADC conversion time modes and the SHA timers
8. Controls the auxiliary PWM operation mode
9. Contains a status register (SYSSTAT) that indicates the state of the $\overline{\text{PWMTRIP}}$ pin, the watchdog timer, and the PWM timer
10. Performs a reset of the motor control peripherals and control registers following a hardware, software, or watchdog initiated reset

SPORT1 and SPORT0 Control

The ADMC(F)340 has two serial ports: SPORT0 and SPORT1. SPORT1 is available with a limited number of pins and is mainly intended as a secondary port for development tools interfacing and/or for code booting from an external serial memory. Figure 18 shows the internal multiplexing of the SPORT0 and SPORT1 signals. SPORT0 is intended as a general-purpose communication port. SPORT0 can support the following operating modes: SPORT, UART, and SPI.

SPORT1 Configuration

There are two operating modes for SPORT1: boot mode and UART mode. These modes are selectable through Bit 4 of MODECTRL Register. With SPORT1 in boot mode, SPORT1 serial clock (SCLK1) is externally available through the SCLK1/SCLK0 pin. The signal SCLK1 is used to drive the external serial memory input clock.

Also SPORT1 Flag signal (FL1) is externally available through the FL1/DT1 pin. This signal is used to drive the external serial memory input reset.

With SPORT1 configured in UART mode, the SPORT0 serial clock (SCLK0) is externally available through the SCLK1/SCLK0 pin. The SPORT1 data transmit (DT1) is externally available through the FL1/DT1 pin.

SPORT0 Configuration

SPORT0 can be configured in SPORT, UART, and SPI modes.

SPORT0 can be configured for UART mode. In this mode, the DR0 and RFS0 signals of the internal serial port are connected together.

SPORT0 can be configured to operate as a master SPI interface. The SPI mode is set through Bit 14 of the MODECTRL Register. When SPORT0 is configured as an SPI interface, the SPORT I/O pins assume the configuration shown in Table XI (ADMCF340 only).

The Slave Select pin automatically generates the select signal at each word transfer (ADMCF340 only). This pin can also be used as a general-purpose I/O during the SPI transfer without affecting the SPORT operations (ADMCF340 only).

The SPI clock polarity and phase are configurable through Bits 13 and 12 of the MODECTRL Register (ADMCF340 only). The SPI transfer using clock phase is shown in Figure 19 and Figure 20 (ADMCF340 only).

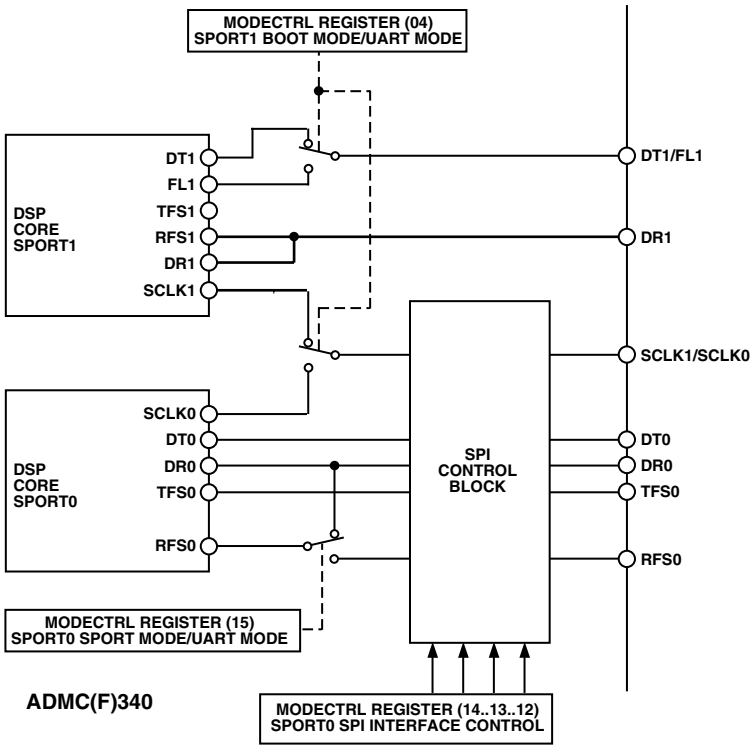


Figure 18. SPORT0 and SPORT1 Internal Multiplexing (Simplified Diagram)

Table XI. SPORT0 Pin Assignment in SPI Mode

SPORT I/O Signal	SPI Mode	SPI MODE I/O
DT0 (Data Transmit)	MOSI (Master Output/Slave Input)	Output
DR0	MISO (Master Input Slave Output)	Input
TFS0	SS (Slave Select)	Output
RFS0	Unused	N/A
SCLK0	SCK (Serial Clock)	Output

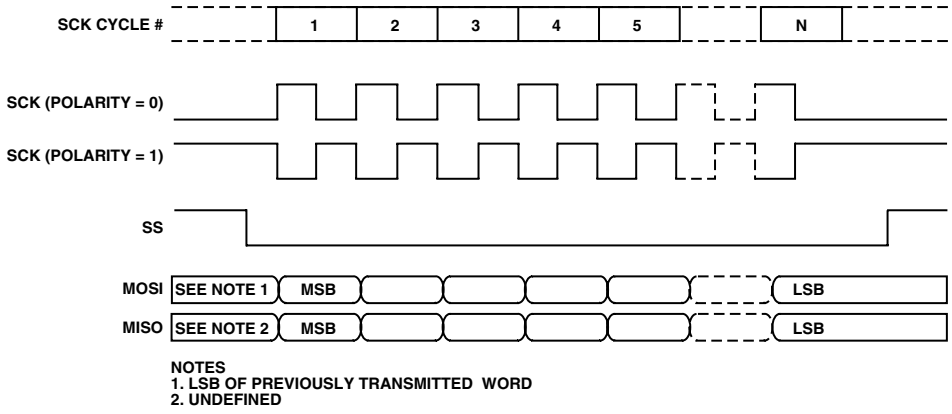


Figure 19. SPI Transfer Using Clock Phase CPHA = 0

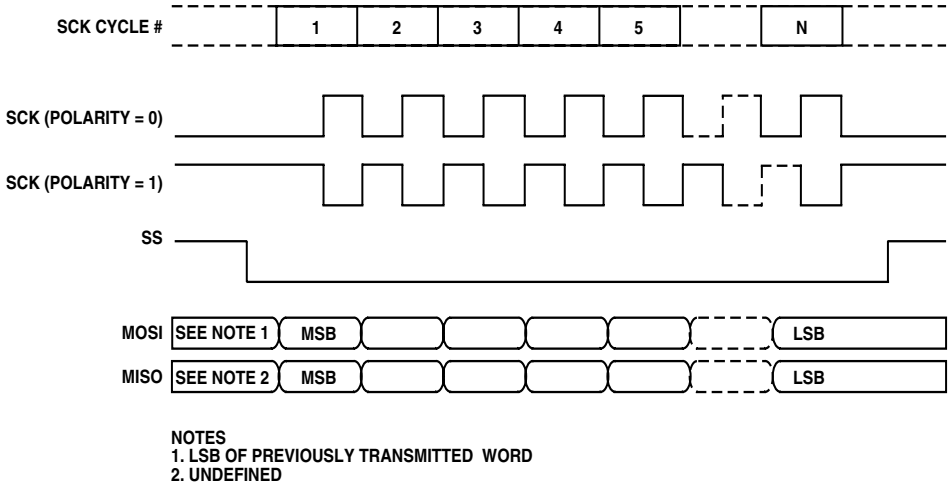


Figure 20. SPI Transfer Using Clock Phase CPHA = 1

Table XII. Peripheral Register Map

Address (HEX)	Name	Bits Used	Function
0x2000	ADC1	[15 . . . 4]	ADC Results for V1/I_{SENSE}1
0x2001	ADC2	[15 . . . 4]	ADC Results for V2/I_{SENSE}2
0x2002	ADC3	[15 . . . 4]	ADC Results for V3/I_{SENSE}3
0x2003	ADCAUX	[15 . . . 4]	ADC Results for VAUX
0x2004	PORTA_DIR	[8 . . . 0]	PA8...PA0 Pins Direction Setting
0x2005	PORTA_DATA	[8 . . . 0]	PA8...PA0 Pins Input/Output Data
0x2006	PORTA_INTEN	[8 . . . 0]	PA8...PA0 Pins Interrupt Enable
0x2007	PORTA_FLAG	[8 . . . 0]	PORTA Pins Interrupt Status
0x2008	PWMTM	[15 . . . 0]	PWM Period
0x2009	PWMDT	[9 . . . 0]	PWM Dead Time
0x200A	PWMPD	[9 . . . 0]	PWM Pulse Deletion Time
0x200B	PWMGATE	[9 . . . 0]	PWM Gate Drive Configuration
0x200C	PWMCHA	[15 . . . 0]	PWM Channel A Pulsewidth
0x200D	PWMCHB	[15 . . . 0]	PWM Channel B Pulsewidth
0x200E	PWMCHC	[15 . . . 0]	PWM Channel C Pulsewidth
0x200F	PWMSEG	[8 . . . 0]	PWM Segment Select
0x2010	AUXCH0	[7 . . . 0]	AUX PWM Output 0
0x2011	AUXCH1	[7 . . . 0]	AUX PWM Output 1
0x2012	AUXTM0	[7 . . . 0]	Auxiliary PWM Frequency Value
0x2013	AUXTM1	[7 . . . 0]	Auxiliary PWM Frequency Value/Offset
0x2014			Reserved
0x2015	MODECTRL	[8 . . . 0]	Mode Control Register
0x2016	SYSSTAT	[3 . . . 0]	System Status
0x2017	IRQFLAG	[1 . . . 0]	Interrupt Status
0x2018	WDTIMER	[15 . . . 0]	Watchdog Timer
0x2019 . . . 43			Reserved
0x2044	PORTB_DIR	[15 . . . 0]	PB15...PB0 Pin Direction Setting
0x2045	PORTB_DATA	[15 . . . 0]	PB15...PB0 Data and Mode Control
0x2046	PORTB_INTEN	[15 . . . 0]	PB15...PB0 Pin Interrupt Enable
0x2047	PORTB_FLAG	[15 . . . 0]	PB15...PB0 Pin Interrupt Status
0x2048			Reserved
0x2049	PORTA_SELECT	[15 . . . 0]	PIO Mode Select
0x204A . . . 5F			Reserved
0x2060	PWMSYNCWT	[7 . . . 0]	PWMSYNC Pulsewidth
0x2061	PWMSWT	[0]	PWM S/W Trip Bit
0x2062 . . . 67			Reserved
0x2068	ICONST_TRIM	[2. . .0]	ICONST_TRIM
0x2069	SHA1_TM	[15...0]	Sample-and-Hold Timer
0x206A	SHA2_TM	[15...0]	Sample-and-Hold Timer
0x206B	SHA3_TM	[15...0]	Sample-and-Hold Timer
0x2070			Reserved
0x2080	FMCR	[15. . .0]	Flash Memory Control Register
0x2081	FMAR	[11. . .0]	Flash Memory Address Register
0x2082	FMDRH	[13. . .0]	Flash Memory Data Register High
0x2083	FMDRL	[15. . .0]	Flash Memory Data Register Low
0x2084 . . . FF			Reserved

Table XIII. DSP Core Registers

Address	Name	Bits used	Function
0x3FFA	SPORT0_Rx_Words1	[15 . . . 0]	Multichannel Receive Word Enables
0x3FF9	SPORT0_Rx_Words0	[15 . . . 0]	Multichannel Receive Word Enables
0x3FF8	SPORT0_Tx_Words1	[15 . . . 0]	Multichannel Transmit Word Enables
0x3FF7	SPORT0_Tx_Words0	[15 . . . 0]	Multichannel Transmit Word Enables
0x3FF6	SPORT0_CTRL_REG	[15 . . . 0]	Control Register
0x3FF5	SPORT0_SCLKDIV	[15 . . . 0]	Serial Clock Divide Modulus
0x3FF4	SPORT0_RFSDIV	[15 . . . 0]	Receive Frame Sync Divide Modulus
0x3FF3	SPORT0_AUTOBUF CTRL	[15 . . . 0]	Autobuffer Control Register
0x3FF2	SPORT1_CTRL_REG	[15 . . . 0]	Control Register
0x3FFF	SYSCNTL	[15 . . . 0]	System Control Register
0x3FFE	MEMWAIT	[15 . . . 0]	Memory Wait State Control Register
0x3FFD	TPERIOD	[15 . . . 0]	Interval Timer Period Register
0x3FFC	TCOUNT	[15 . . . 0]	Interval Timer Count Register
0x3FFB	TSCALE	[7 . . . 0]	Interval Timer Scale Register
0x3FFA . . . F3			Reserved
0x3FF2	SPORT1_CTRL_REG	[15 . . . 0]	SPORT1 Control Register
0x3FF1	SPORT1_SCLKDIV	[15 . . . 0]	SPORT1 Clock Divide Register
0x3FF0	SPORT1_RFSDIV	[15 . . . 0]	SPORT1 Receive Frame Sync Divide
0x3FEF	SPORT1_AUTOBUF_CTRL	[15 . . . 0]	SPORT1 Autobuffer Control Register

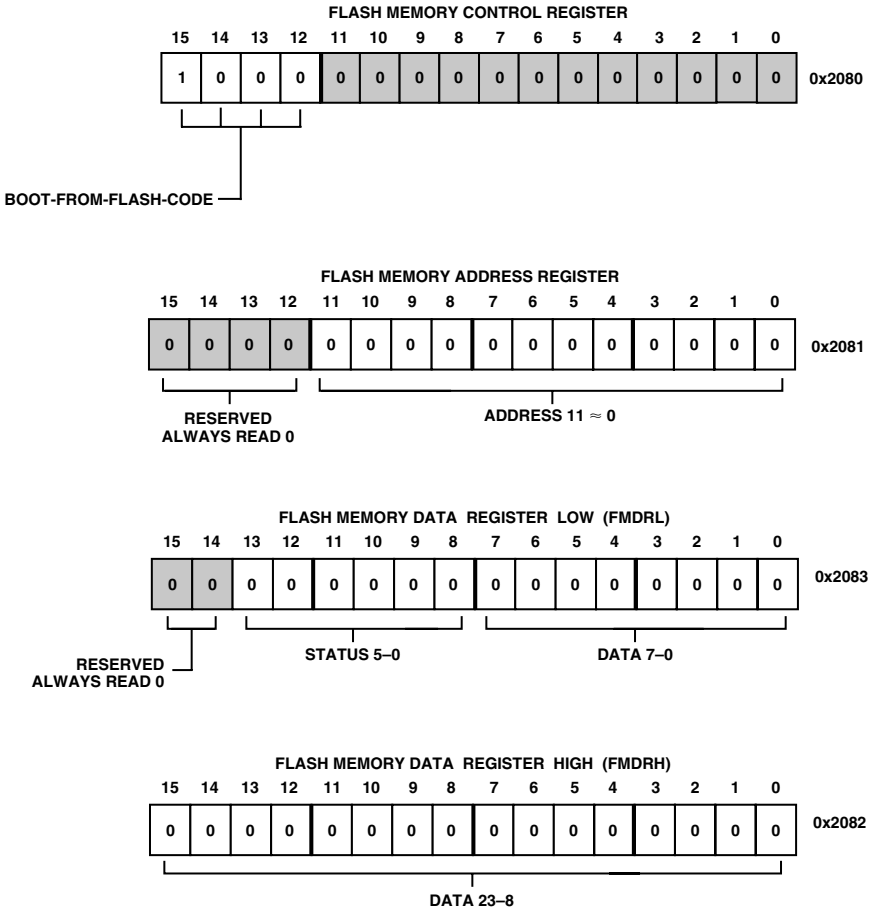


Figure 21. Configuration of Flash Memory Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

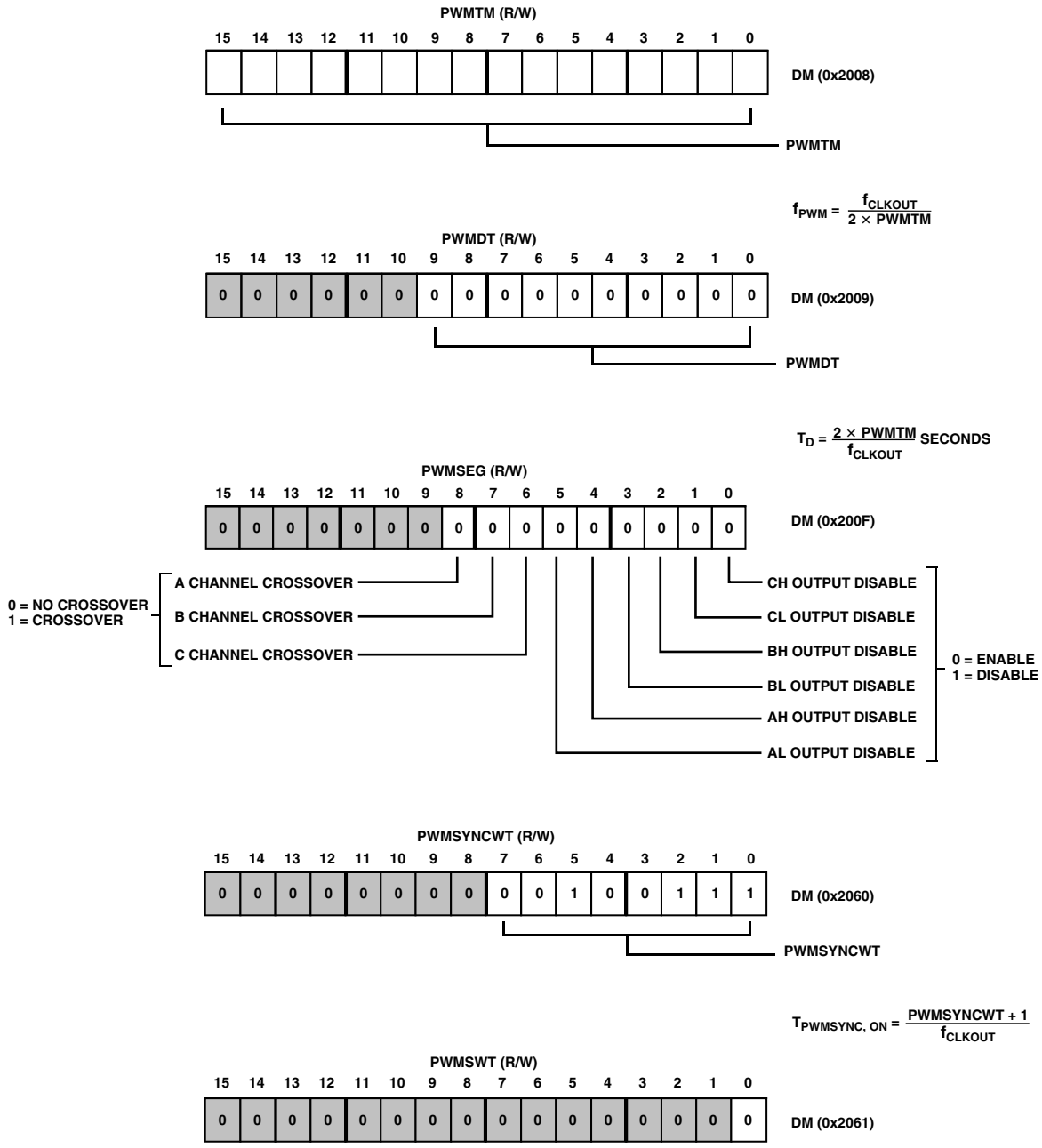


Figure 22. Configuration of PWM Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

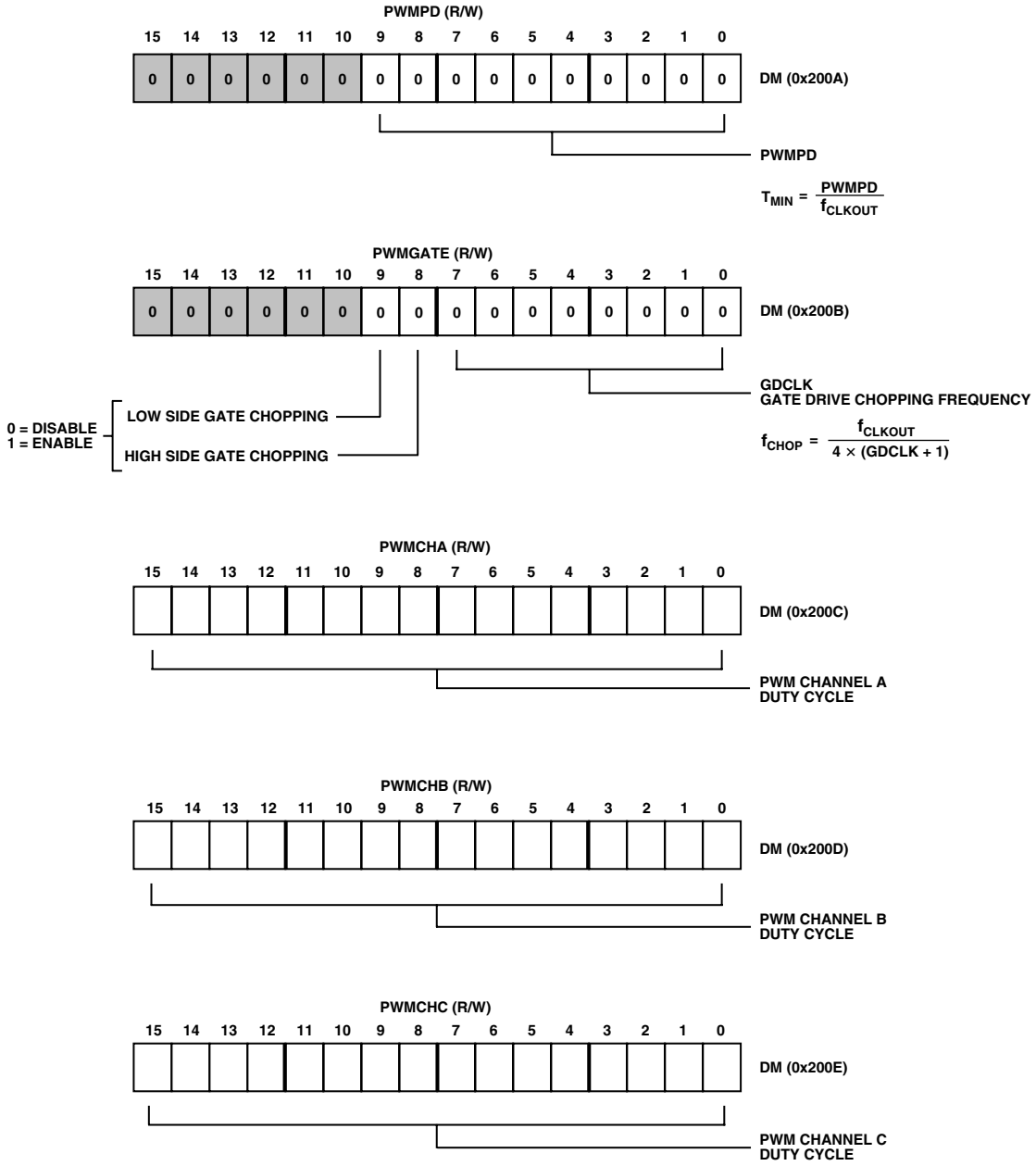


Figure 23. Configuration of Additional PWM Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

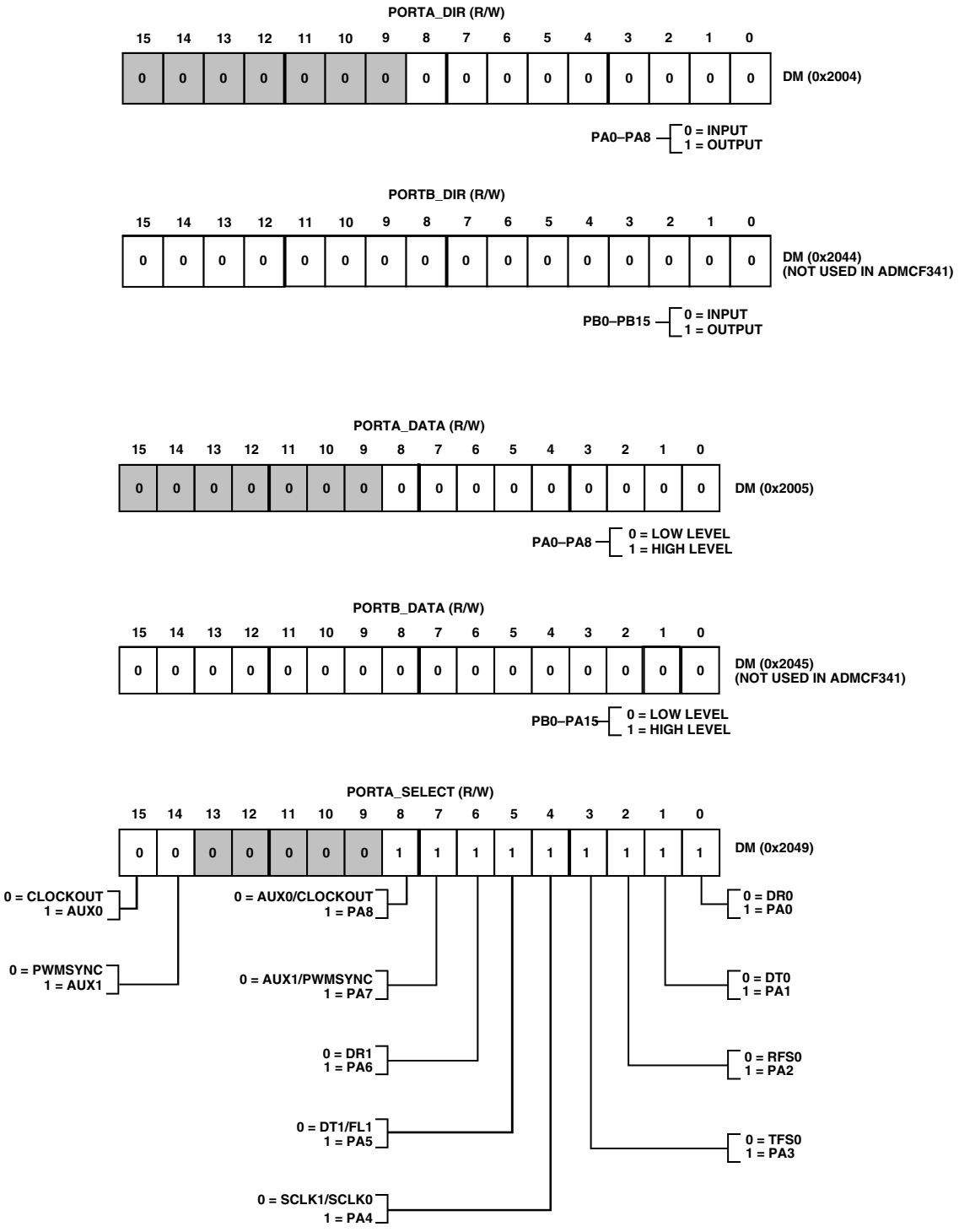


Figure 24. Configuration of PIO Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

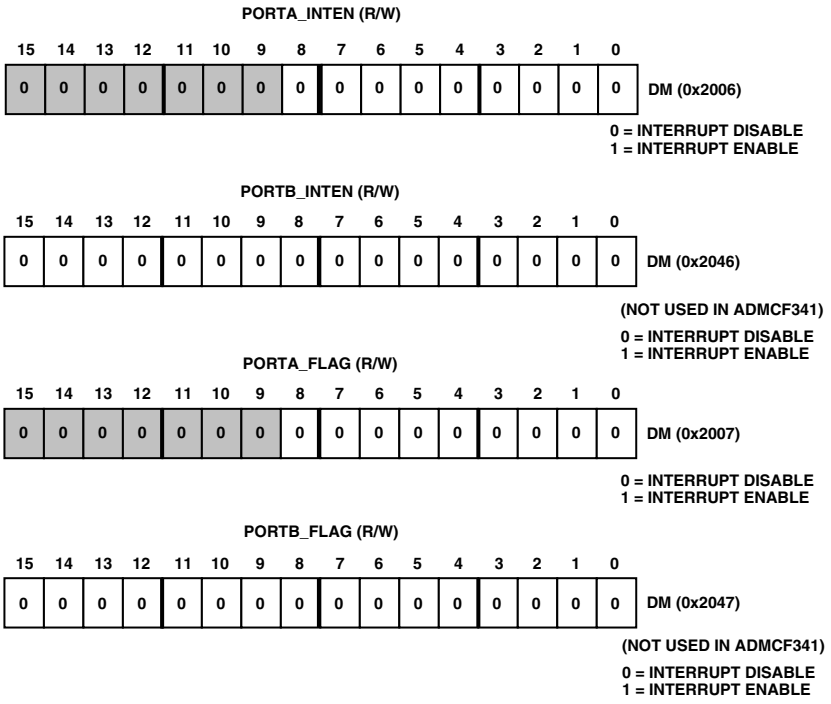


Figure 25. Configuration of Additional PIO Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

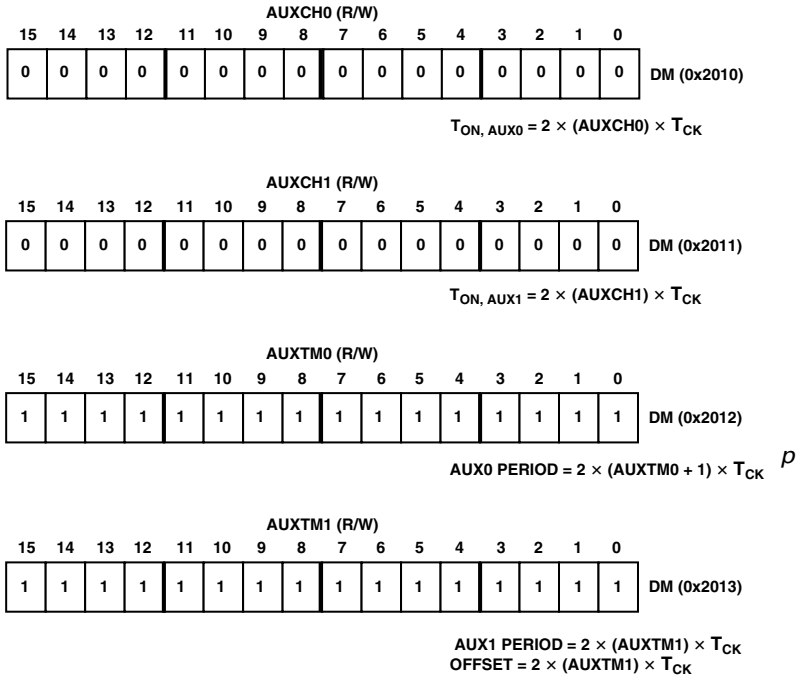


Figure 26. Configuration of Auxiliary PWM Register

Default bit values are shown; if no value is shown, the bit field is undefined at reset.

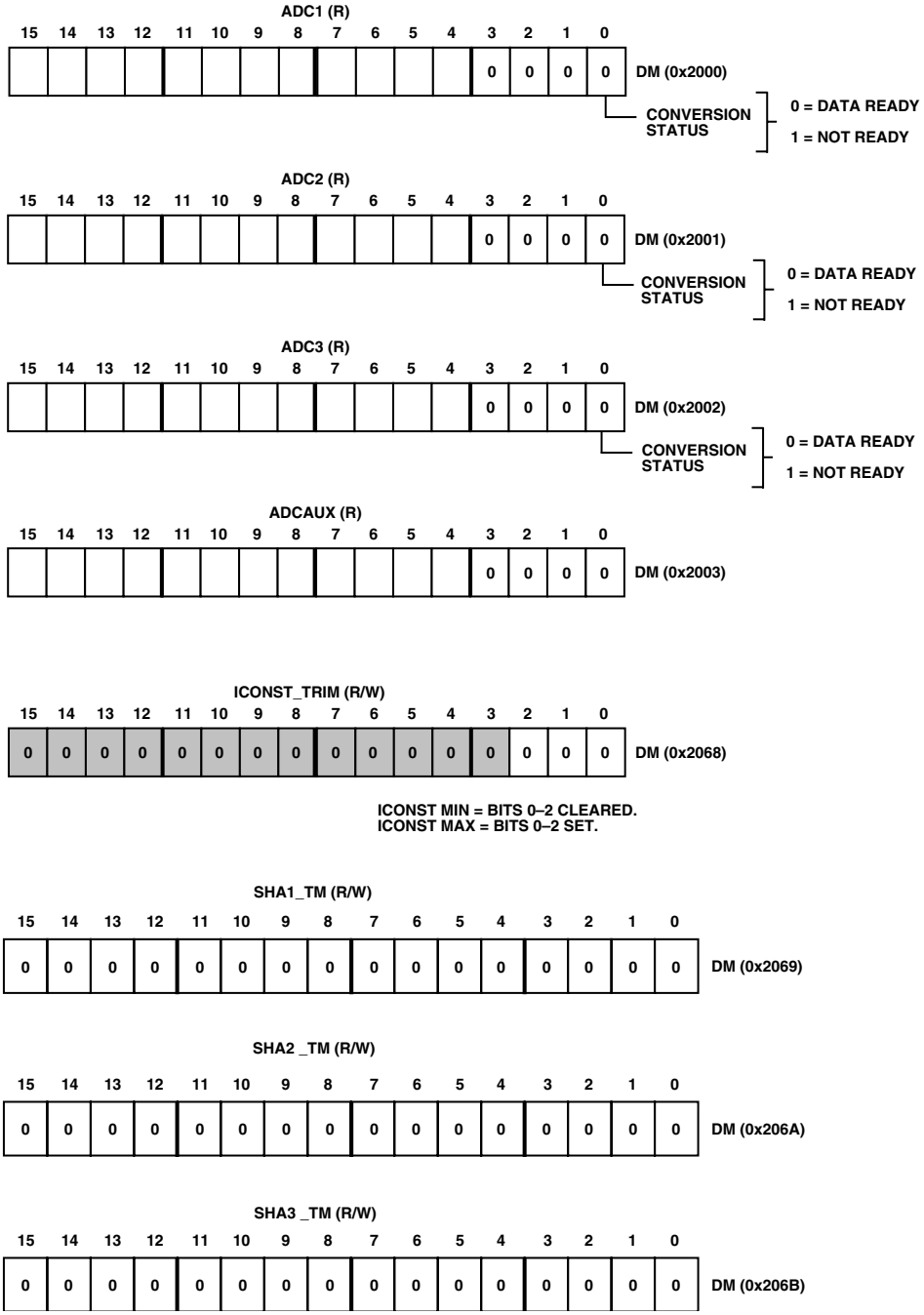


Figure 27. Configuration of ADC Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

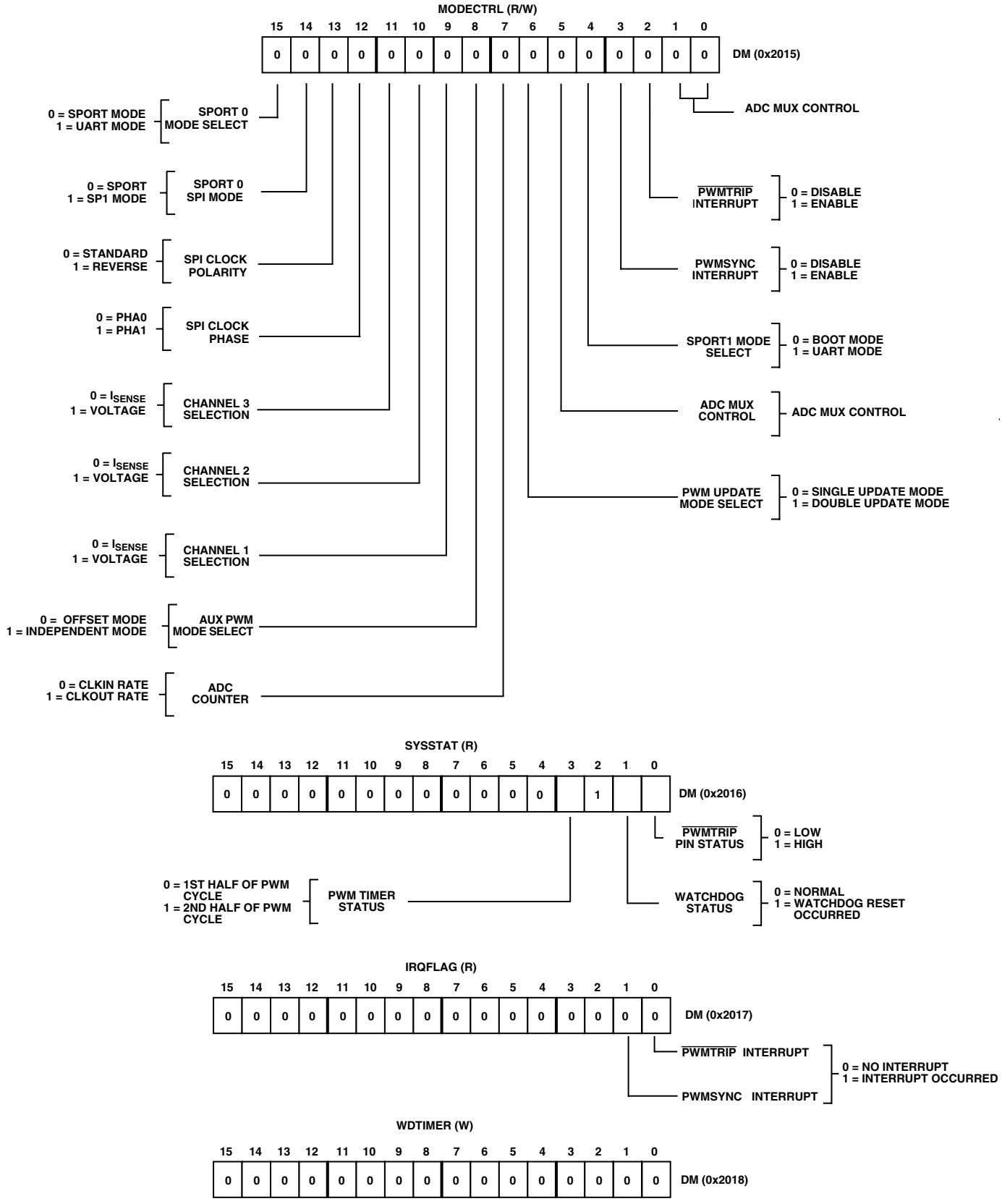


Figure 28. Configuration of Status/Control Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset.

Table XIV. Auxiliary Analog Input Selection

Selection	MODECTRL (5)	MODECTRL (1)	MODECTRL (0)
VAUX0 (1)	0	0	0
VAUX1 (1)	0	0	1
VAUX2 (1)	0	1	0
V_{REF} (1)	0	1	1
VAUX4	1	0	0
VAUX5	1	0	1
VAUX6	1	1	0
VAUX7	1	1	1

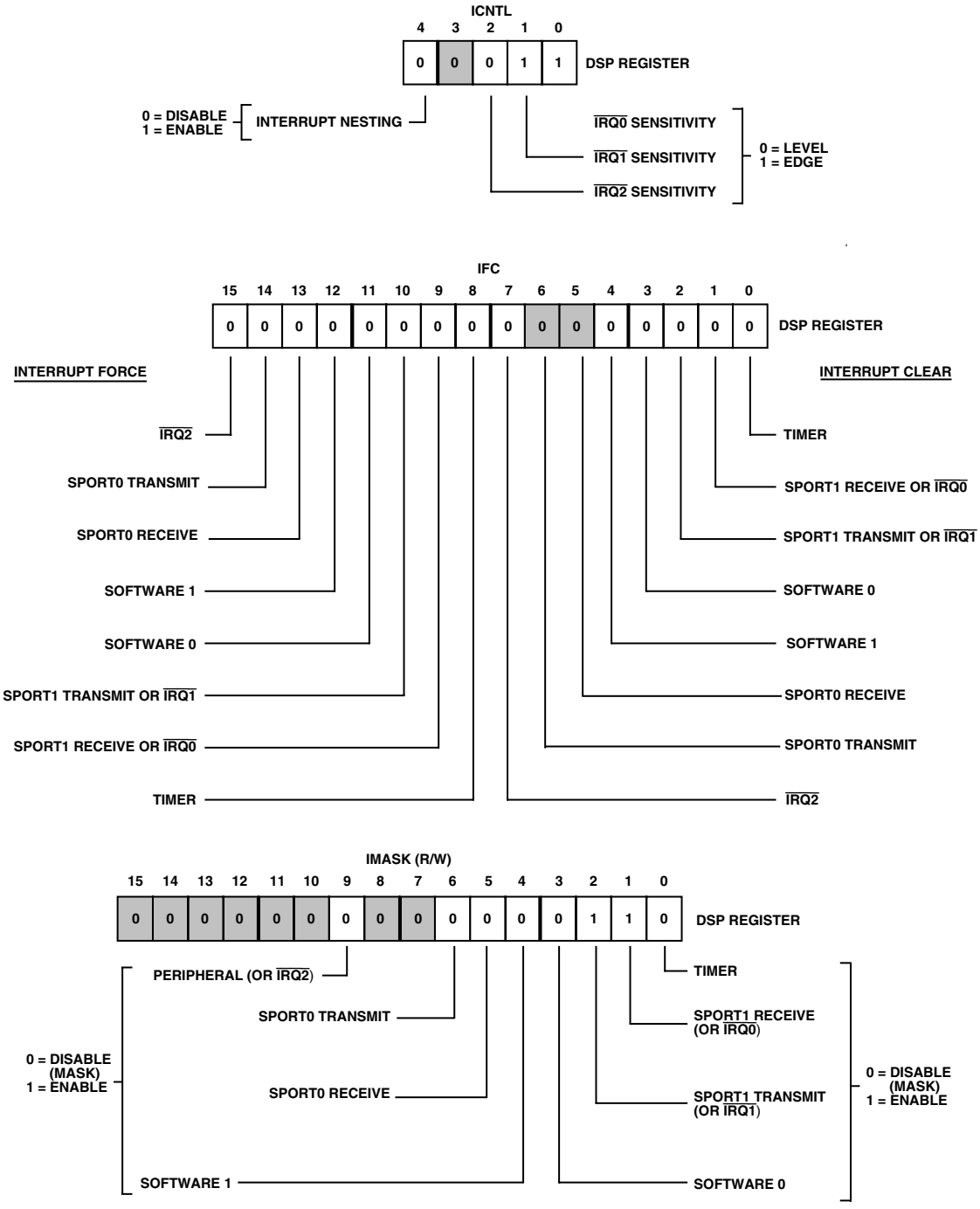


Figure 29. Configuration of Interrupt Control Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown in a gray field—these bits should always be written as shown.

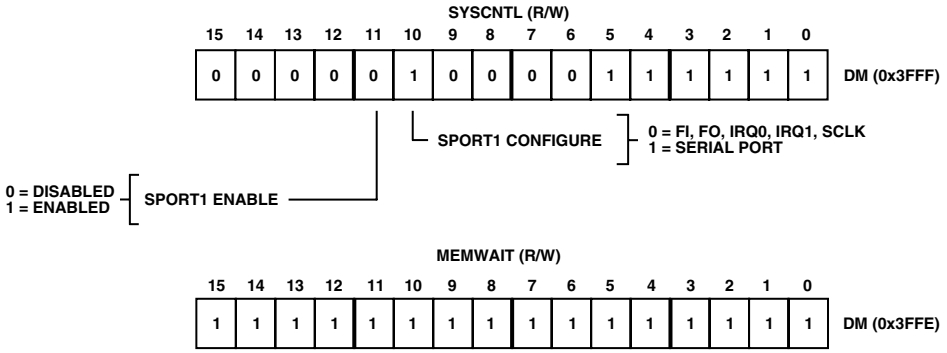
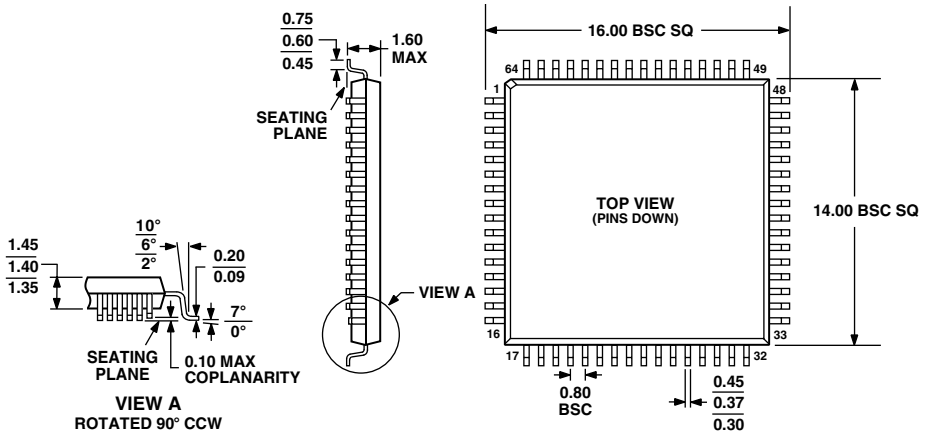


Figure 30. Configuration of Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset.

OUTLINE DIMENSIONS

64-Lead Thin Plastic Quad Flatpack [LQFP]
(ST-64A)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BEB

C02723–0–10/02(A)

Revision History

Location	Page
10/02—Data Sheet changed from REV. 0 to REV. A.	
Changed ADMCF340 to ADMC(F)340	UNIVERSAL
Changes to PRODUCT TITLE	1
Changes to FEATURES	1
Changes to VOLTAGE REFERENCE	3
Changes to ABSOLUTE MAXIMUM RATINGS	6
Changes to ORDERING GUIDE	6
Changes to SPORT0 Configuration section	26

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