MSM7582B

π/4 Shift QPSK MODEM

GENERAL DESCRIPTION

The MSM7582B are CMOS ICs for the π/4 shift QPSK modem developed for the digital cordless telephone systems.
The devices are designed for Personal and Cell station applications.

FEATURES

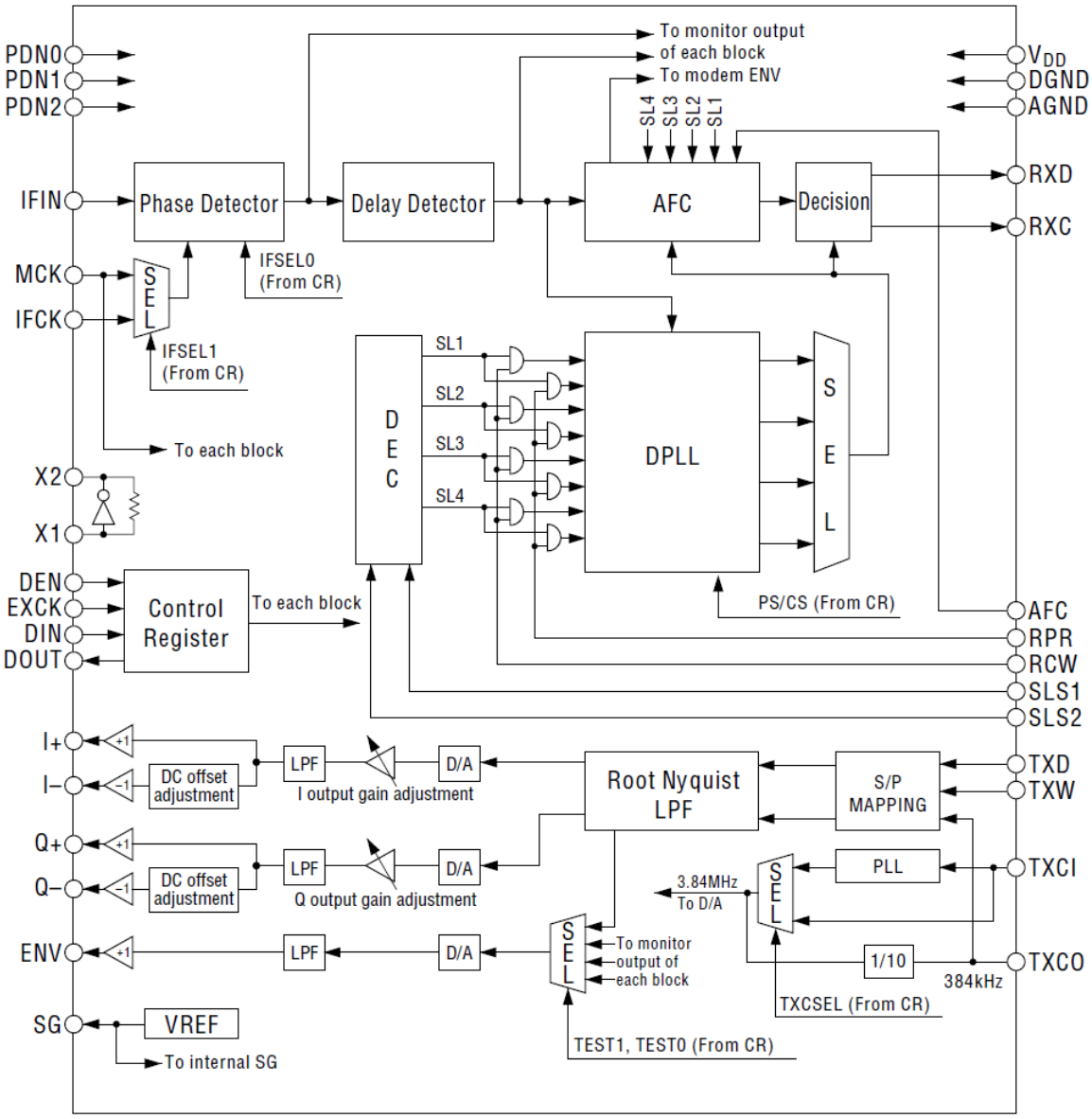
- Single Power Supply (V_{DD}: 2.7 V to 3.6 V)

(Modulator Block)
- Built-in Root Nyquist Filter for Baseband Limiting (50% Roll-off)
- Ramp Bit for Burst Signal Rise-up: 2.0 symbols
- Ramp Bit for Burst Signal Fall-down: 2.0 symbols
- Built-in D/A converters for Analog Output of Quadrature Signal I/Q Components and Power Envelope Output $\sqrt{I^2 + Q^2}$
- Differential I/Q Analog output format
- I/Q Output DC Offset / Gain Adjustable

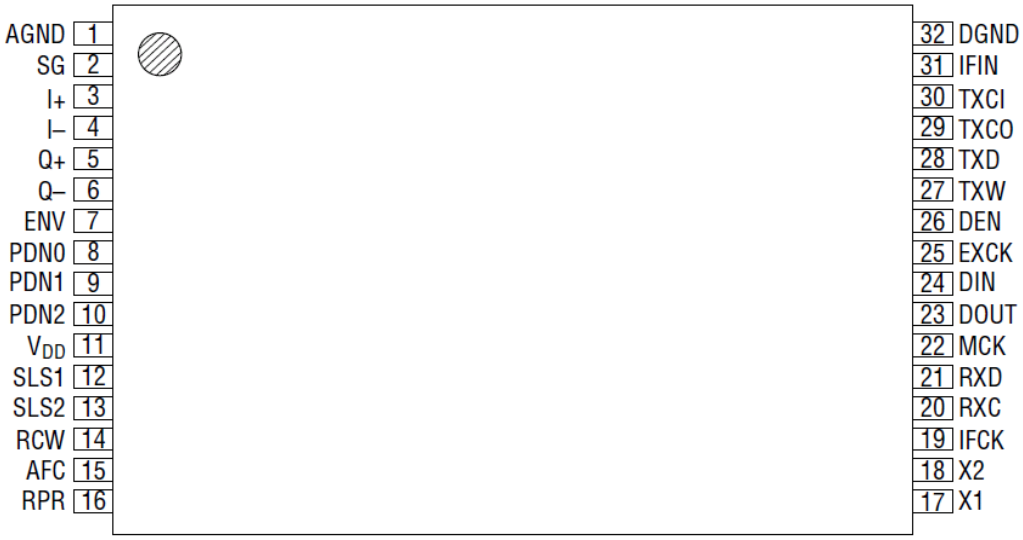
(Demodulator Block)
- Full Digital System, π/4 shift QPSK Demodulation
- Input IF signal Frequency Selectable: 1.2/10.7/10.75/10.8 MHz
- Built-in Clock Recovery: 4 Circuits useful for Cell station

(Common)
- Various Power-down Modes: Tramsmit/Receive Independant
- Built-in Precise Analog Voltage Reference
- MCU Serial Interface for Mode setting and Built-in Test circuit
- Test Modes: Eye pattern / AFC Compensating Signal / Phase Detection Signal, possible to monitor
- Transmission Speed: 384 kbps
- Low Power consumption
  Operating mode : 15 mA Typ. / Modulator (V_{DD} = 3.0 V)
  : 9 mA Typ. / Demodulator (V_{DD} = 3.0 V)
  Whole system Power-down mode: 0.01 mA Typ. (V_{DD} = 3.0 V)
- Package:
  32-pin plastic TSOP (TSOP(1)32-P-0814-0.50-1K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic TSOP

PIN AND FUNCTIONAL DESCRIPTIONS

TXD

Transmit data input for 384 kbps.

TXCI

Transmit clock input.
When the control register CR0 – B6 is "0", a 384 kHz clock pulse synchronous with TXD should be input to this pin. This clock pulse should be continuous because these devices use APLL to generate the internal clock pulse.
When CR0 – B6 is "1", a 3.84 MHz clock pulse should be input to this pin. When the 3.84 MHz clock pulse is applied, TXCO outputs a 384 kHz clock pulse, which is generated by dividing the 3.84 MHz to TXCI by 10. The transmit data, synchronous 384 kHz clock pulse, should be input to the TXD. In this case the devices do not use APLL, and the 3.84 MHz clock pulse need not be continuous. (Refer to Fig. 1.)

TXCO

Transmit clock output.
When CR0 - B6 is "0", TXCO outputs the 384 kHz clock pulse (APLL output) for monitoring purposes. When CR0 – B6 is "1", this pin outputs a 384 kHz clock pulse generated by dividing the TXCI input by 10. (Refer to Fig. 1.)
When CR0 – B6 = "0" and CR5 – B7 = "1", this pin outputs the burst timing position.

TXW

Transmit data window input.
The transmit timing signal for the burst data is input to the device pin. If TXW is "1", the modulation data is output. (Refer to Fig. 1.)

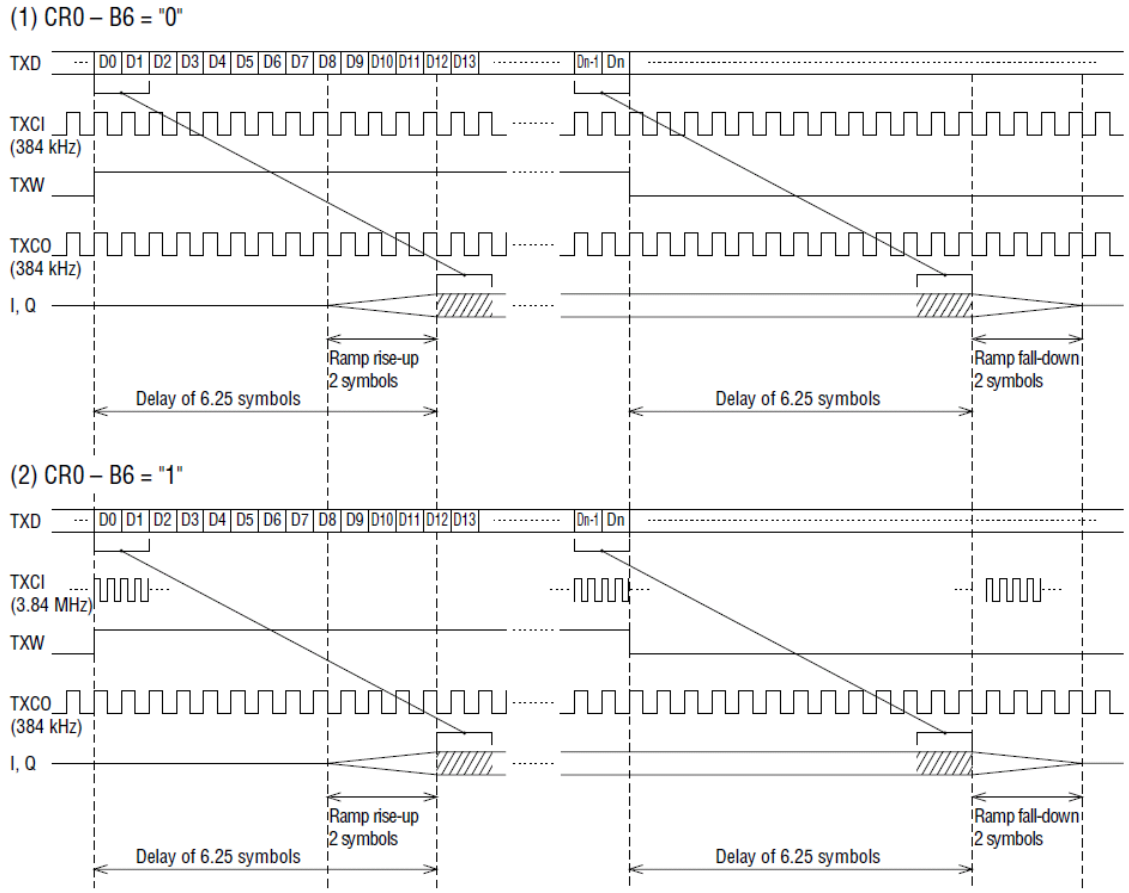


Figure 1 Transmit Timing Diagram

I+, I–

Quadrature modulation signal I component differential analog outputs.
Their output levels are 500 mV_{pp} with 1.6 Vdc as the center value. The output pin load conditions are: R ≥ 10 kΩ, C ≤ 20 pF. The gain of these pins can be adjusted using the control register CR1 – B7 to B4, and the offset voltage at the I– pin can be adjusted using CR3 – B7 to B3.

Q+, Q–

Quadrature modulation signal Q component differential analog outputs.
Their output levels are 500 mV_{PP} with 1.6 Vdc as the center value. The output pin load conditions are: R ≥ 10 kΩ, C ≤ 20 pF. The gain of these pins can be adjusted using the control register CR1 – B3 to B0, and the offset voltage at the Q– pin can be adjusted by using CR4 – B7 to B3.

ENV

Quadrature modulation signal envelope ($\sqrt{I^2 + Q^2}$)output.
Its output level is 500 mV_{PP} with 1.6 Vdc as a center value. The output pin load conditions are : R ≥ 10 kΩ, C ≤ 20 pF. The gain of this output can be adjusted using the control register CR2 – B7 to B4.
This pin is also used to monitor eye pattern, AFC Compensating signal, and phase defection of the demodulator block during the test mode. Refer to the description of the control register for details.

SG

Internal reference voltage output.
The output voltage is about 2.0 V. A bypass capacitor should be connected between this pin and the AGND pin. The external SG voltage, if necessary should be used via a buffer.

PDN0, PDN1, PDN2

Inputs for power-down control.
PDN0 controls the standby / communication modes, PDN1 controls the modulator, and PDN2 controls the demodulator. Refer to Table 1 for details.
The control register should be reset by input of a signal with width of 200 ns or more.
Be sure to reset all the control registers by keeping Mode A for 200ns or longer after the power is turned on and the V_{DD} exceeds 2.7V.

Table-1 Power Down Control

	PDN0	PDN2	PDN1	Function	Mode
Standby Mode	0	0/1	1	All power-down. The control register is reset.	Mode A
	0	0	0	All power-down. The control register is not reset.	Mode B
	0	1	0	Modulator power is off (VREF and PLL power are also off). Demodulator power is on.	Mode C
Communication Mode	1	0	0	Modulator power is off (VREF and PLL power is on). I and Q outputs are in a high-impedance state. Only demodulator clock recovery block power is on.	Mode D
	1	0	1	Modulator power is on Only demodulator clock recovery block power is on.	Mode E
	1	1	0	Modulator power is off (VREF and PLL power is on). I and Q outputs are in a high-impedance state. Demodulator power is on.	Mode F
	1	1	1	Modulator power is on Demodulator power is on.	Mode G

V_{DD}

+3 V power supply voltage.

AGND

Analog signal ground.

DGND

Digital signal ground.
AGND and DGND pins should be connected as close as possible on the PCB.

MCK

Master clock input.
The clock frequency is 19.2 MHz.

IFIN

Modulated signal input for the demodulator block.
Select the IF frequency from 1.2 MHz, 10.7 MHz, 10.75 MHz, and 10.8 MHz, based on CR0 – B4 and B3.

IFCK

Clock signal input for demodulator block IF frequencies (10.7 MHz or 10.75 MHz).
If the IF frequency is 10.7 MHz, 19.0222 MHz should be supplied. When it is 10.75 MHz, 19.1111 MHz should be supplied. When the IF frequency is 1.2 MHz or 10.8 MHz, set this pin to "0" or "1". (Refer to Fig. 2.)

X1, X2

Crystal oscillator connection pins.
When supplying a 19.0222 MHz or 19.1111 MHz clock to IFCK, use these pins (Refer to Fig. 2.)

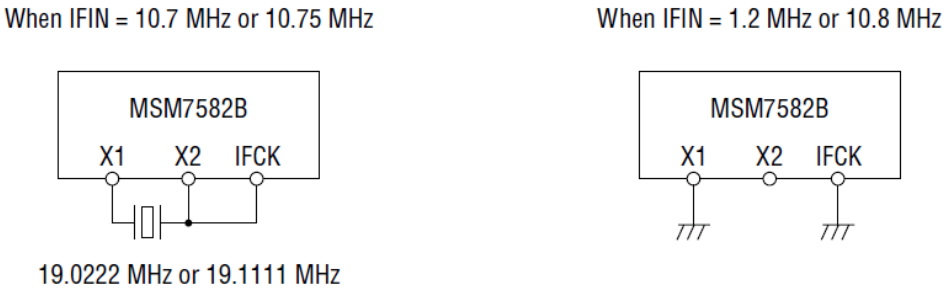


Figure 2 How to Use IFCK, X1, and X2

RXD, RXC

Receive data and clock output. When power is turned on, the outputs of circuits selected by SLS1 and SLS2 appear at these pins. (Refer to Fig. 3)

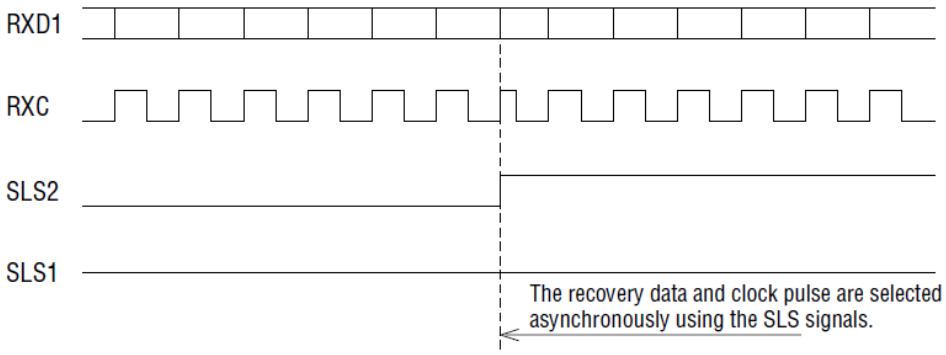


Figure 3 RXD and RXC Timing Diagram

SLS2, SLS1

Receiver slot select signal inputs.
The devices have four sets of clock recovery circuit to each channel and four AFC information storage registers. One these circuits is selected from a combination of the signals at these pins.

(SLS2, SLS1) = (0, 0): Slot 1, (0, 1): Slot 2
(1, 0): Slot 3, (1, 1): Slot 4

RPR

High-speed phase clock control signal input for the clock recovery circuit.
If this pin is "1", the clock recovery circuit starts in the high-speed phase clock mode. When the phase difference is less than a defined value, the circuit shifts to the low-speed phase clock mode automatically. When this pin is "0", the circuit is always in the low-speed phase clock mode.

AFC

AFC operation range specification signal input.
As shown in Fig. 4, the AFC information is reset when both AFC and RPR are set to "1". AFC operation starts after a fixed number of clock cycles and after the AFC information is reset. If RPR is set to "1", an average number of times that AFC turns on is low. If RPR is "0", AFC is high. If AFC is "0", frequency error is not calculated, but the frequency is corrected using an error that is held.

RCW

Clock recovery circuit operation ON/OFF control signal input. If RCW pin is "0", DPLL does not make any phase corrections.

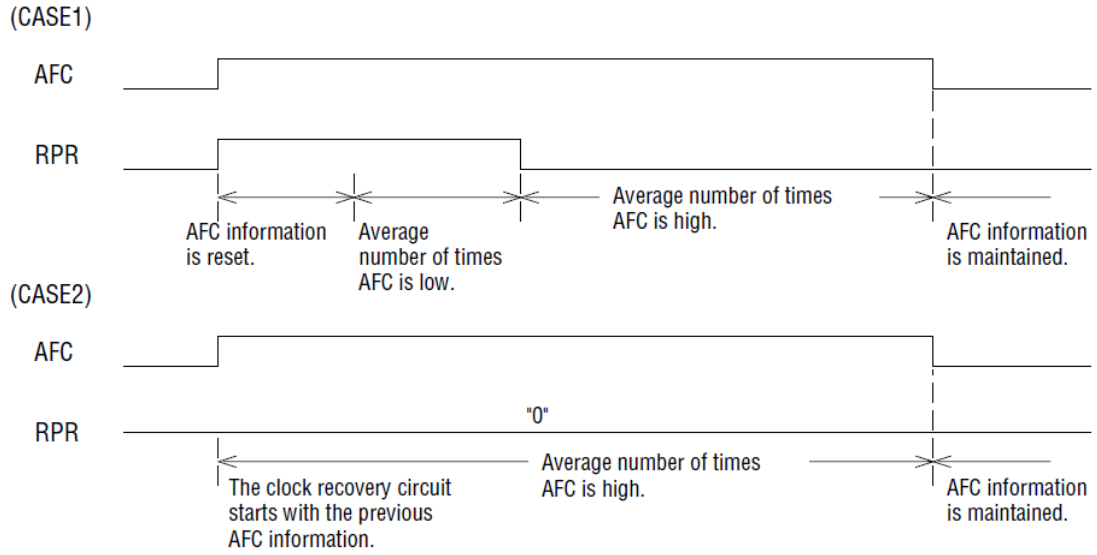


Figure 4 AFC Control Timing Diagram

DEN , EXCK, DIN, DOUT

Serial control ports for the microprocessor interface.
The MSM7582 and MSM7582B contain a 6-byte control register. An external CPU uses these pins to read data from and write data to the control register. DEN is an enable signal input pin. EXCK is a data shift clock pulse input pin. DIN is an address and data input pin. DOUT is a data output pin. Figure 5 shows an input/output timing diagram.

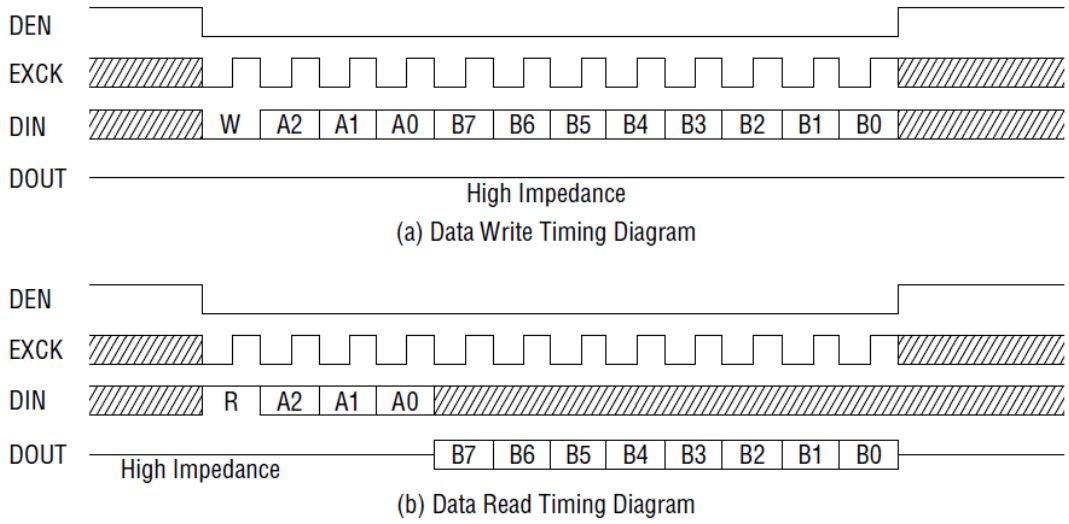


Figure 5 MCU Interface Input/Output Timing Diagram

The register map is shown below

Table-2 Control Register Map

Register	Address			Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	PS/CS	TXCSEL	MODOFF	IFSEL1	IFSEL0	ENVSEL	TEST1	TEST0	R/W
CR1	0	0	1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0	R/W
CR2	0	1	0	ENV GAIN3	ENV GAIN2	ENV GAIN1	ENV GAIN0	—	—	—	ICT0*	R/W
CR3	0	1	1	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—	R/W
CR4	1	0	0	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—	R/W
CR5	1	0	1	BSTO ENBL	ICT6	ICT5	ICT4	LOCAL INV1	LOCAL INV0	CLK SEL1	CLK SEL0	R/W

R/W : Read/Write enable

* Read-only register

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condtion	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 5	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condtion	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	—	3.6	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	All digital input pins	$0.45 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage	V_{IL}	All digital input pins	0	—	$0.16 \times V_{DD}$	V
Master Clock Frequency	f_{MCK}	MCK	—	19.2	—	MHz
Modulator Input Frequency	f_{TXC1}	TXCI (when CR0 – B6 = "0")	—	384	—	kHz
	f_{TXC2}	TXCI (when CR0 – B6 = "1")	—	3.84	—	MHz
Demodulator Input Frequency	f_{IFCK1}	IFCK (when IFIN = 10.7 MHz)	–50 ppm	19.0222	+50 ppm	MHz
	f_{IFCK2}	IFCK (when IFIN = 10.75 MHz)	–50 ppm	19.1111	+50 ppm	MHz
Clock Duty Cycle	D_{CCK}	MCK, IFCK, TXCI	40	50	60	%
IF Input Duty Cycle	D_{CIF}	IFCK	45	50	55	%

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Mode A, Mode B (when V_{DD} = 3.0 V)	—	0.02	0.05	mA
	I_{DD2}	Mode C (when V_{DD} = 3.0 V)	—	5.5	11.0	mA
	I_{DD3}	Mode D (when V_{DD} = 3.0 V)	—	5.5	11.0	mA
	I_{DD4}	Mode E (when V_{DD} = 3.0 V)	—	11.5	23.0	mA
	I_{DD5}	Mode F (when V_{DD} = 3.0 V)	—	9.5	19.0	mA
	I_{DD6}	Mode G (when V_{DD} = 3.0 V)	—	14.0	28.0	mA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	$0.5 \times V_{DD}$	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.2 mA	0.0	—	0.4	V
Input Leakage Current	I_{IH}	—	—	—	10	µA
	I_{IL}	—	—	—	10	µA

Analog Interface Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condtion	Min.	Typ.	Max.	Unit
Output Resistance Load	R_{LIQ}	I+, I–, Q+, Q–, ENV	10	—	—	kΩ
Output Capacitance Load	C_{LIQ}	I+, I–, Q+, Q–, ENV	—	—	20	pF
Output DC Voltage Level	V_{DC1}	I+, I–, Q+, Q– (TXW = 0)	1.55	1.6	1.65	V
	V_{DC2}	I+ (CR0 – B5 = 1) when not modulated	—	1.77	—	V
	V_{DC3}	Q+ (CR0 – B5 = 1) when not modulated	—	1.67	—	V
	V_{DC4}	ENV (TXW = 0)	—	1.35	—	V
	V_{DC5}	ENV (TXW = 1, CR0 – B2 = 0, TXD = 0)	—	1.72	—	V
	V_{DC6}	ENV (TXW = 1, CR0 – B2 = 1, TXD = 0)	—	1.63	—	V
Output AC Voltage Level	V_{AC}	I+, I–, Q+, Q– (TXD = 0)	340	360	380	mV_{PP}
Offset Voltage Difference	V_{OFF}	Difference among I+, I–, Q+, and Q–	–20	—	+20	mV
Output DC Voltage Adjustment Level Range	DCVL	—	—	±45	—	mV
Output AC Voltage Adjustment Level Range	ACVL	—	—	±4	—	%
Out-of-band Spectrum	P600	600 kHz detuning (*)	60	—	—	dB
	P900	900 kHz detuning (*)	65	—	—	dB
Modulation Accuracy	EVM	—	—	1.0	3.0	% rms
Demodulator IF Input Level	IFV	IFIN input level	0.4	—	V_{DD}	V_{PP}
IFIN Input Impedance	RIF	—	—	20	—	kΩ
	CIF	—	—	5	—	pF
SG Output Voltage	VSG	—	—	2.0	—	V
SG Output Impedance	RSG	—	—	2	—	kΩ
SG Warm-up Time	T_{SG}	SG↔AGND 0.1µF (Rise time to 90 % of max. level)	—	400	—	µs
Modulator D/A Conversion sampling Frequency	F_{SDA}	—	—	1.92	—	MHz
Modulator D/A Conversion offset Frequency	F_{CDA}	—	—	380	—	kHz

* Power attenuation at 600 kHz or 900 kHz ±96 kHz as referred to two times of the power in frequency band of 0 to 96 kHz

Digital Interface Characteristics

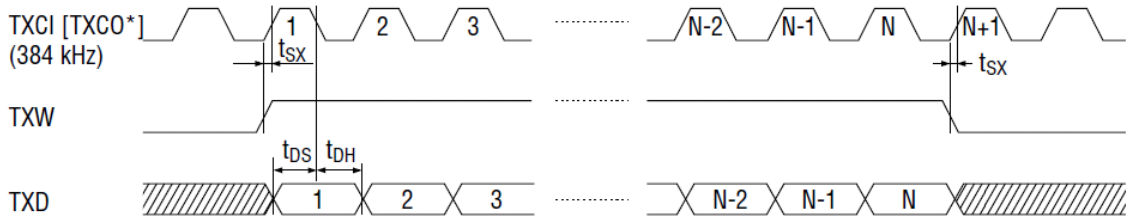
(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
			Others				
Transmitter Digital Input/Output Setting Time	t_{SX}	C load = 50 pF	Fig. 6	–200	—	+200	ns
	t_{DS} t_{DH}			200	—	—	ns
	t_{XD1} t_{XD2}			0	—	200	ns
	t_{XD3} t_{XD4}			0	—	200	ns
Receiver Digital Input/Output Setting Time	t_{RD1}	C load = 50 pF	Fig. 7	0	—	200	ns
	t_{RD2}			0	—	200	ns
	t_{RS1} to t_{RS4}			10	—	—	µs
	t_{RW}			10	—	—	µs
Serial Port Digital Input/Output Setting Time	t_{M1}	C load = 50 pF	Fig. 8	50	—	—	ns
	t_{M2}			50	—	—	ns
	t_{M3}			50	—	—	ns
	t_{M4}			50	—	—	ns
	t_{M5}			100	—	—	ns
	t_{M6}			50	—	—	ns
	t_{M7}			50	—	—	ns
	t_{M8}			0	—	50	ns
	t_{M9}			20	—	—	ns
	t_{M10}			20	—	—	ns
	t_{M11}			0	—	50	ns
	t_{M12}			—	—	4.0(*)	ns
				8.2(*)	—	—	
Shift Clock Frequency	f_{EXCK}	EXCK	EXCK	—	—	10	MHz

* Don't raise the DEN in the range (4.0ns to 8.2ns) delayed from falling edge of the 12th EXCK.

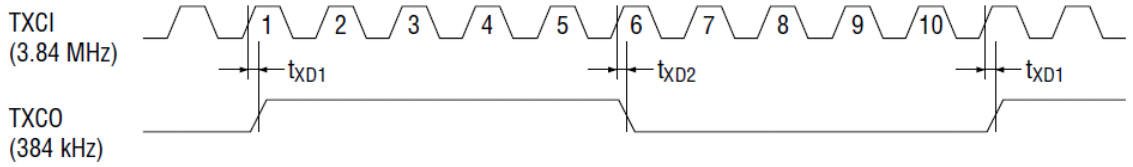
TIMING DIAGRAM

Transmit Data Input Timing



* [ ]: When CR0 – B6 = "1", TXCO is indicated.

Transmit Clock (TXCO) Output Timing (when CR0 – B6 = 1)



Transmit Burst Position Output (TXCO) Timing (when CR0 – B6 = 0 and CR5 – B7 = 1)

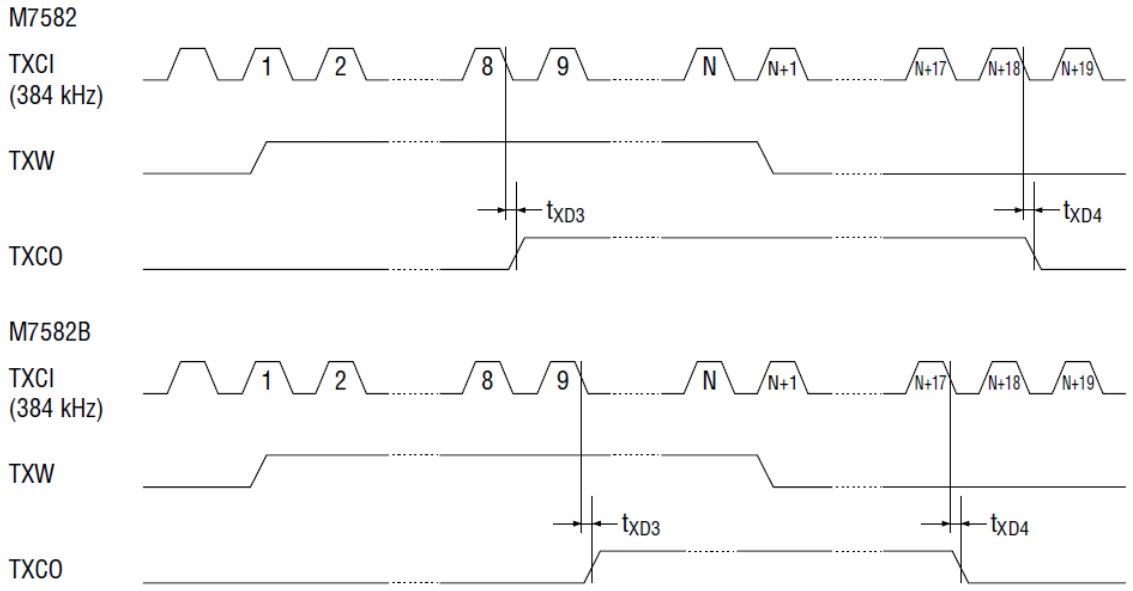


Figure 6 Transmit (Modulator) Digital Input/Output Timing

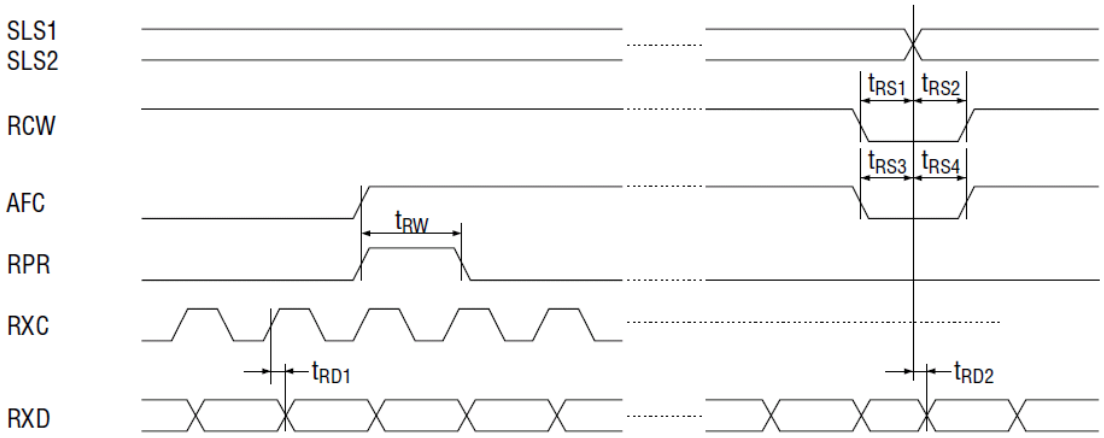


Figure 7 Receiver (Demodulator) Digital Input/Output Timing

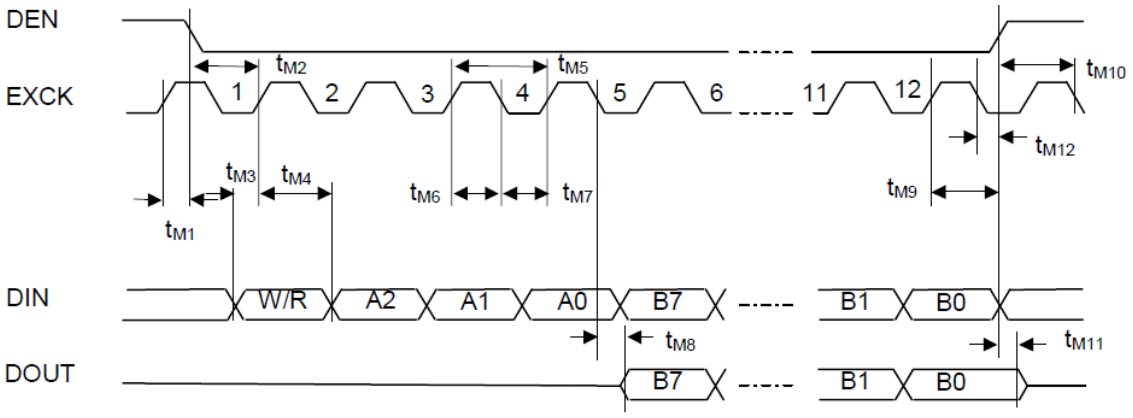


Figure 8 Serial Control Port Interface

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (basic operation mode setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	PS/CS	TXC SEL	MOD OFF	IFSEL 1	IFSEL 0	ENV SEL	TEST 1	TEST 0
Initial value (*)	0	0	0	0	0	0	0	0

* the initial value is set when a reset signal is supplied by a PDN.

B7: PS/CS selection
1/CS (4 Clock recovery DPLLs are on.)
0/PS (2 Clock recovery DPLLs are on.)

B6: Transmit timing clock selection
0/TXCI input: 384 kHz.
TXCO output: 384 kHz output from APLL. Transmit data TXD is input in synchronization with the rising edge of TXCI (APLL is on.)
1/TXCI input: 3.84 MHz.
TXCO output: 384 kHz (one-tenth of the TXCI frequency). Transmit data TXD is input in synchronization with the rising edge of TXCO (APLL is off.)

B5: Modulation on/off control
1/modulation OFF (with phase fixed)
0/modulation ON.

B4, B3: Receiver input IF frequency selection
(0, 0), (0, 1): 1.2 MHz
(1, 0): 10.8 MHz
(1, 1): 10.7 MHz/10.75 MHz

B2: Transmit envelope ($I^2 + Q^2$ or $\sqrt{I^2 + Q^2}$)output selection
1/$I^2 + Q^2$ output
0/$\sqrt{I^2 + Q^2}$ output

B1, B0: Test mode selection bits. Each monitor output is output to the transmit ENV pin.
(0, 0): Transmit envelope ($I^2 + Q^2$ or $\sqrt{I^2 + Q^2}$) output
(0, 1): receiver phase detection signal output
(1, 0): receiver delay detection signal output
(1, 1): receiver AFC information output

(2) CR1 (I, Q gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0
Initial value	0	0	0	0	0	0	0	0

B7 to B4: I+/I– output gain setting, in 3 mV steps (Refer to Table-3.)

B3 to B0: Q+/Q– output gain setting, in 3 mV steps (Refer to Table-3.)

(3) CR2 (ENV gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	ENV GAIN3	ENV GAIN2	ENV GAIN1	ENV GAIN0	—	—	—	ICT0
Initial value	0	0	0	0	0	0	0	1

B7 to B4: ENV output gain adjustment (Refer to Table-3.)

B3 to B1: Not used

B0 : Device test control bit.

Table-3 I, Q, and ENV Output Gain Values

CR1-B7 CR1-B3 CR2-B7	-B6 -B2 -B6	-B5 -B1 -B5	-B4 -B0 -B4	Description
0	1	1	1	Amplitude 1.042 × Reference value
0	1	1	0	1.036
0	1	0	1	1.030
0	1	0	0	1.024
0	0	1	1	1.018
0	0	1	0	1.012
0	0	0	1	1.006
0	0	0	0	1.000 (Reference value)
1	1	1	1	0.994
1	1	1	0	0.988
1	1	0	1	0.982
1	1	0	0	0.976
1	0	1	1	0.970
1	0	1	0	0.964
1	0	0	1	0.958
1	0	0	0	0.952

(4) CR3 (I– output offset voltage adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B3: I– output pin offset voltage adjustment (Refer to Table-4.)

B2 to B0: Not used

(5) CR4 (Q– output offset voltage adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B4: Q– output pin offset voltage adjustment (Refer to Table-4.)

B3 to B1: Not used

Table-4 I and Q Channel Offset Adjustment Values

CR3-B7 / CR4-B7	B6	B5	B4	B3	Description	CR3-B7 / CR4-B7	B6	B5	B4	B3	Description
0	1	1	1	1	Offset +45 mV	1	1	1	1	1	Offset –3 mV
0	1	1	1	0	+42 mV	1	1	1	1	0	–6 mV
0	1	1	0	1	+39 mV	1	1	1	0	1	–9 mV
0	1	1	0	0	+36 mV	1	1	1	0	0	–12 mV
0	1	0	1	1	+33 mV	1	1	0	1	1	–15 mV
0	1	0	1	0	+30 mV	1	1	0	1	0	–18 mV
0	1	0	0	1	+27 mV	1	1	0	0	1	–21 mV
0	1	0	0	0	+24 mV	1	1	0	0	0	–24 mV
0	0	1	1	1	+21 mV	1	0	1	1	1	–27 mV
0	0	1	1	0	+18 mV	1	0	1	1	0	–30 mV
0	0	1	0	1	+15 mV	1	0	1	0	1	–33 mV
0	0	1	0	0	+12 mV	1	0	1	0	0	–36 mV
0	0	0	1	1	+9 mV	1	0	0	1	1	–39 mV
0	0	0	1	0	+6 mV	1	0	0	1	0	–42 mV
0	0	0	0	1	+3 mV	1	0	0	0	1	–45 mV
0	0	0	0	0	0 mV	1	0	0	0	0	–48 mV

(6) CR5

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	BSTO ENBL	ICT6	ICT5	ICT4	LOCAL INV1	LOCAL INV0	CLK SEL1	CLK SEL0
Initial value	0	0	0	0	0	0	0	0

B7: Modulator burst window output enable bit.
1/The timing of the I and Q baseband modulation output burst is output at the TXCO pin.
0/The 384 kHz transmit timing clock pulse is output at the TXCO pin.

B6 to B4: ICT6 to ICT4. Device test control bits.

B3, B2: Local inverting mode setting bits.
(1, 1) = local inverting mode
(0, 0) = normal mode

B1: Clock pulse shaping mode selection bit.
1/Clock pulse shaping mode (Refer to Fig 9.)
0/Oscillator circuit mode

B0: Power-on control bit for X1, X2 pins, when the clock pulse shaping mode.
1/ Always power-on
0/ Power-down in the whole device power-down state when Power on otherwise.

Note: CR5 – B6 to B4 are used to test the device. They should be set to "0" during normal operation.

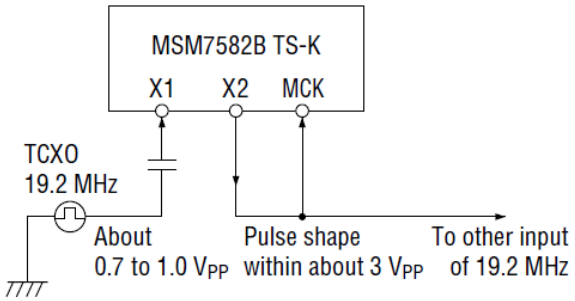


Figure 9 Example of Application Circuit when the Clock Pulse Shaping Mode is Generated by CR5-B1

State Transition Time

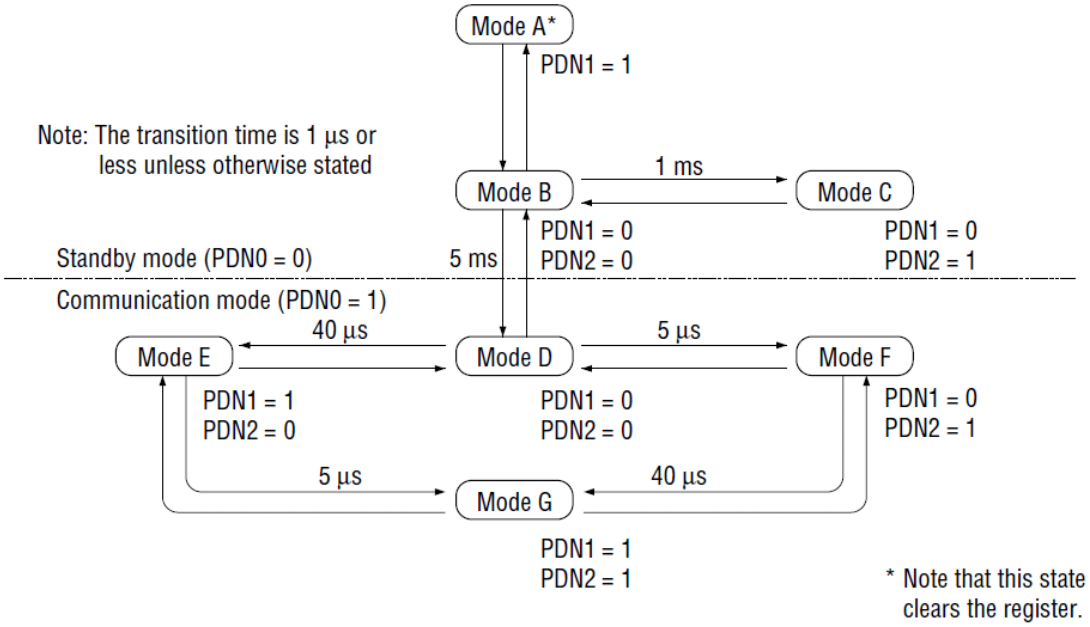


Figure 10 Power-Down State Transition Time

APPLICATION CIRCUIT

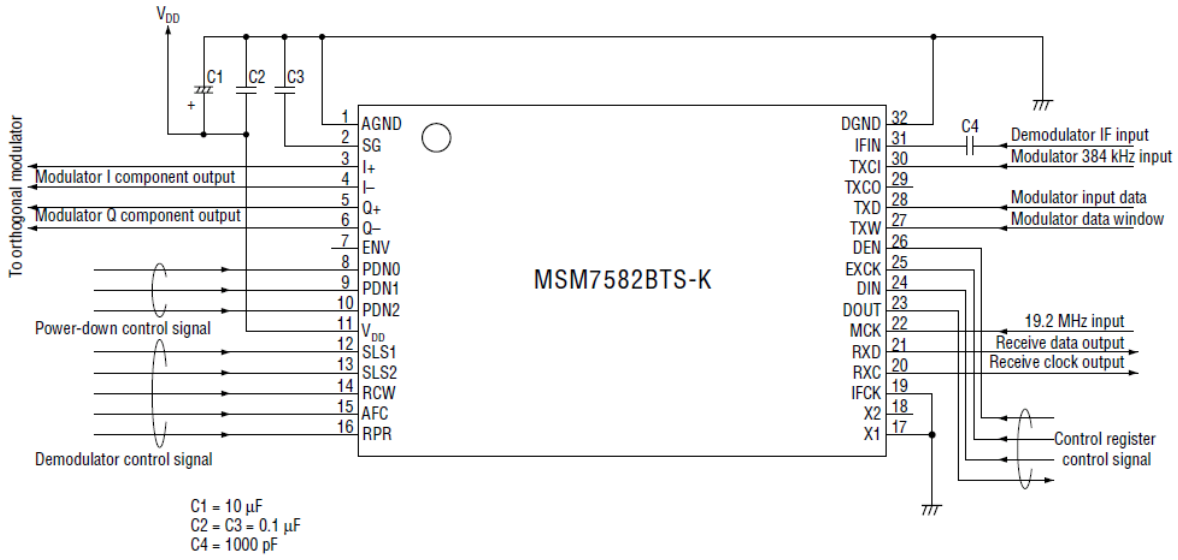
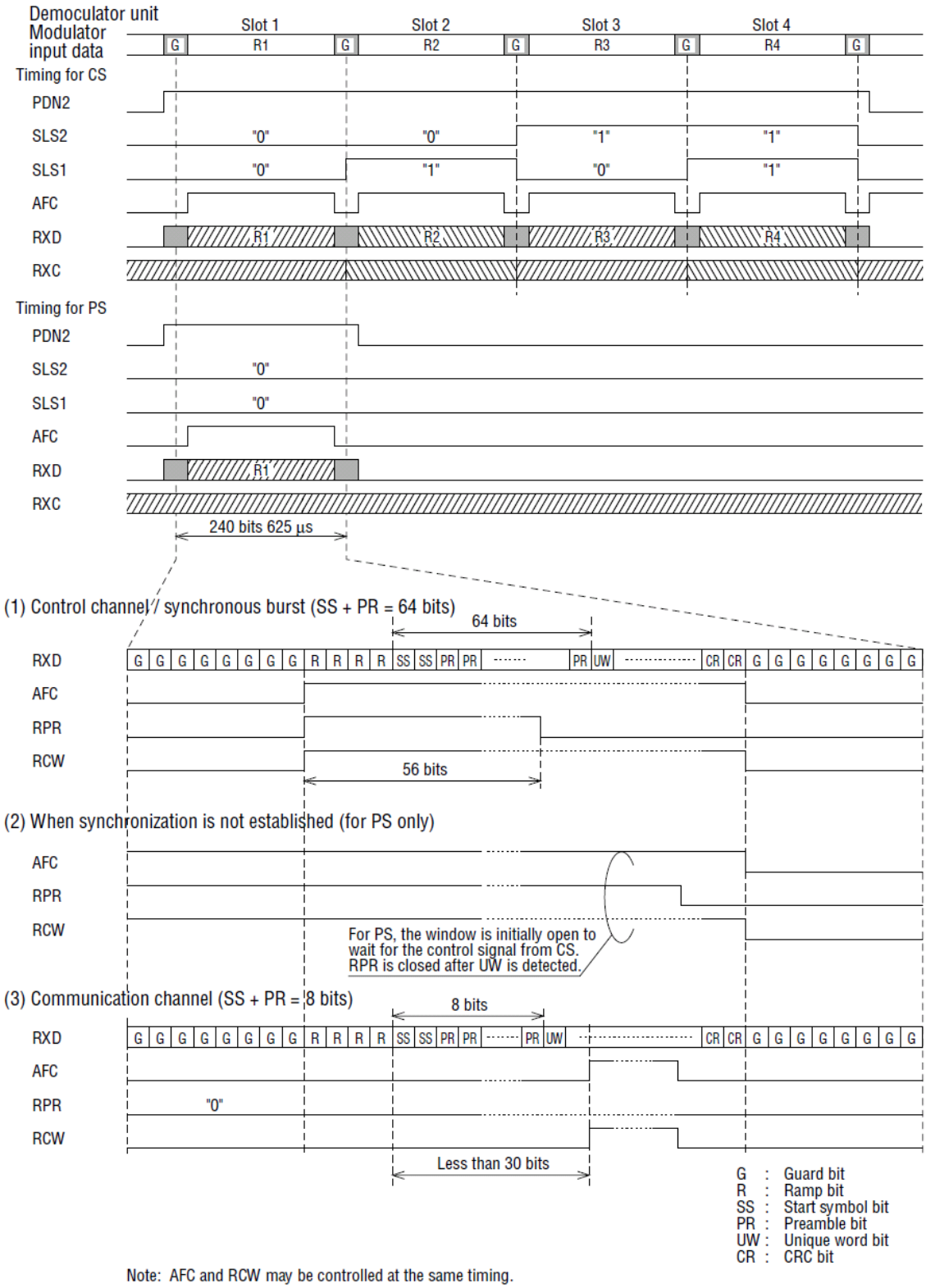


Figure 11 Example of Circuit Configuration

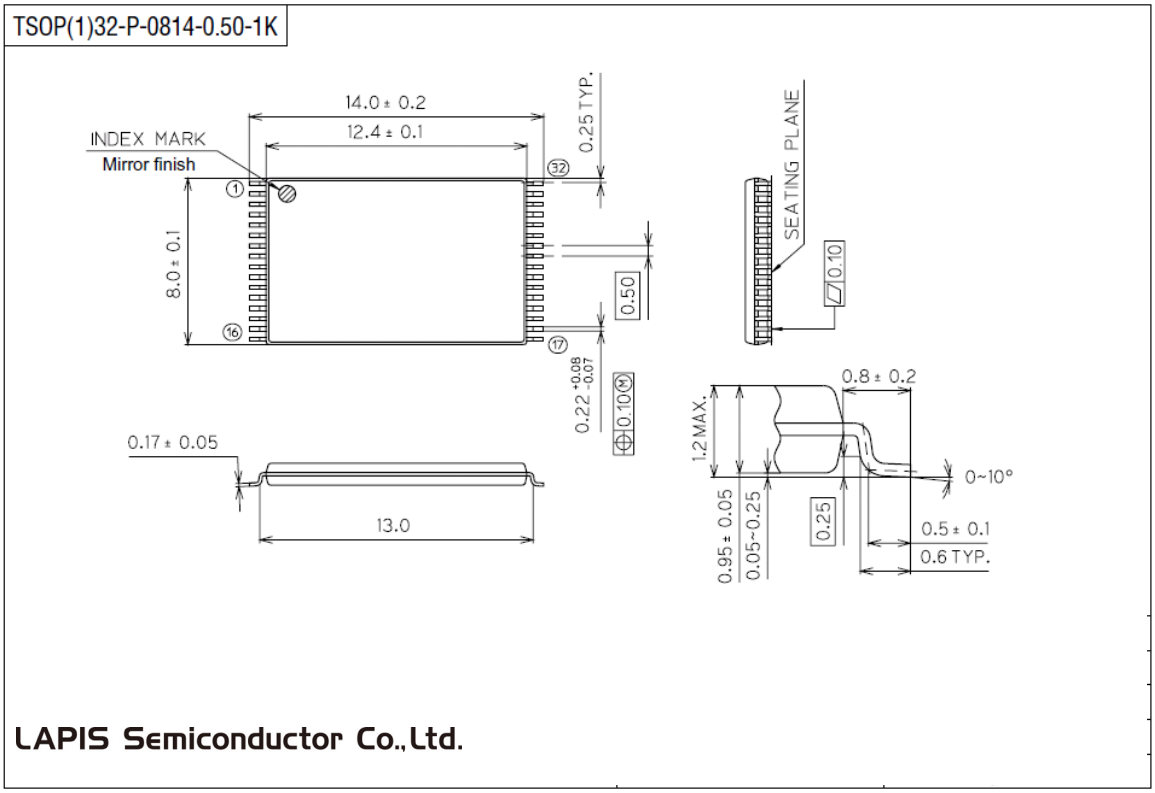
Demodulator Control Timing Diagram (Example)



Note: AFC and RCW may be controlled at the same timing.

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7582B-02	Nov. 2001	–	–	Final edition 2
FEDL7582B-03	Jul. 2004	–	–	Final edition 3
		13	13	Partially changed the Transmitter Digital Input/Output Setting Time..
FEDL7582B-04	Jun. 8, 2007	13	13	Added t_{M12} Corrected values of Serial Port Digital Input/Output Setting Time
		15	15	Added t_{M12} Corrected Figure 8 Serial Control Port Interface
FEDL7582B-05	Oct. 13, 2011	–	–	Company Name Change
FEDL7582B-06	Jun. 21, 2012	–	–	Modification of property information

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