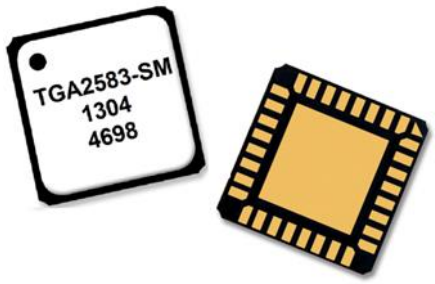
TGA2583-SM

2.7 to 3.7GHz, 10W GaN Power Amplifier

Applications

- Commercial and Military Radar

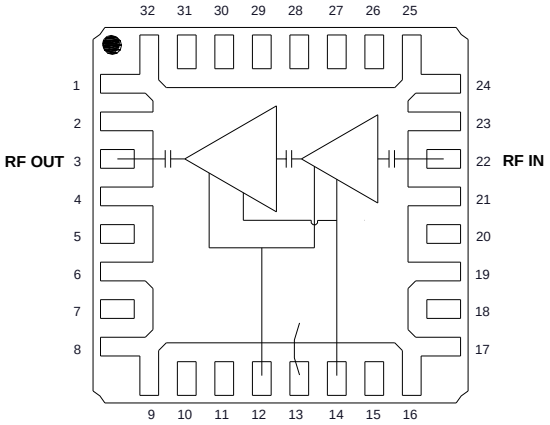


QFN 5x5 mm 32L

Product Features

- Frequency Range: 2.7 - 3.7 GHz
- P_{SAT}: 40.5 dBm
- PAE: > 50 %
- Small Signal Gain: 33 dB
- Return Loss: > 12 dB
- Bias: V_D = 25 - 32 V (CW or Pulsed), I_{DQ} = 175 mA, V_G = −2.3 V Typical
- Pulsed V_D: PW = 100 us, DC = 10 %
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Functional Block Diagram



General Description

TriQuint's TGA2583-SM is a packaged MMIC power amplifier which operates from 2.7 to 3.7 GHz. The TGA2583-SM is designed using TriQuint's production 0.25-µm GaN on SiC process.

The TGA2583-SM typically provides 40.5 dBm of saturated output power, > 50% power-added efficiency, and 33 dB small signal gain. It can operate under both pulse and CW conditions.

The TGA2583-SM is available in a low-cost, surface mount 32 lead 5x5 AIN QFN. It is ideally suited to support both commercial and defense related radar applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

Lead-free and RoHS compliant

Evaluation Boards are available upon request.

Pin Configuration

Pad No.	Symbol
1, 3-4, 6, 8-9, 13, 16-17, 19, 21, 23-25, 32	GND
3	RF OUT
5, 7, 10-11, 15, 18, 20, 26-31	NC
12	DRAIN
14	GATE
22	RF IN

Ordering Information

Part	ECCN	Description
TGA2583-SM	EAR99	2.7 - 3.7 GHz, 10 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	−8 to 0 V
Drain Current (I_D)	1530 mA
Gate Current (I_G)	−5.4 to 11.5 mA
Power Dissipation (P_{DISS}), 85°C	27 W
Input Power (P_{IN}), CW, 50 Ω, 85°C	30 dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D = 28 V, 85°C	23 dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	260°C
Storage Temperature	−55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	25 – 32 V
Drain Current (I_{DQ})	175 – 350 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 7
Gate Voltage (V_G)	−2.3 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 7

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 175 mA, V_G = −2.3 V Typ, Pulsed V_D: PW = 100 us, DC = 10 %

Parameter	Min	Typical	Max	Units
Operational Frequency Range	2.7		3.7	GHz
Small Signal Gain		33		dB
Input Return Loss		> 15		dB
Output Return Loss		12		dB
Output Power at Saturation (P_{IN} = 16 dBm)		40.5		dBm
Power-Added Efficiency (P_{IN} = 16 dBm)		> 50		%
Gain Temperature Coefficient		-0.05		dB/°C
Power Temperature Coefficient		-0.005		dBm/°C

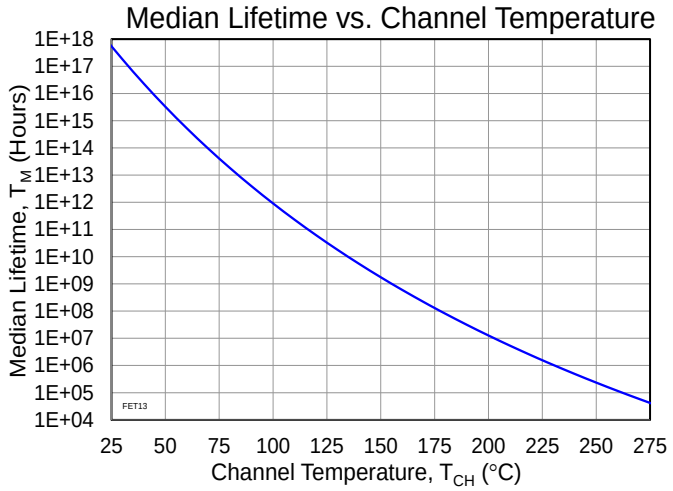
40.

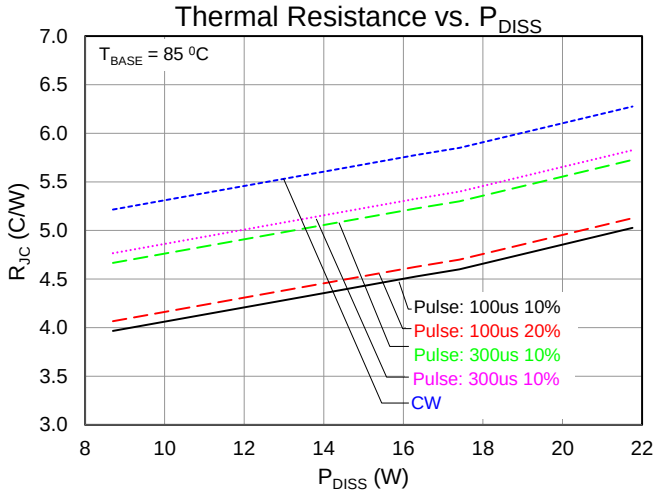
Thermal and Reliability Information

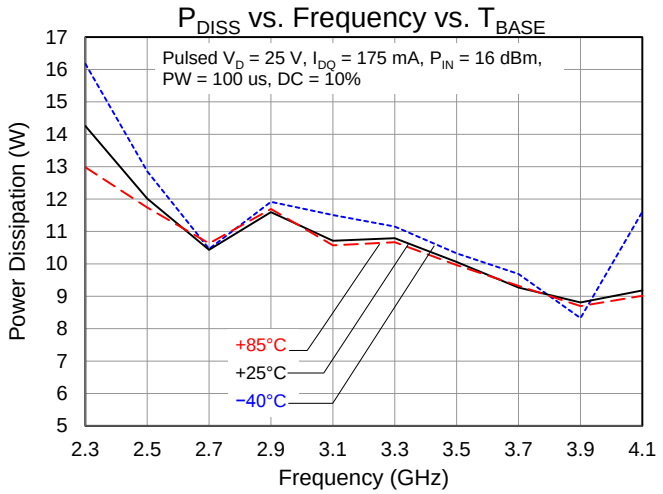
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 25 V Pulse PW = 100 us, DC = 10 % At Freq = 2.9 GHz, P_{IN} = 16 dBm: I_{DQ} = 175 mA, I_{D_Drive} = 910 mA P_{OUT} = 40.5 dBm P_{DISS} = 11.5 W	4.2	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		133	°C
Median Lifetime (T_M)		1.24E+10	Hrs

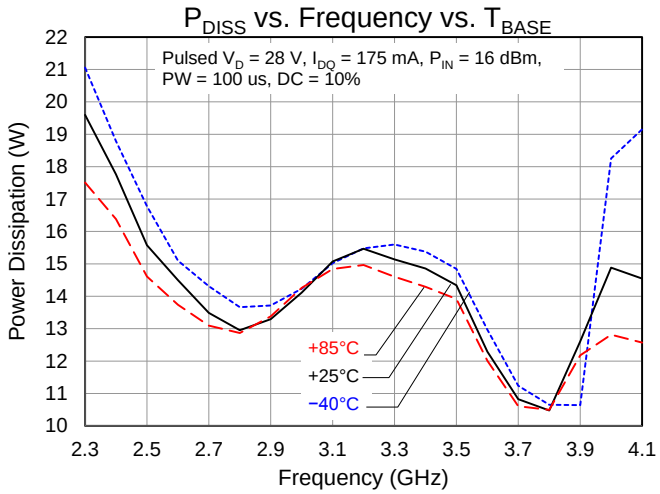
Notes:
1. Thermal resistance measured to back of package.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in $I_{D\ MAX}$





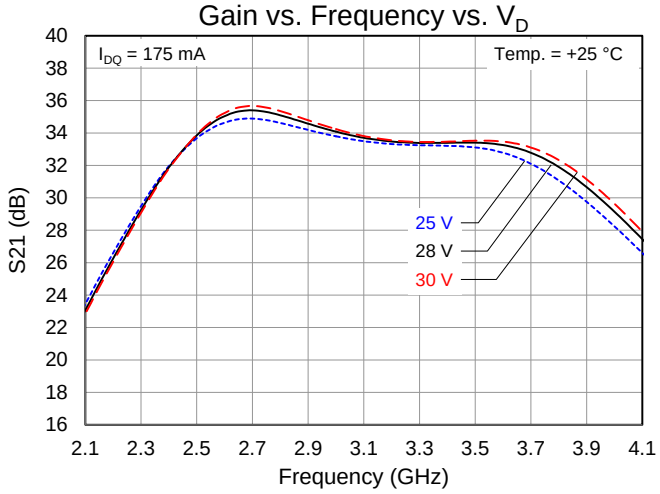




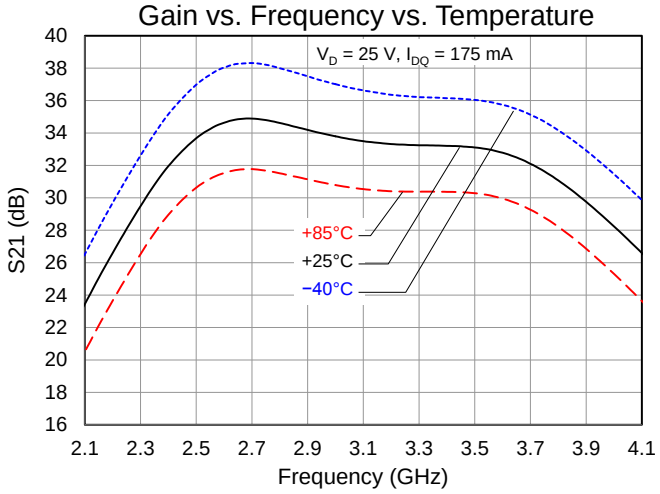
Typical Performance: Small Signal

Condition: CW

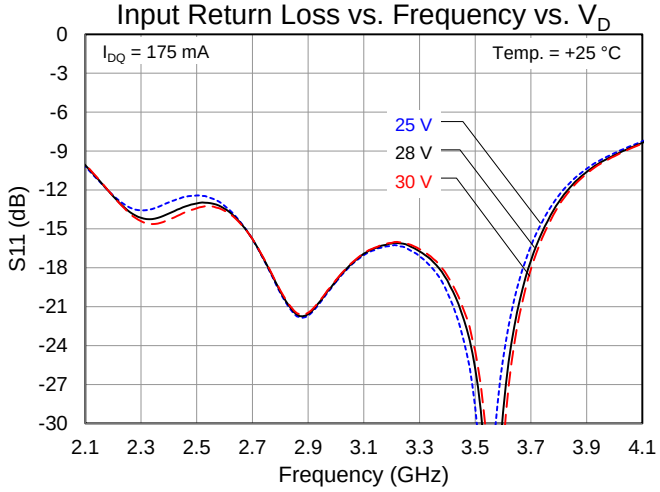
Gain vs. Frequency vs. V_D



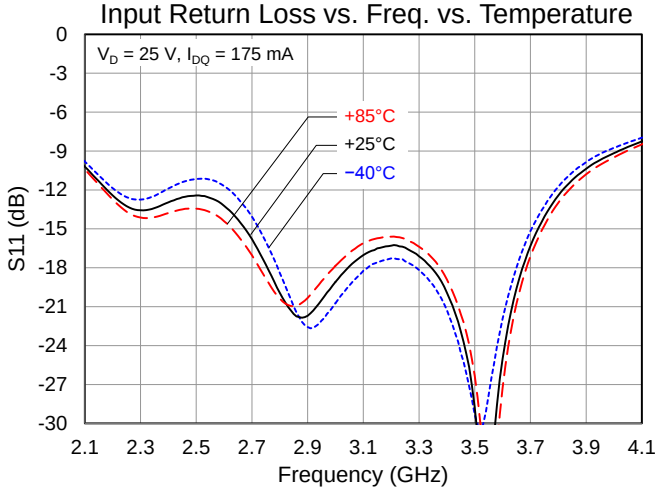
Gain vs. Frequency vs. Temperature



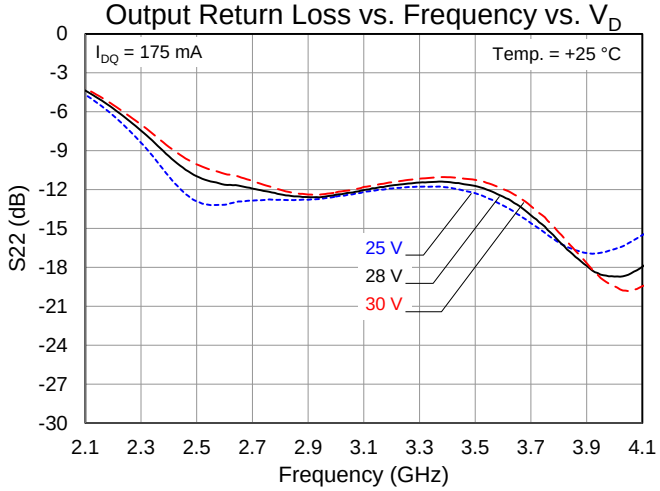
Input Return Loss vs. Frequency vs. V_D



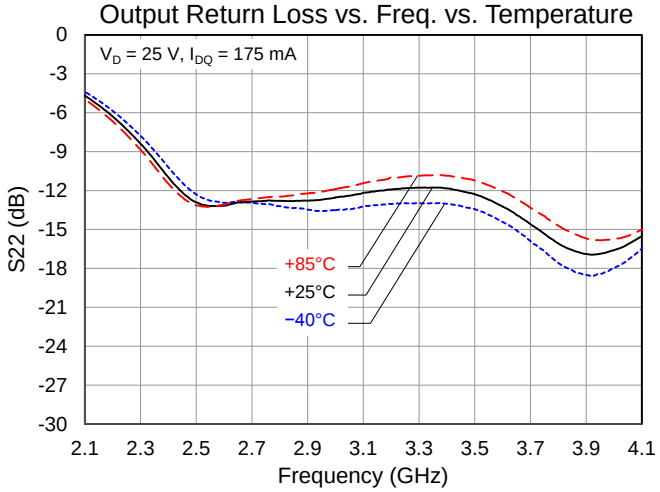
Input Return Loss vs. Freq. vs. Temperature



Output Return Loss vs. Frequency vs. V_D



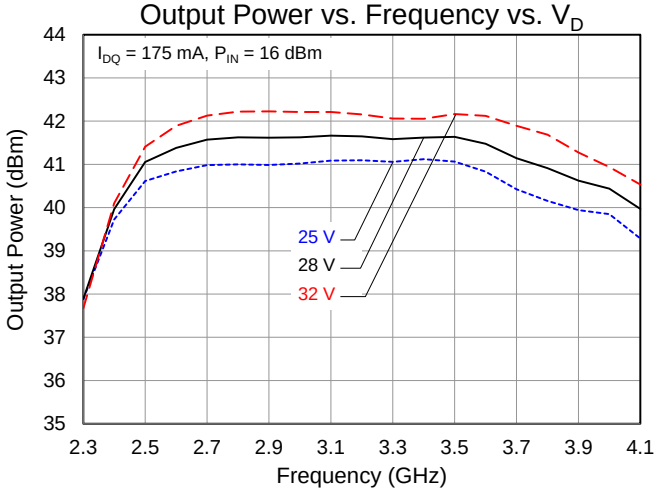
Output Return Loss vs. Freq. vs. Temperature



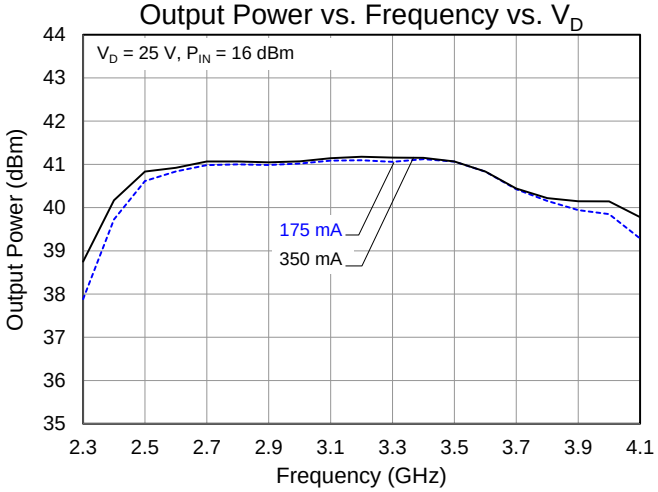
Typical Performance: Large Signal

Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

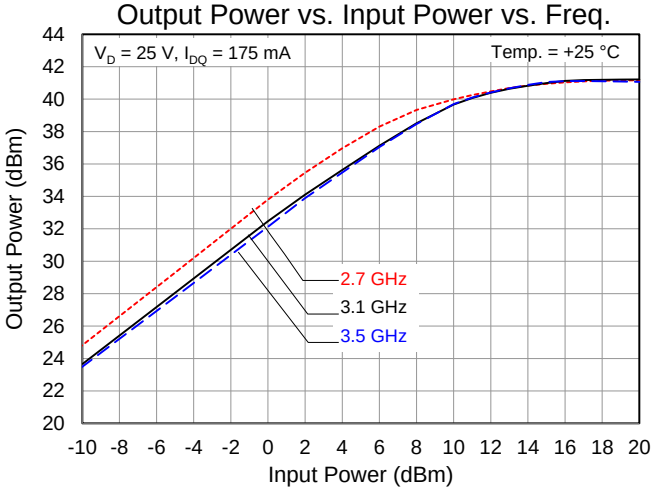
Output Power vs. Frequency vs. V_D



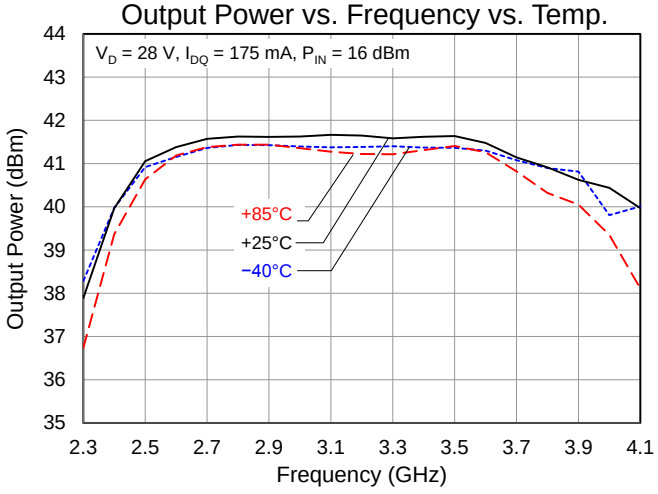
Output Power vs. Frequency vs. V_D



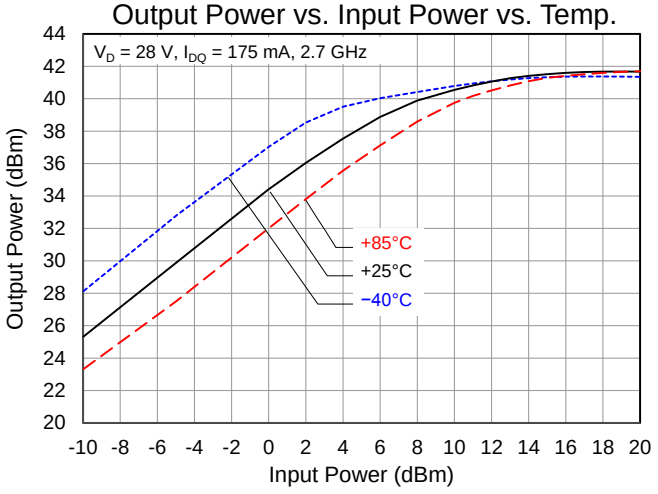
Output Power vs. Input Power vs. Freq.



Output Power vs. Frequency vs. Temp.



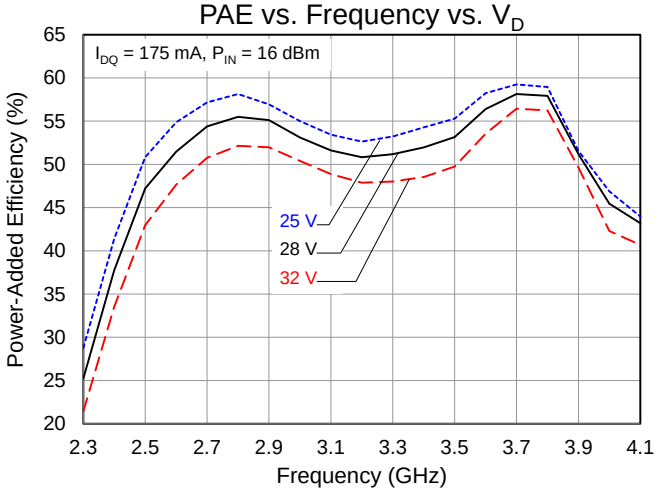
Output Power vs. Input Power vs. Temp.



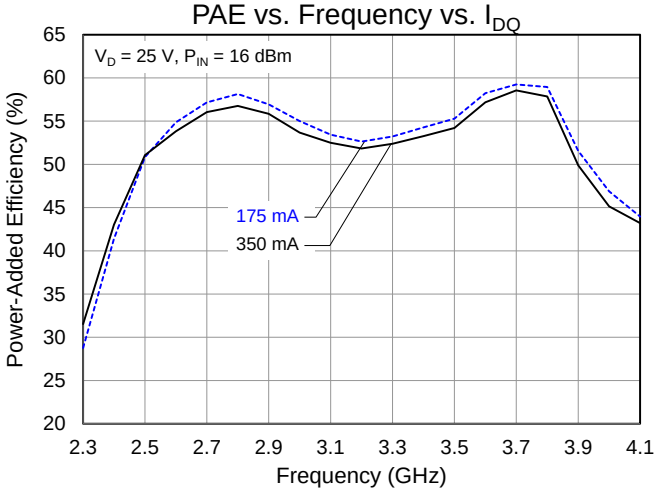
Typical Performance: Large Signal

Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

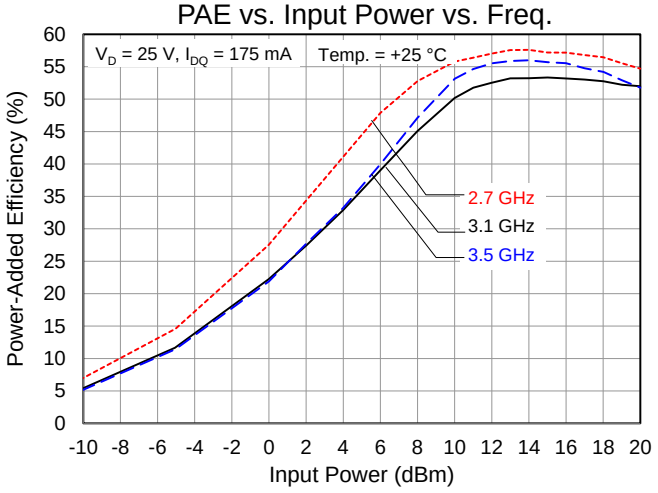
PAE vs. Frequency vs. V_D



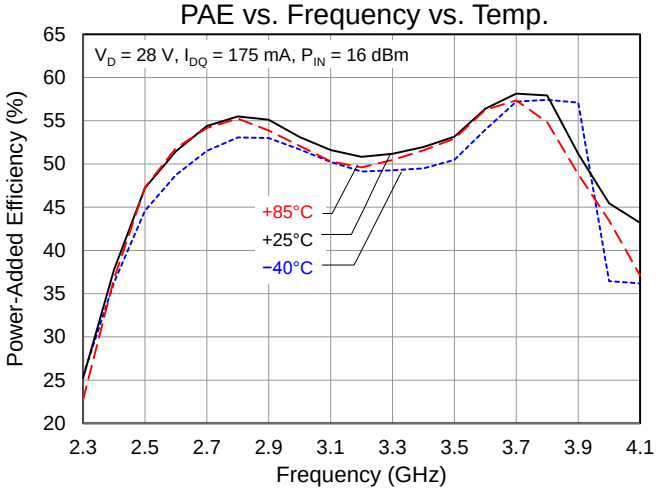
PAE vs. Frequency vs. I_{DQ}



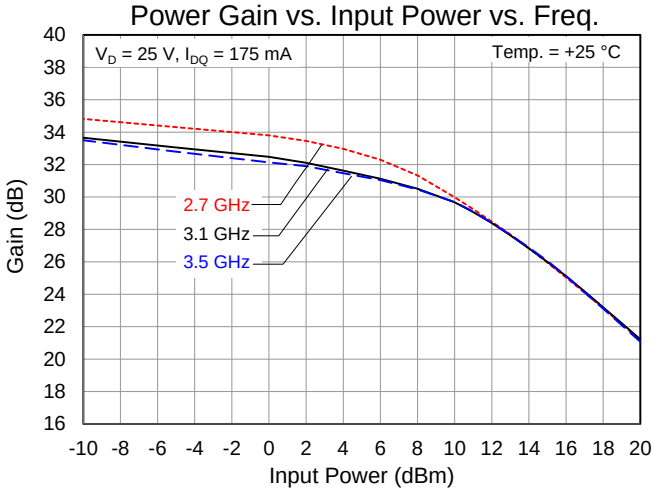
PAE vs. Input Power vs. Freq.



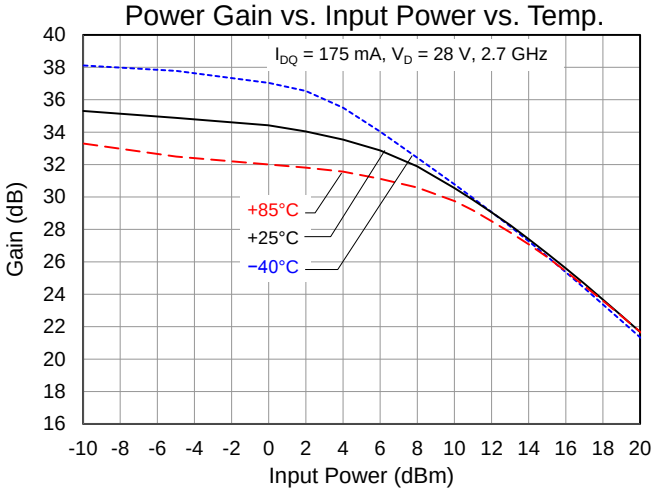
PAE vs. Frequency vs. Temp.



Power Gain vs. Input Power vs. Freq.



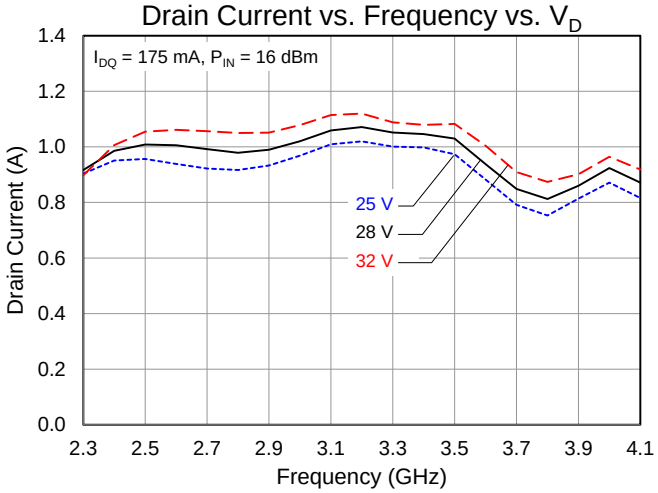
Power Gain vs. Input Power vs. Temp.



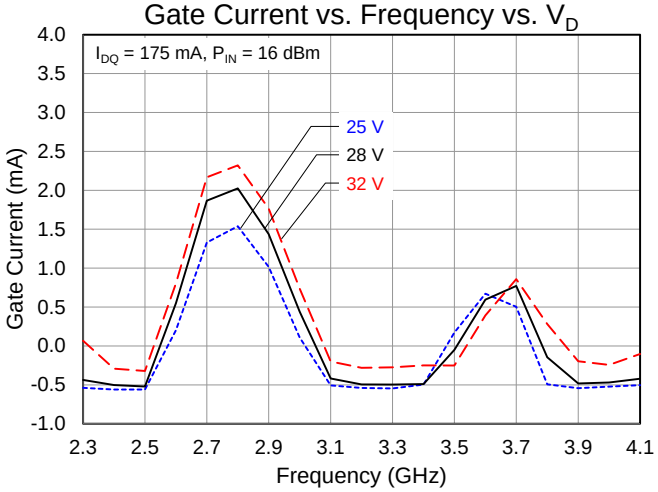
Typical Performance: Large Signal

Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

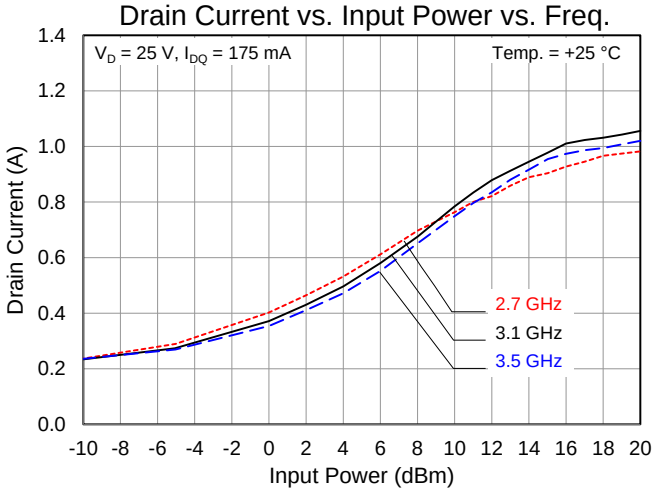
Drain Current vs. Frequency vs. V_D



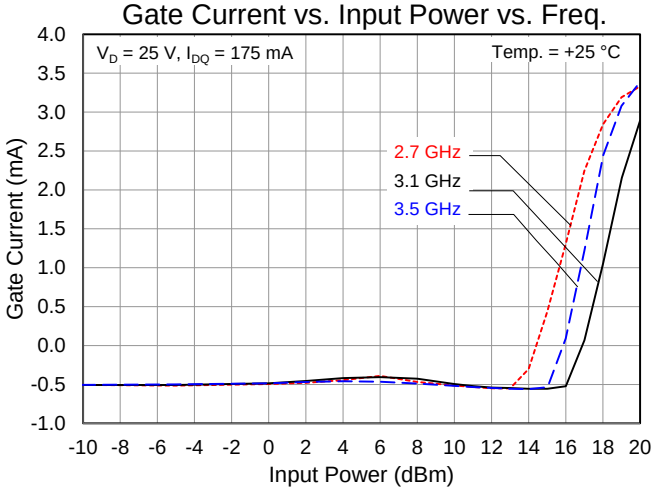
Gate Current vs. Frequency vs. V_D



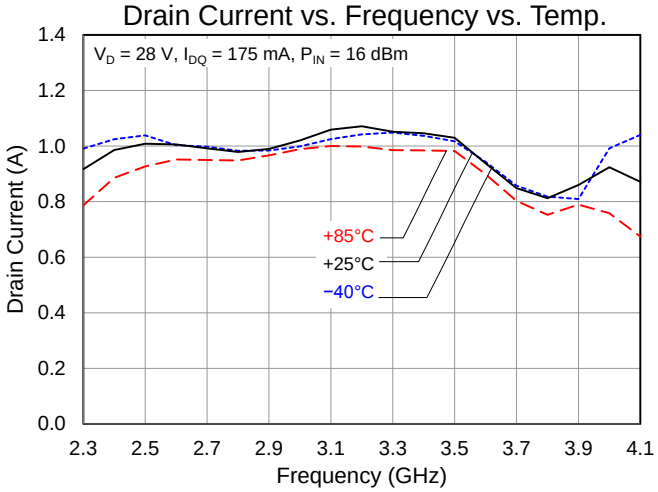
Drain Current vs. Input Power vs. Freq.



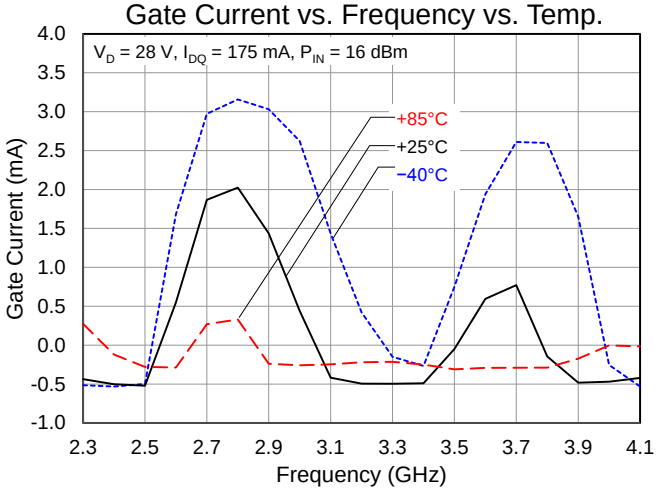
Gate Current vs. Input Power vs. Freq.



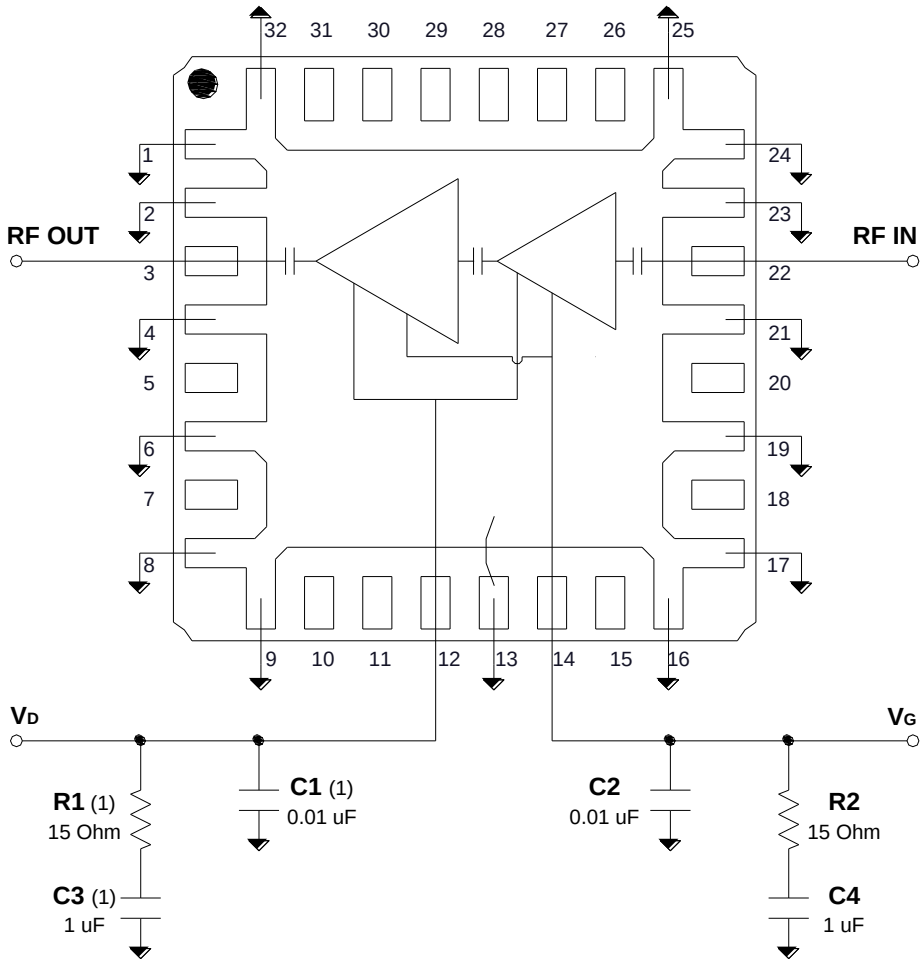
Drain Current vs. Frequency vs. Temp.



Gate Current vs. Frequency vs. Temp.



Applications Information



Notes:

1. Remove if pulsing on drain

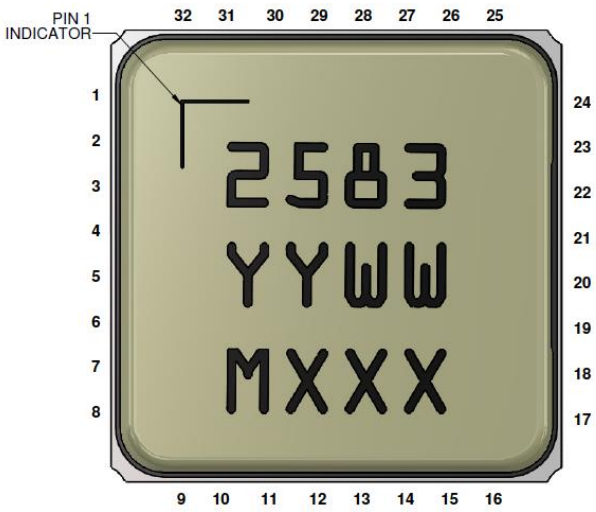
Bias-up Procedure

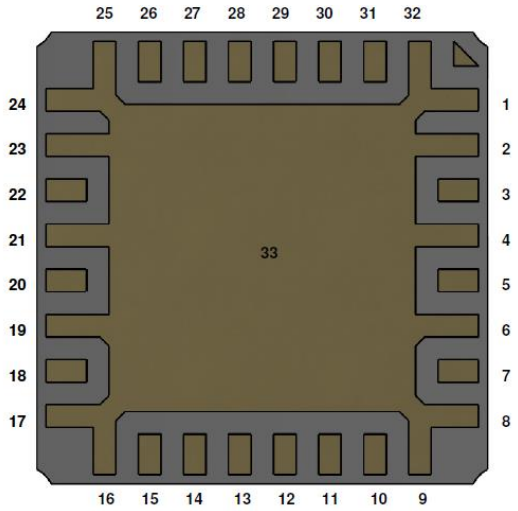
1. Set I_D limit to 1.53 A, I_G limit to 8 mA
2. Apply −5 V to V_G
3. Apply +25 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 175 mA (V_G ~ −2.3 V Typ.).
5. Turn on RF supply

Bias-down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Pin Layout

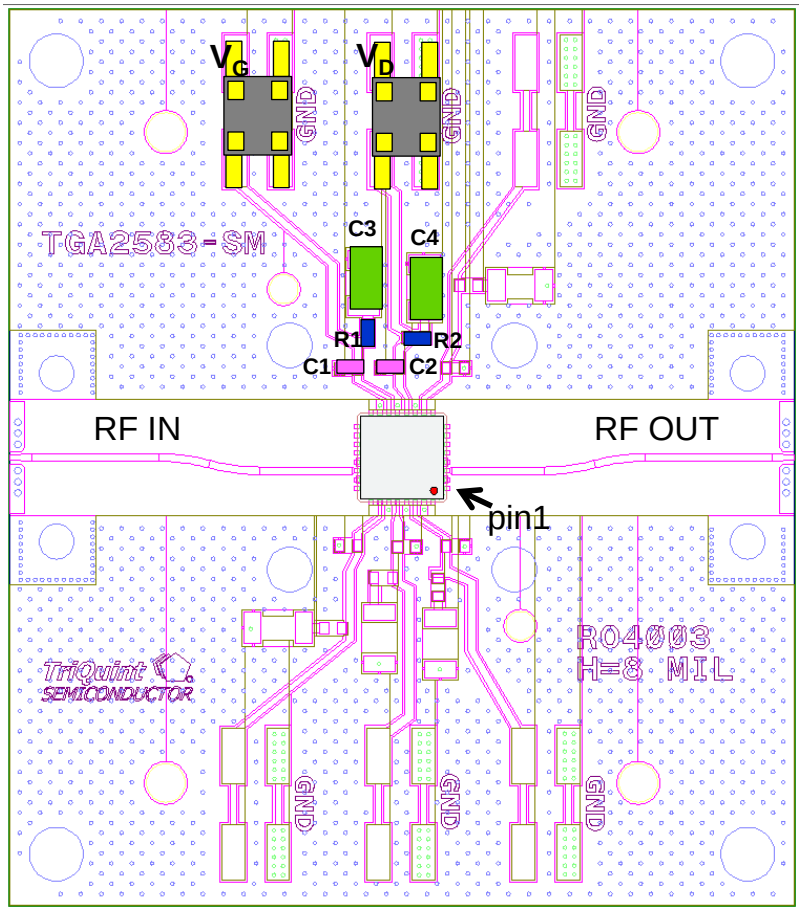


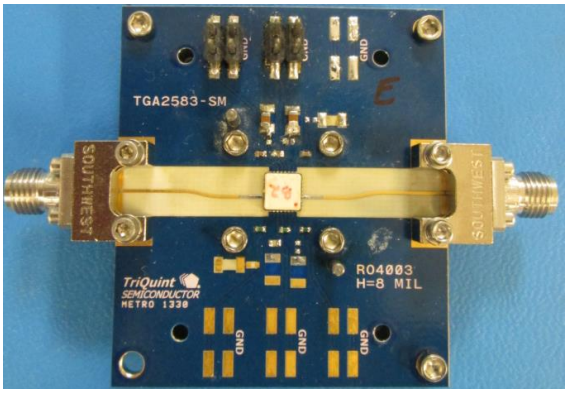


Pin Description

Pin No.	Symbol	Description
1, 3-4, 6, 8-9, 13, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB
3	RF OUT	Output; matched to 50 Ω; DC blocked
5, 7, 10-11, 15, 18, 20, 26-31	NC	No connection
12	DRAIN	Drain voltage; bias network is required; see recommended Application Information on page 8
14	GATE	Gate voltage; bias network is required; see recommended Application Information on page 8
22	RF IN	Input; matched to 50 Ω; DC blocked
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Evaluation Board

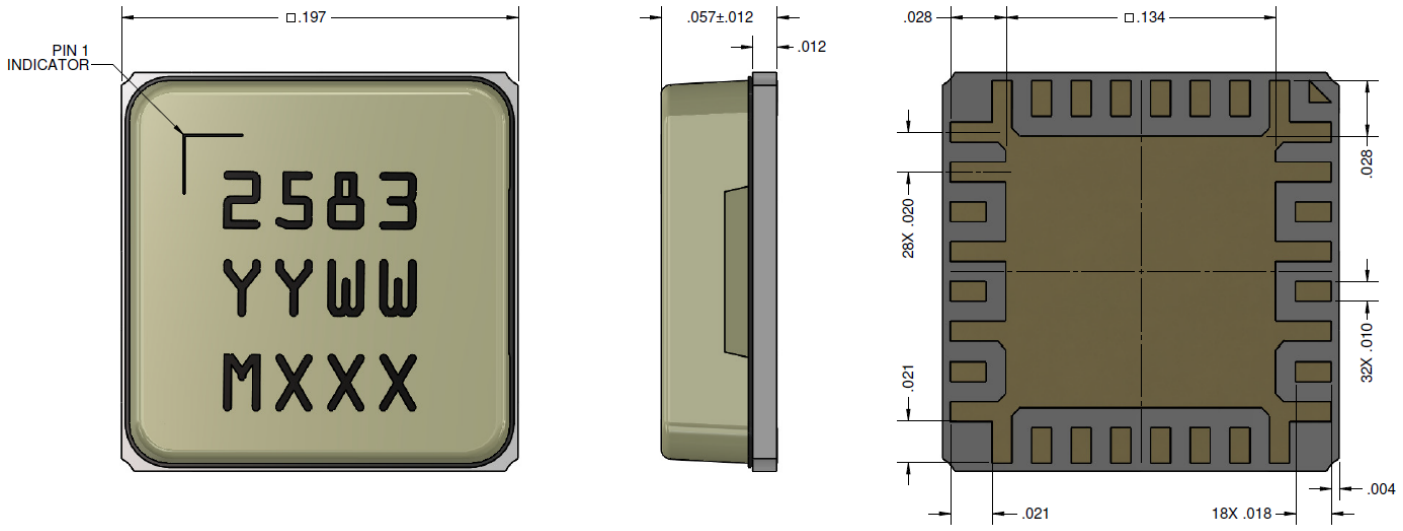




Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	0.01 µF	Cap, 0402, 50 V, 10%, X7R	Various	
C3, C4	1 µF	Cap, 0805, 50 V, 10%, X7R	Various	
R1, R2	15 Ohm	Res, 0402, 5%	Various	

Mechanical Information



Units: inches

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.005

Materials:

Base: Ceramic

Lid: Plastic

All metalized features are gold plated

Part is epoxy sealed

Marking:

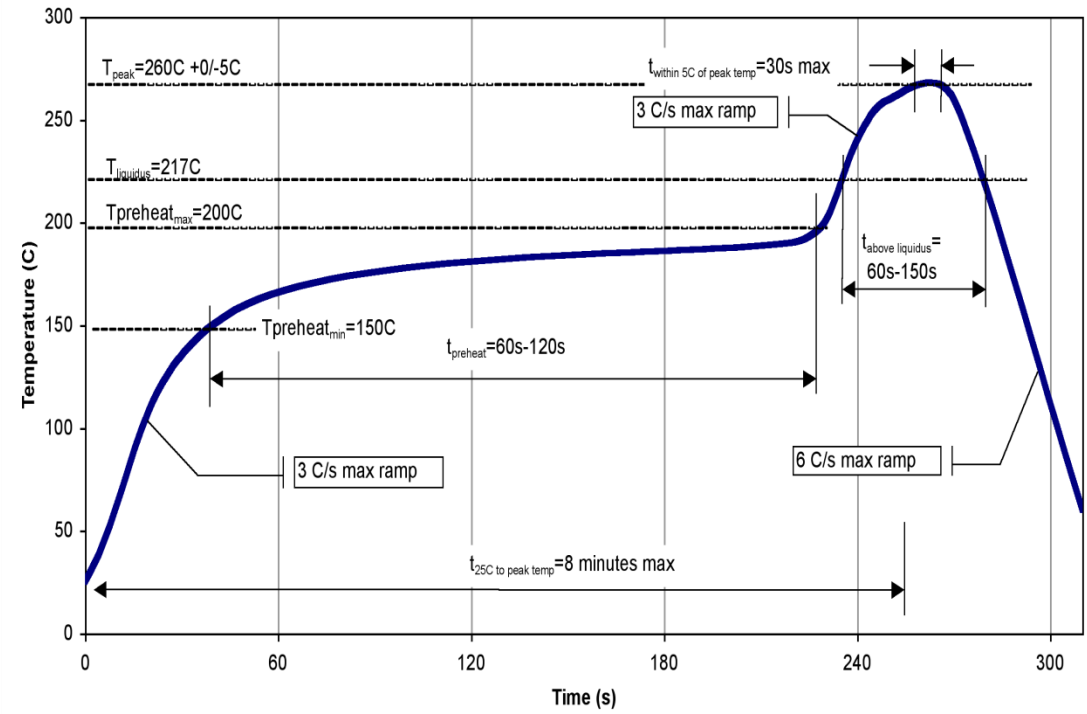
2583: Part number

YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level TBD at TBD°C convection reflow
The part is rated Moisture Sensitivity Level TBD at TBD°C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce: EAR99

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260°C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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For technical questions and application information: **Email:** info-products@triquint.com

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