

MSF2N70

700V N-Channel MOSFET

Description

The MSF2N70 is a N-channel enhancement-mode MOSFET , providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220F package is universally preferred for all commercial-industrial applications

Features

- 100% EAS Test
- Rugged Gate Oxide Technology
- Extremely Low Intrinsic Capacitances
- Remarkable Switching Characteristics
- Unequalled Gate Charge: 10.5 nC (Typ.)
- Extended Safe Operating Area

Lower RDS(ON) : 5.5 Ω (Typ.) @VGS=10V

- RoHS compliant package

Application

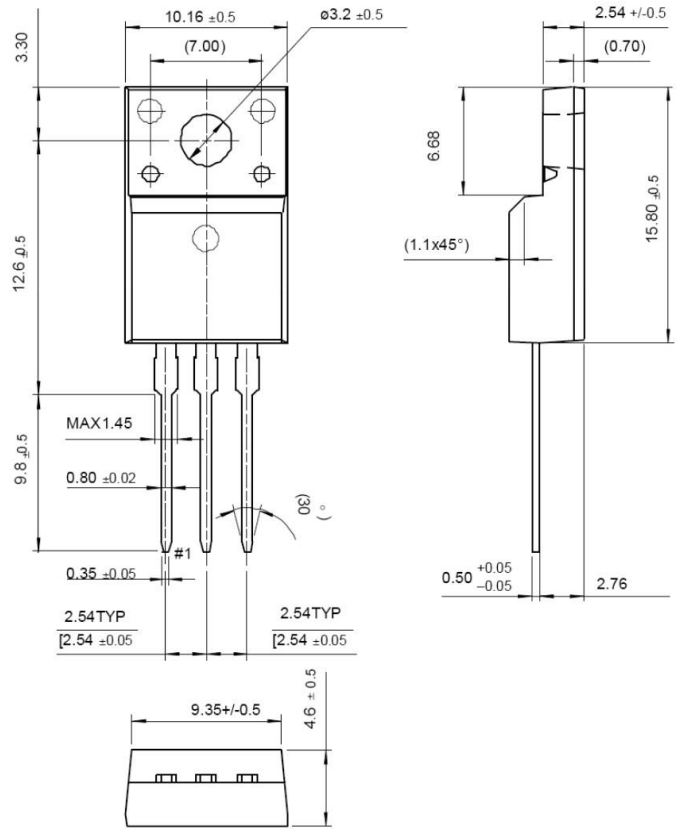
- Adapter
- Switching Mode Power Supply

Packing & Order Information

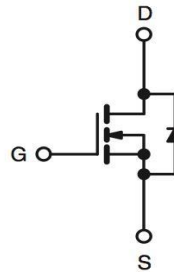
50/Tube ; 1,000/Box



RoHS
COMPLIANT



Graphic symbol



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage	700	V
V _{GS}	Gate-Source Voltage	±30	V
I _D	Drain Current -Continuous (TC=25°C)	1.6	A
	Drain Current -Continuous (TC=100°C)	1.0	A
I _{DM}	Pulsed Drain Current	6.0	A
E _{AS}	Single Pulsed Avalanche Energy	140	mJ
E _{AR}	Repetitive Avalanche Energy	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5	V/ns

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
P _D	Power Dissipation (TC=25°C)	45	W
	Power Dissipation (TC=100°C)	0.22	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

NOTE:

1. Repetitive rating; pulse width limited by maximum junction temperature.

Thermal characteristics (Tc=25°C unless otherwise noted)

Symbol	Parameter	Max.	Units
R _{thjc}	Typical thermal resistance	2.7	°C/W
R _{θJA}	Typical thermal resistance	62.5	

Static Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
V _{GS}	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
*R _{DS(ON)}	V _{GS} = 10 V, I _D = 0.8 A	--	5.5	6.0	Ω
BV _{DSS}	V _{GS} = 0 V, I _D = 250μA	700	--	--	V
ΔBV _{DSS} /ΔT _J	I _D = 250μA, Referenced to 25°C	--	0.7	--	V/°C
I _{DSS}	V _{DS} = 700 V, V _{GS} = 0 V V _{DS} = 560 V, V _{GS} = 0 V, T _J = 125°C	--	--	10 100	μA
I _{GSSF}	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA

Dynamic Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
C _{ISS}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0MHz	--	340	445	pF
C _{OSS}		--	45	60	pF
C _{RSS}		--	7.5	10	pF
t _{d(on)}	V _{DS} = 350 V, I _D = 1.6 A, R _G = 25 Ω	--	10	20	ns
t _r		--	25	50	ns
t _{d(off)}		--	20	40	ns
t _f		--	25	50	ns
Q _g	V _{DS} = 560 V, I _D = 1.6 A, V _{GS} = 10 V	--	10.5	1414	nC
Q _{gs}		--	2.0	--	
Q _{gd}		--	4.0	--	

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Source-Drain Diode Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
I_S		--	--	1.6	A
I_{SM}		--	--	6	
V_{SD}	$I_S = 1.6 \text{ A}, V_{GS} = 0 \text{ V}$	--	--	1.5	V
t_{rr}	$I_S = 1.6 \text{ A}, V_{GS} = 0 \text{ V}$	--	250	--	ns
Q_{rr}	$di/dt = 100 \text{ A}/\mu\text{s}$	--	1.2	--	μC

Notes;

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 1.6 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \text{ W}$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 1.6 \text{ A}, di/dt \leq 100 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature

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■ Characteristics Curve

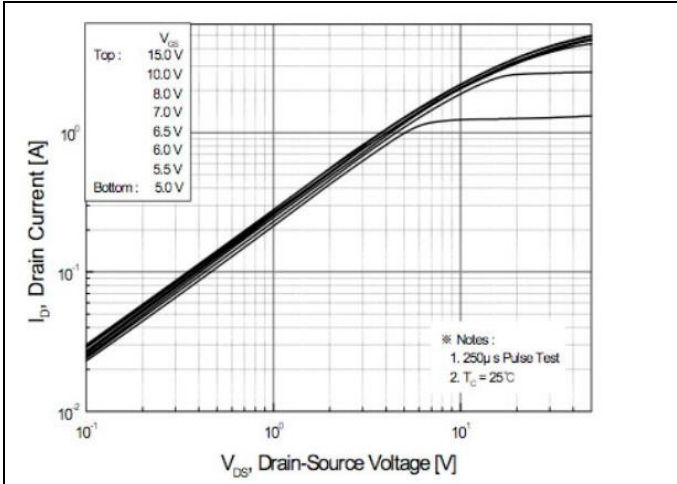


FIG.1-ON REGION CHARACTERISTICS

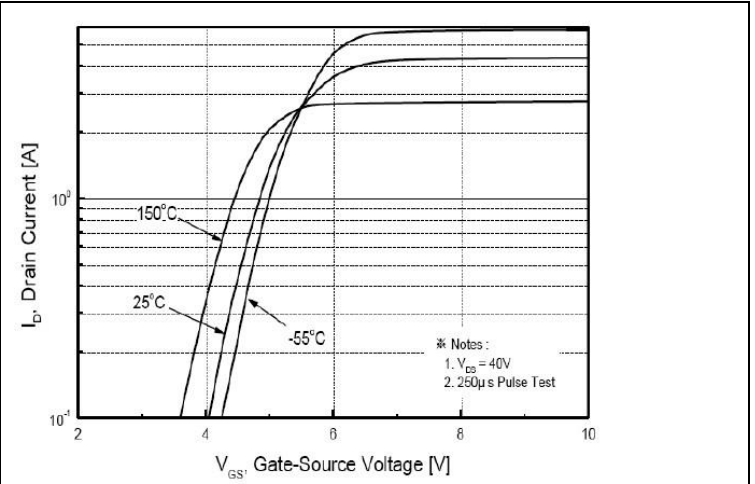


FIG.2-TRANSFER CHARACTERISTICS

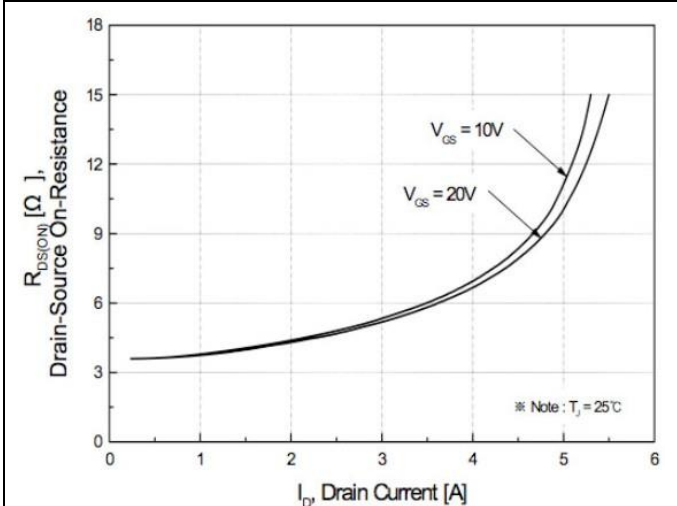


FIG.3-ON RESISTANCE VARIATION VS DRAIN CURRENT AND GATE VOLTAGE

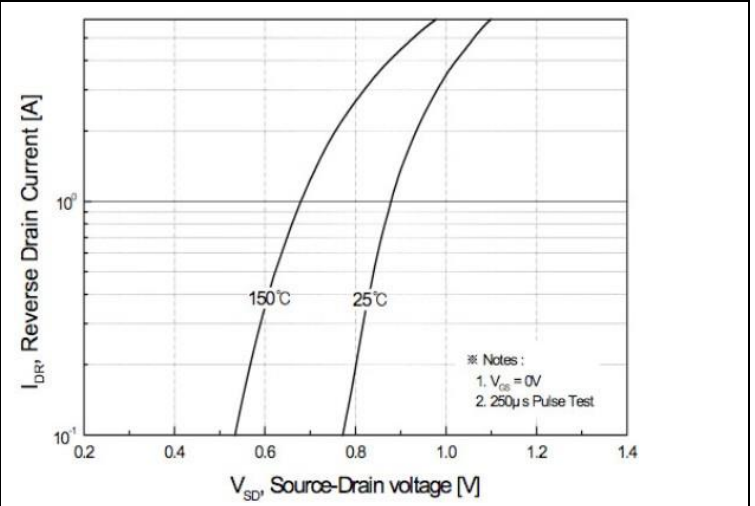


FIG.4-BODY DIODE FORWARD VOLTAGE VARIATION WITH SOURCE CURRENT AND TEMPERATURE

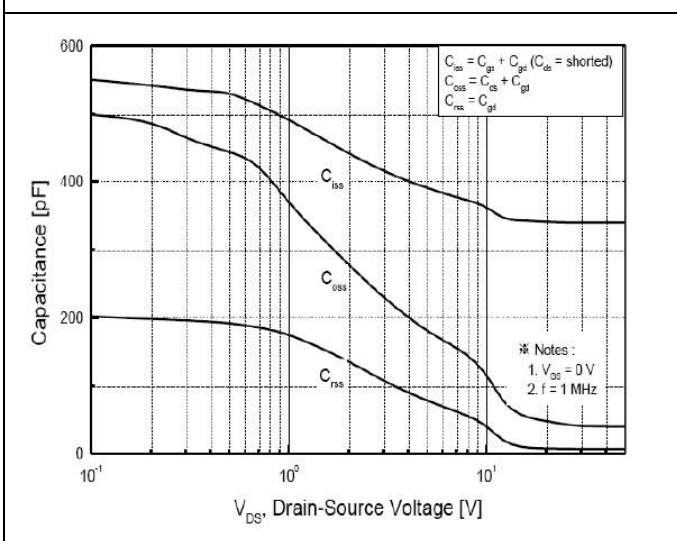


FIG.5-CAPACITANCE CHARACTERISTICS

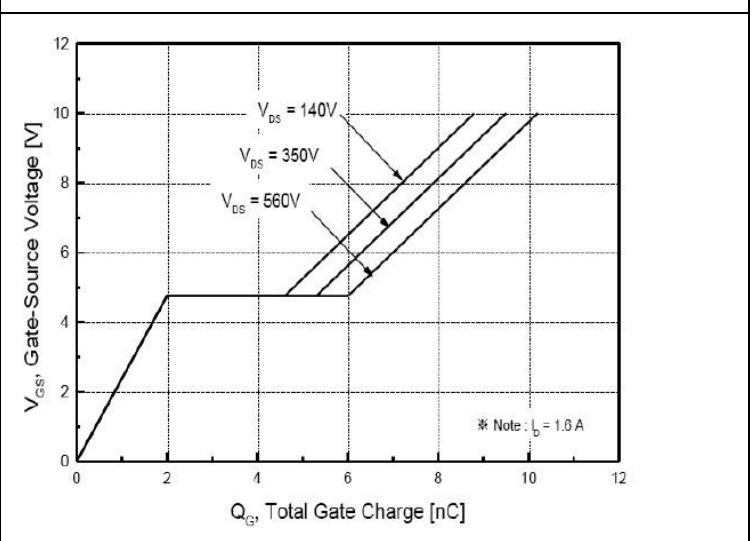


FIG.6-GATE CHARGE CHARACTERISTICS

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Characteristics Curve

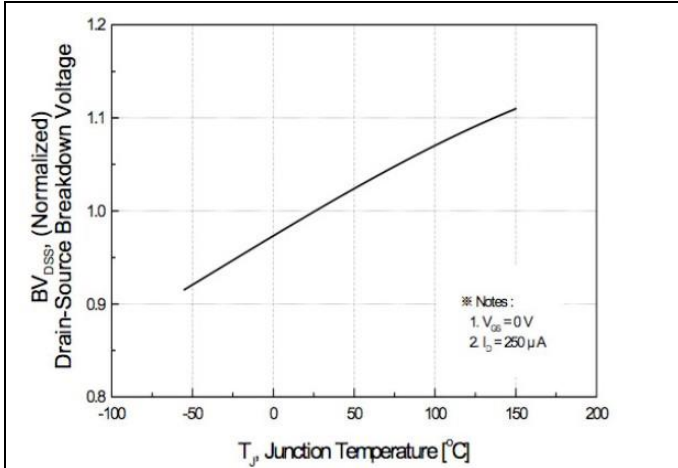


FIG.7-BREAKDOWN VOLTAGE VARIATION VS TEMPERATURE

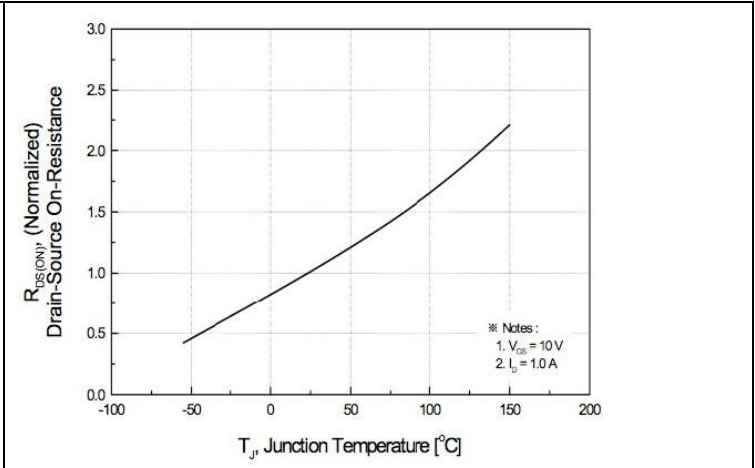


FIG.8-ON-RESISTANCE VARIATION VS TEMPERATURE

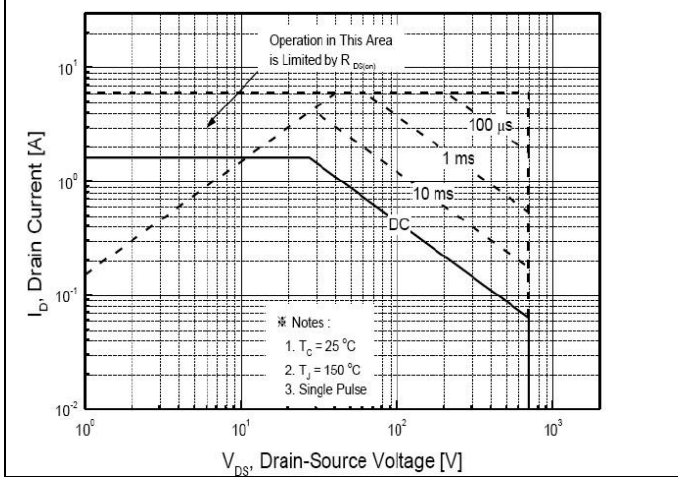


FIG.9-MAXIMUM SAFE OPERATING AREA

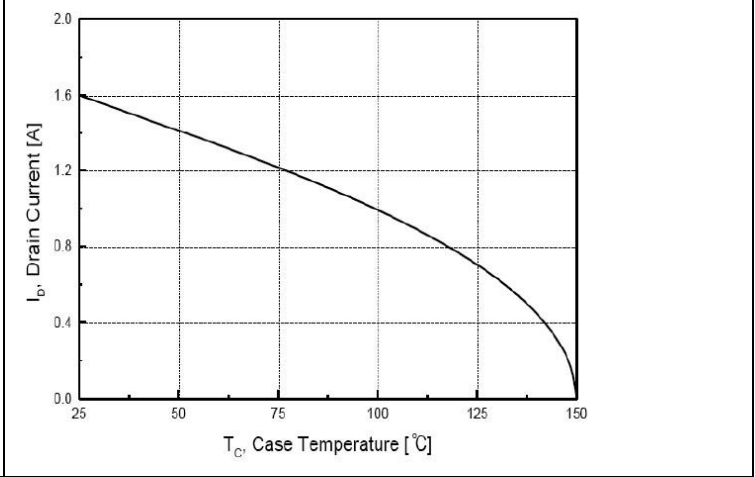


FIG.10-MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

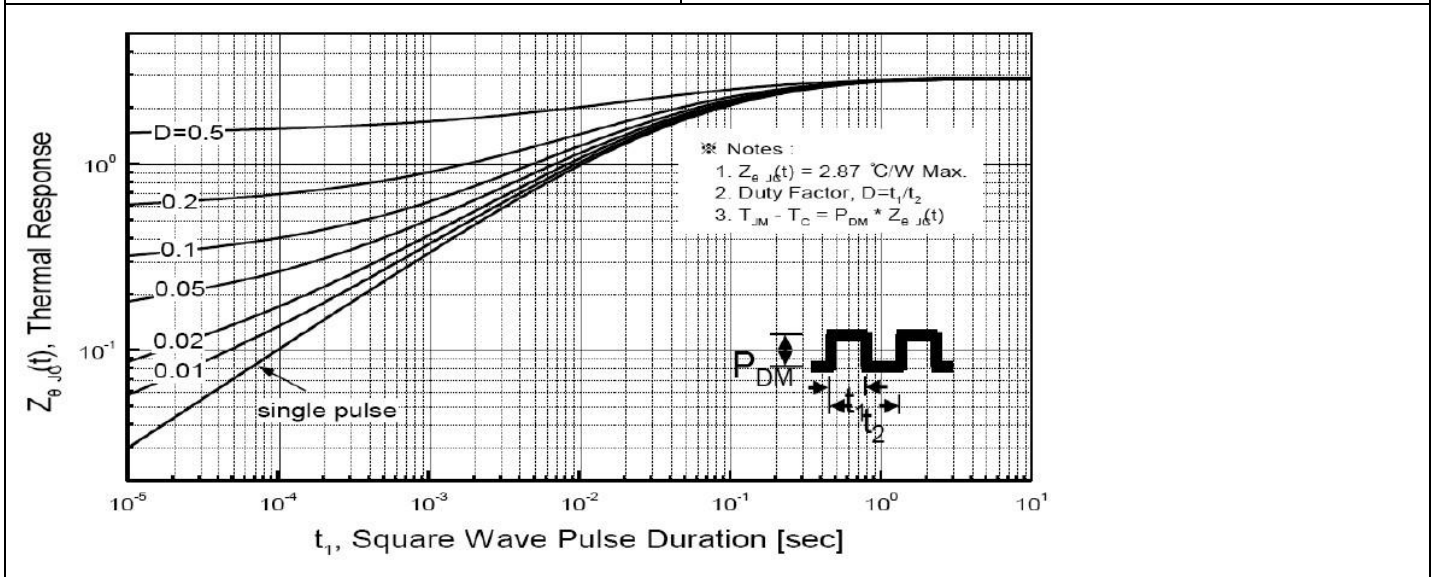


FIG.11-TRANSIENT THERMAL RESPONSE CURVE

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■ Characteristics Test Circuit & Waveform

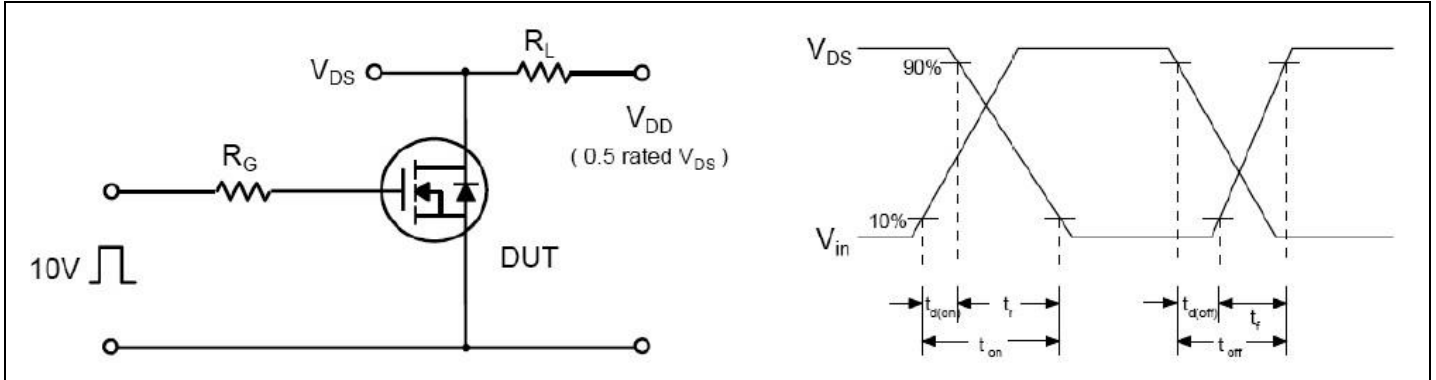


Fig 12. Resistive Switching Test Circuit & Waveforms

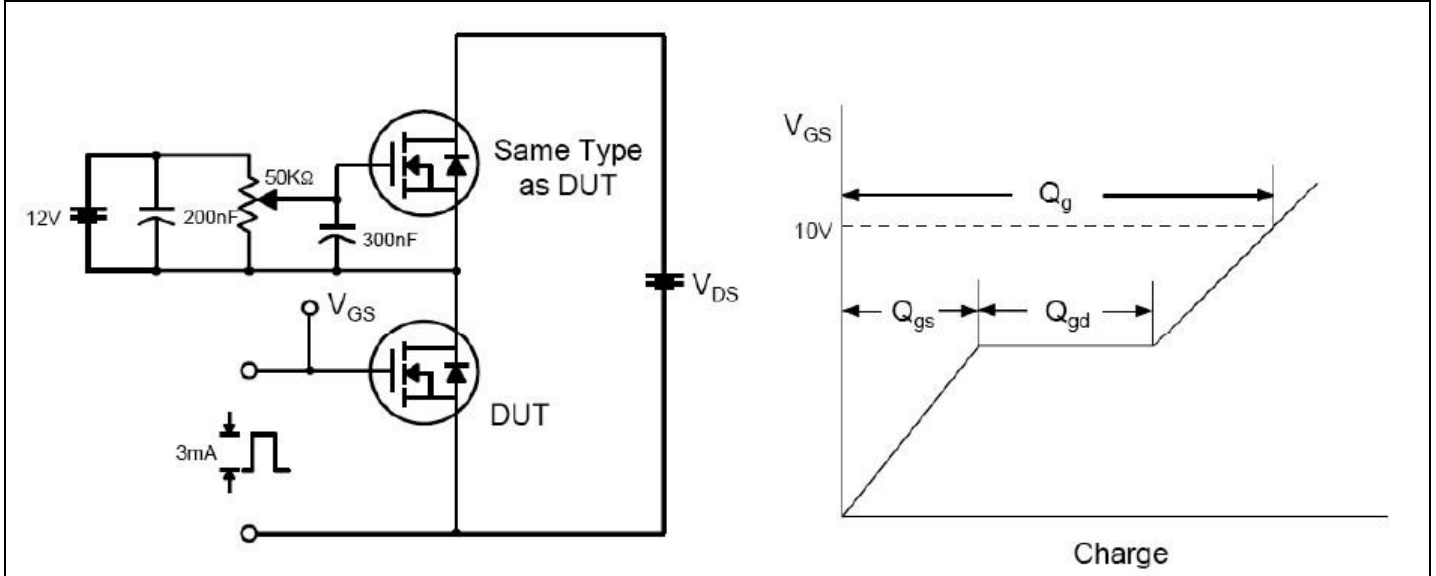


Fig 13. Gate Charge Test Circuit & Waveform

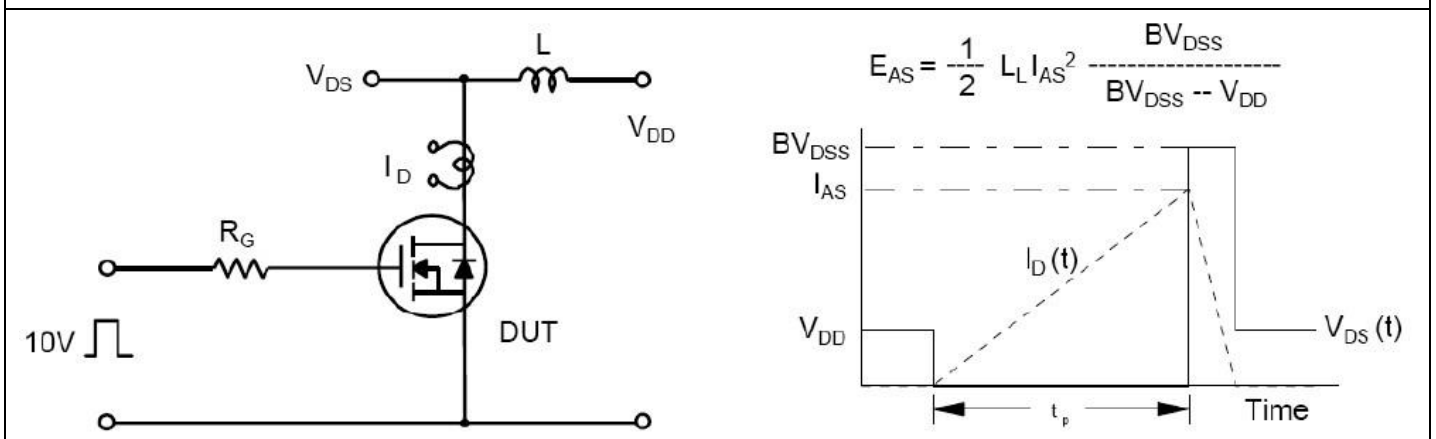


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

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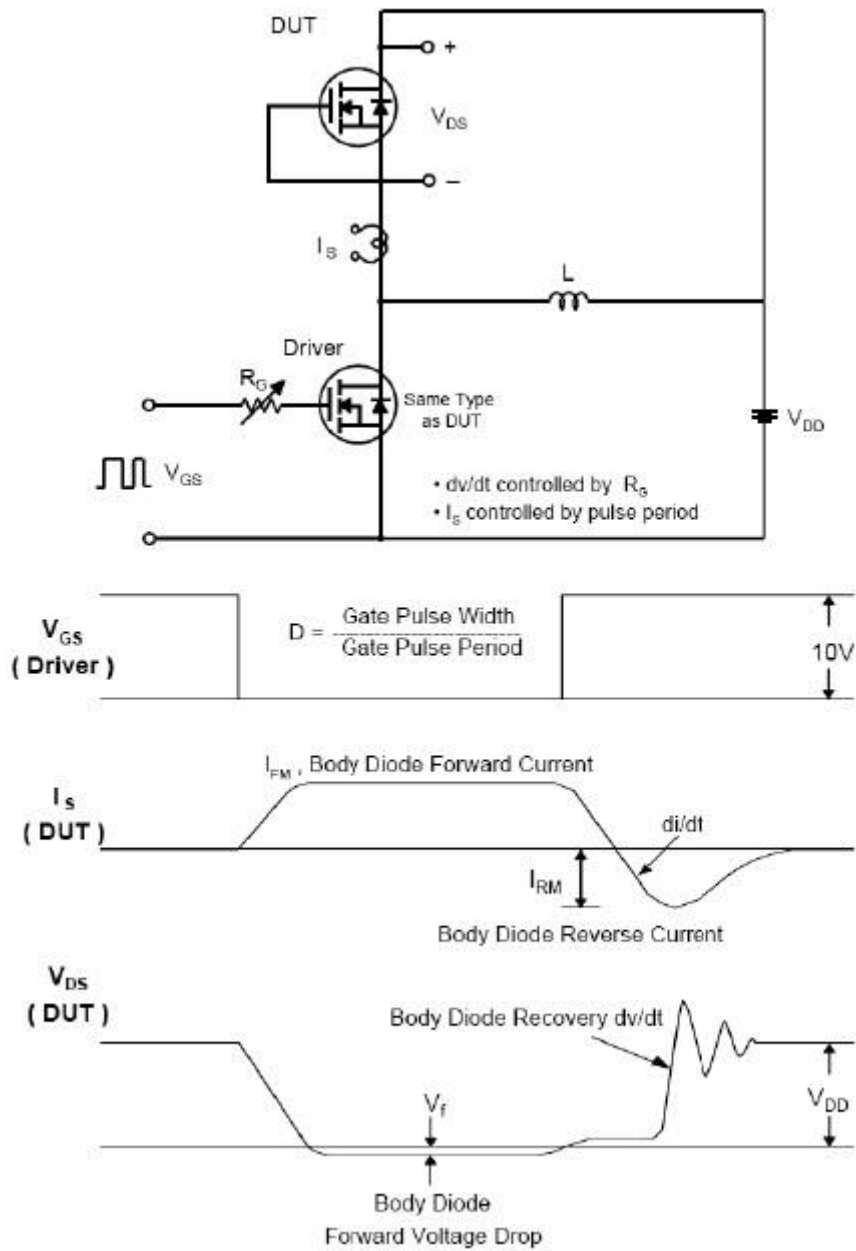


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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