

P-Channel Enhancement Mode Vertical DMOS FETs

Features

- ▶ High input impedance and high gain
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low C_{ISS} and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ Free from secondary breakdown

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Analog switches
- ▶ Power management
- ▶ Telecom switches

General Description

This low threshold enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$V_{GS(th)}$ (max) (V)
	TO-236AB (SOT-23)	TO-92			
TP2104	TP2104K1-G	TP2104N3-G	-40	6.0	-2.0

-G indicates package is RoHS compliant ('Green')



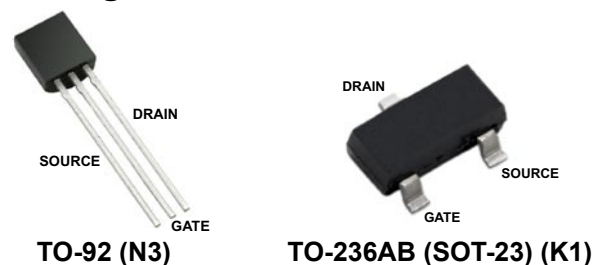
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

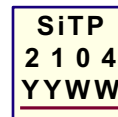
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configuration



Product Marking



YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)



W = Code for week sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-236AB (SOT-23) (K1)

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (A)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^\dagger (mA)	I_{DRM} (A)
TO-236AB (SOT-23)	-160	-0.8	0.36	200	350	-160	-0.8
TO-92	-250	-1.0	0.74	125	170	-250	-1.0

[†] I_D (continuous) is limited by max rated T_j .

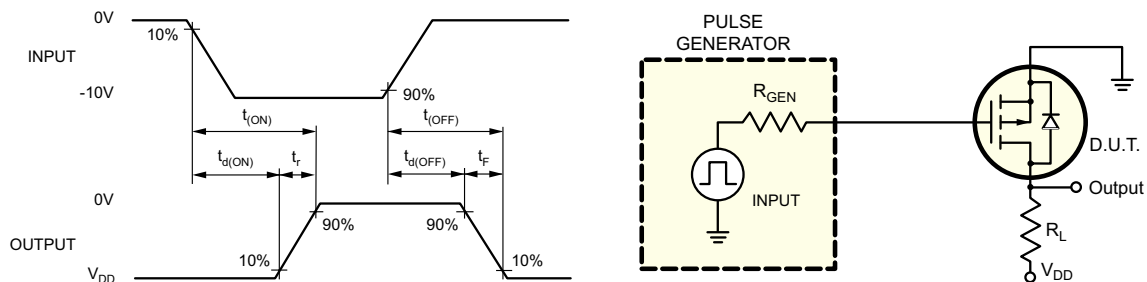
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-40	-	-	V	$V_{GS} = 0V, I_D = -1.0mA$
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.0	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	5.8	6.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate body leakage	-	-1.0	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
			-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.6	-	-	A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	10	Ω	$V_{GS} = -4.5V, I_D = -50mA$
			-	6.0		$V_{GS} = -10V, I_D = -500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.55	1.0	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -500mA$
G_{FS}	Forward transconductance	150	200	-	mmho	$V_{DS} = -25V, I_D = -500mA$
C_{ISS}	Input capacitance	-	35	60	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0 \text{ MHz}$
C_{OSS}	Common source output capacitance	-	22	30		
C_{RSS}	Reverse transfer capacitance	-	8.0	10		
$t_{d(ON)}$	Turn-on delay time	-	4.0	6.0	ns	$V_{DD} = -25V, I_D = -500mA, R_{GEN} = 25\Omega$
t_r	Rise time	-	4.0	8.0		
$t_{d(OFF)}$	Turn-off delay time	-	5.0	9.0		
t_f	Fall time	-	5.0	8.0		
V_{SD}	Diode forward voltage drop	-	-1.2	-2.0	V	$V_{GS} = 0V, I_{SD} = -500mA$
t_{rr}	Reverse recovery time	-	400	-	ns	$V_{GS} = 0V, I_{SD} = -500mA$

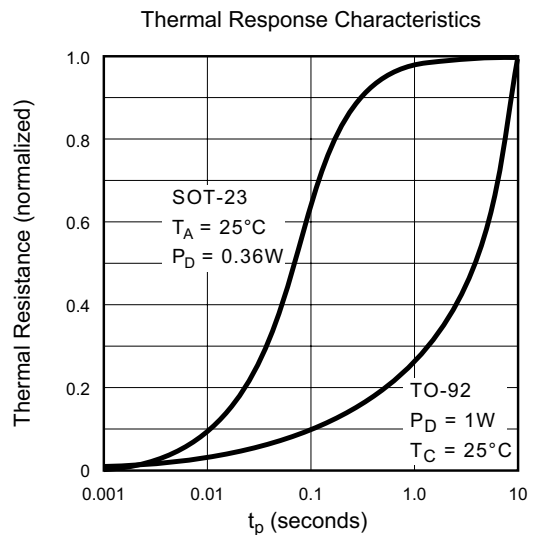
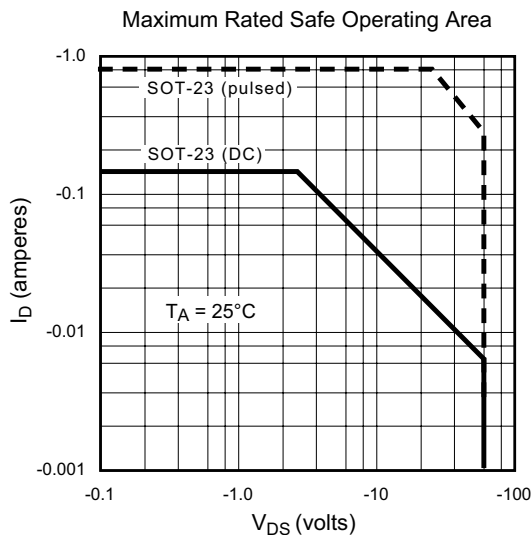
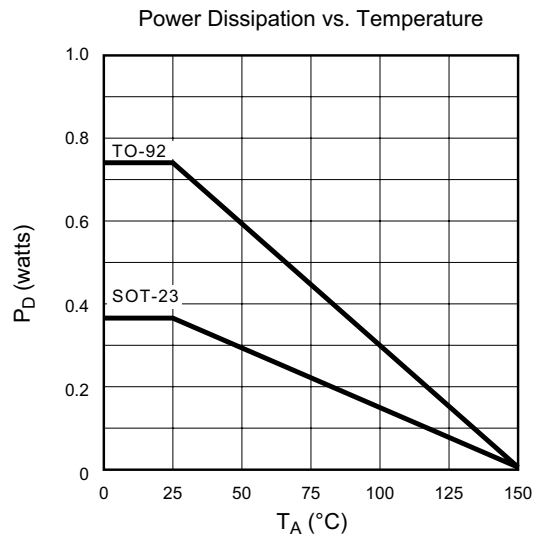
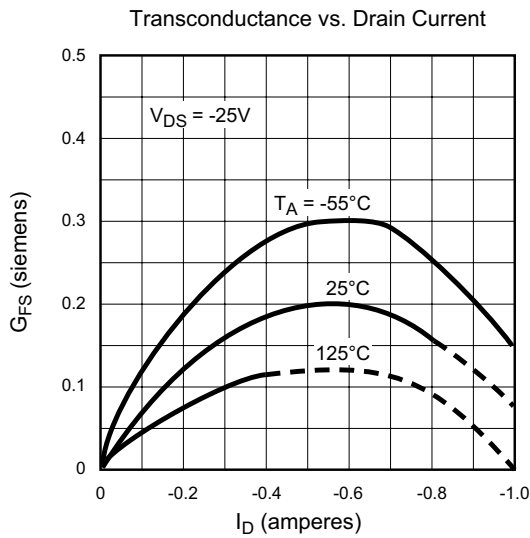
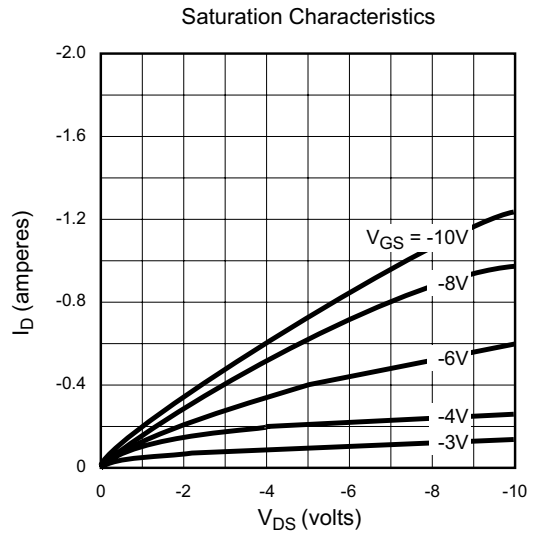
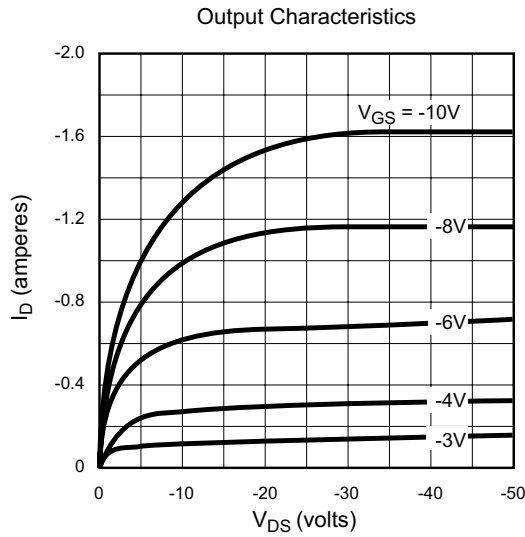
Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

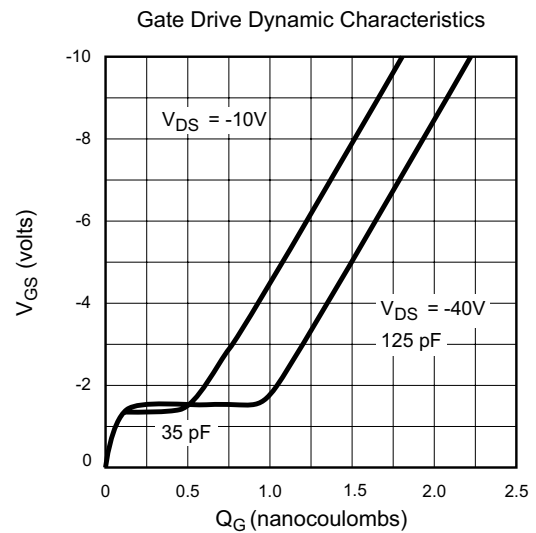
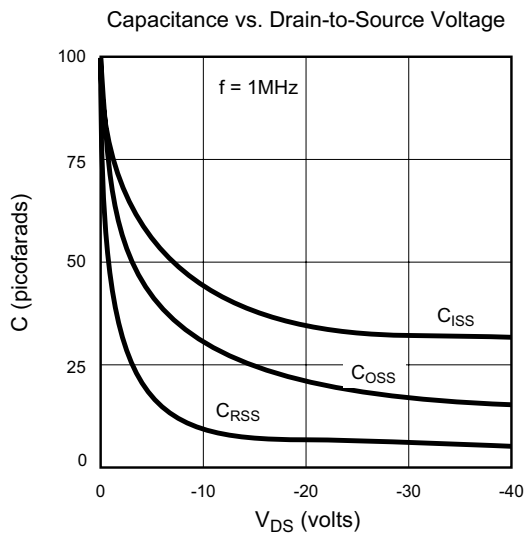
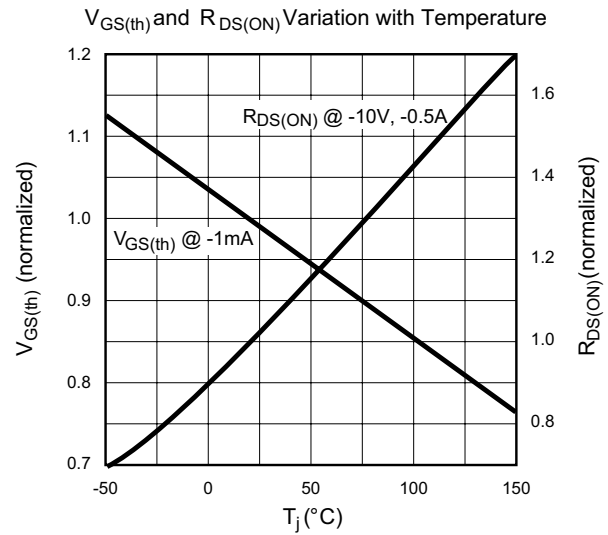
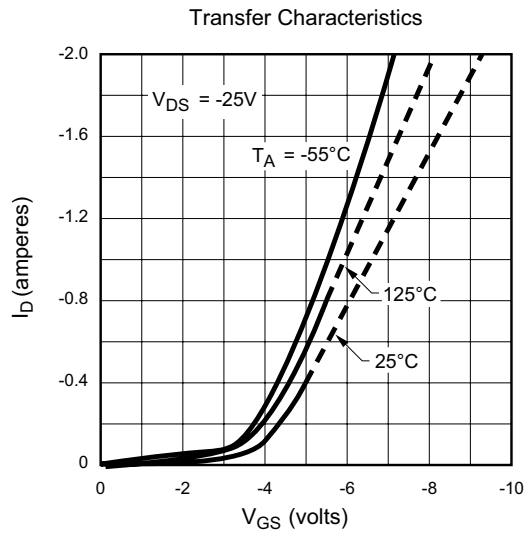
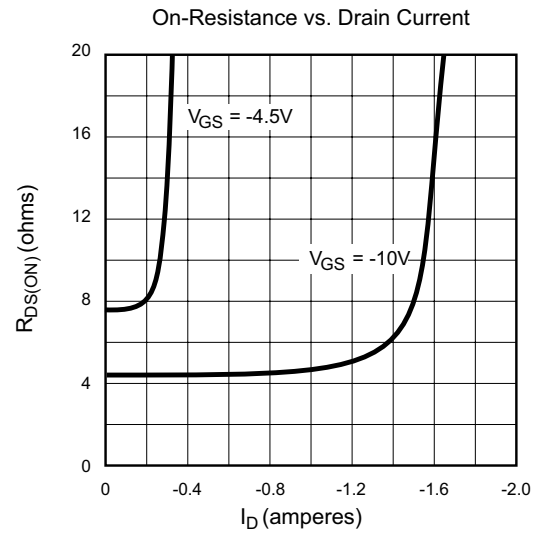
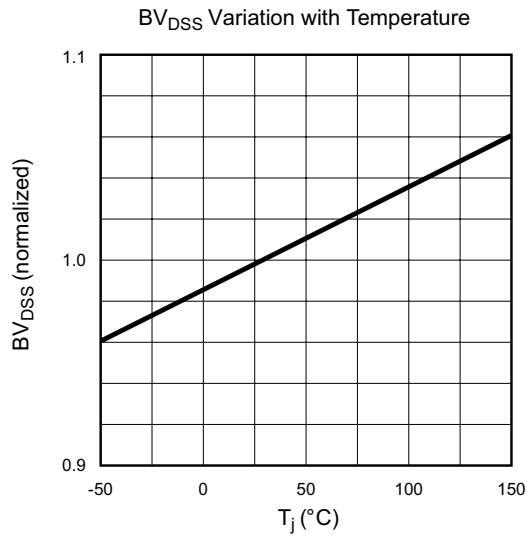
Switching Waveforms and Test Circuit



Typical Performance Curves

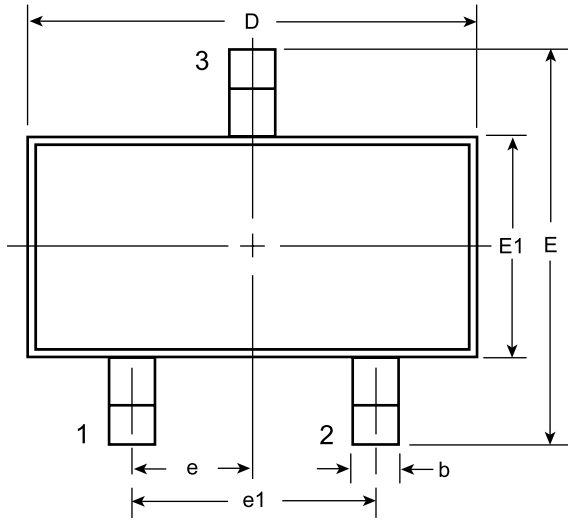


Typical Performance Curves (cont.)

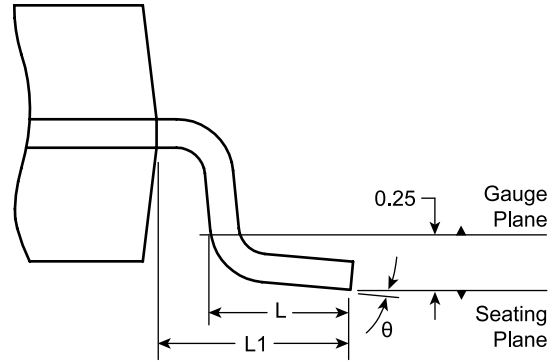


3-Lead TO-236AB (SOT-23) Package Outline (K1)

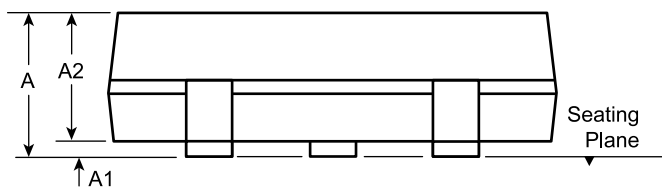
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



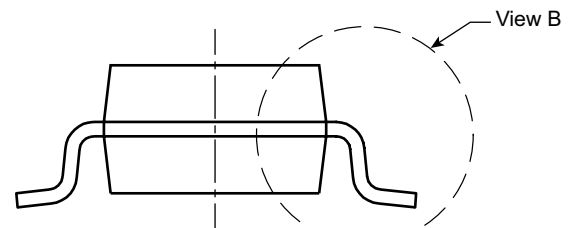
Top View



View B



Side View



View A - A

Symbol	A	A1	A2	b	D	E	E1	e	e1	L	L1	θ	
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

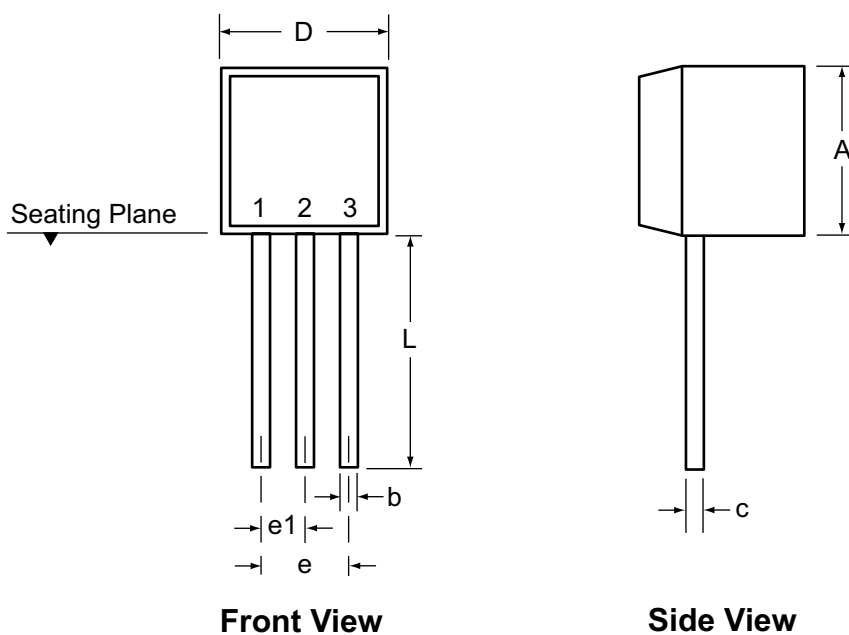
JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

[†] This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO236ABK1, Version B072208.

3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

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