

N-Channel Enhancement Mode Power MOSFET

MTN4N60I3

 BV_{DSS} : 600V
 $R_{DS(ON)}$: 2.8 Ω (typ.)
 I_D : 4A**Description**

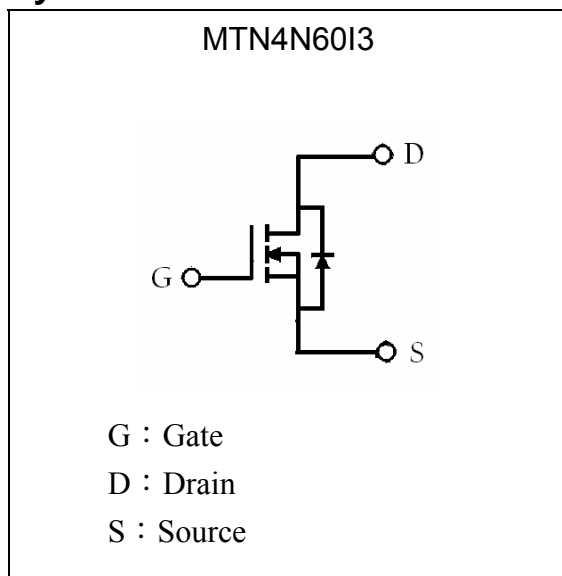
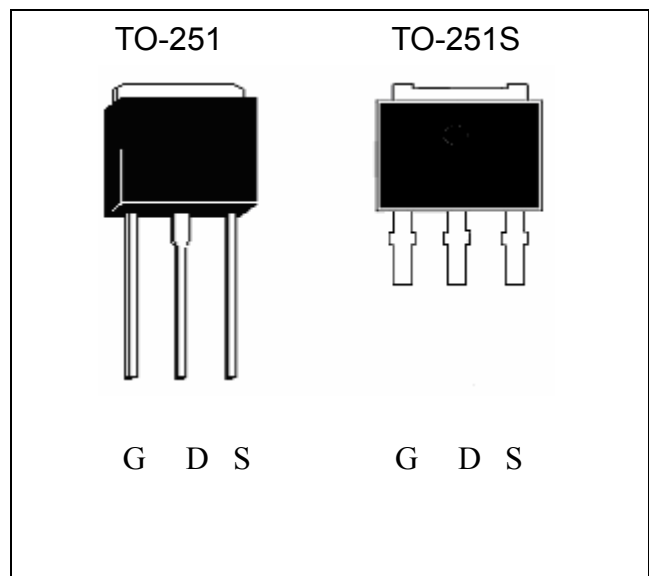
The MTN4N60I3 is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-251 package is universally preferred for all commercial-industrial applications

Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Pb-free lead plating package

Applications

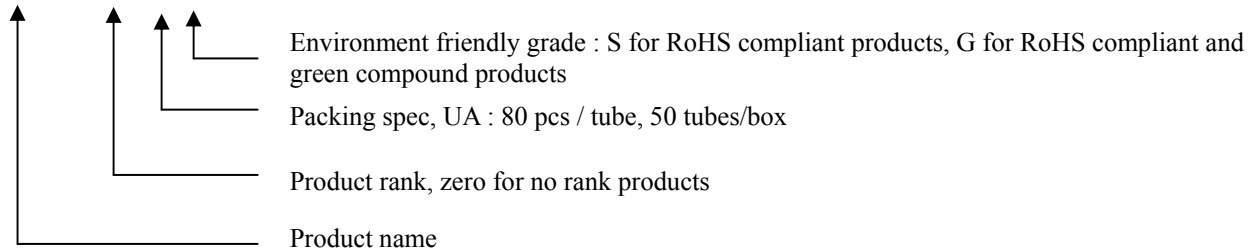
- Open Framed Power Supply
- Adapter
- STB

Symbol**Outline**



Ordering Information

Device	Package	Shipping
MTN4N60I3-0-UA-G	TO-251 (RoHS compliant and halogen-free package)	80 pcs/tube, 50 tubes/box
MTN4N60I3S-0-UA-G	TO-251S (RoHS compliant and halogen-free package)	80 pcs/tube, 50 tubes/box



Absolute Maximum Ratings (T_C=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	±30	V
Continuous Drain Current	I _D	4*	A
Continuous Drain Current @T _C =100°C	I _D	2.4*	A
Pulsed Drain Current @ V _{GS} =10V (Note 1)	I _{DM}	16*	A
Single Pulse Avalanche Energy (Note 2)	E _{AS}	34.9	mJ
Avalanche Current (Note 1)	I _{AR}	4	A
Repetitive Avalanche Energy (Note 1)	E _{AR}	5	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Maximum Temperature for Soldering @ Lead at 0.125 in(0.318mm) from case for 10 seconds	T _L	300	°C
Total Power Dissipation (T _C =25°C)	P _d	50	W
Linear Derating Factor		0.4	W/°C
Operating Junction and Storage Temperature	T _j , T _{stg}	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1.Repetitive rating; pulse width limited by maximum junction temperature.

2. I_{AS}=4A, V_{DD}=50V, L=4mH, V_G=10V, starting T_J=+25°C.

3. I_{SD}≤4A, di/dt≤100A/μs, V_{DD}≤BV_{DSS}, starting T_J=+25°C.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	110	°C/W



Characteristics (Tc=25°C, unless otherwise specified)

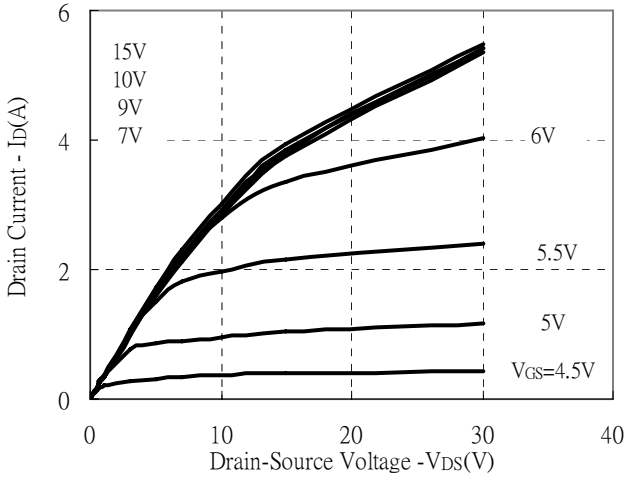
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	600	-	-	V	V _{GS} =0, I _D =250μA, T _j =25°C
ΔBV _{DSS} /ΔT _j	-	0.65	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2.0	-	4.0	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	2	-	S	V _{DS} =15V, I _D =2A
I _{GSS}	-	-	±100	nA	V _{GS} =±30
I _{DSS}	-	-	1	μA	V _{DS} =600V, V _{GS} =0
	-	-	10	μA	V _{DS} =480V, V _{GS} =0, T _j =125°C
*R _{DS(ON)}	-	2.8	3.2	Ω	V _{GS} =10V, I _D =2A
Dynamic					
*Q _g	-	12.8	-	nC	I _D =4A, V _{DD} =480V, V _{GS} =10V
*Q _{gs}	-	2.4	-		
*Q _{gd}	-	7.1	-		
*t _{d(ON)}	-	15	-	ns	V _{DD} =300V, I _D =4A, V _{GS} =10V, R _G =25 Ω, R _D =75 Ω
*t _r	-	21	-		
*t _{d(OFF)}	-	30	-		
*t _f	-	22	-		
C _{iss}	-	560	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	51	-		
C _{rss}	-	7.2	-		
Source-Drain Diode					
*I _S	-	-	4	A	
*I _{SM}	-	-	16		
*V _{SD}	-	-	1.5	V	I _S =4A, V _{GS} =0V
*t _{rr}	-	277	-	ns	V _{GS} =0, I _F =4A, dI/dt=100A/μs
*Q _{rr}	-	2.1	-	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

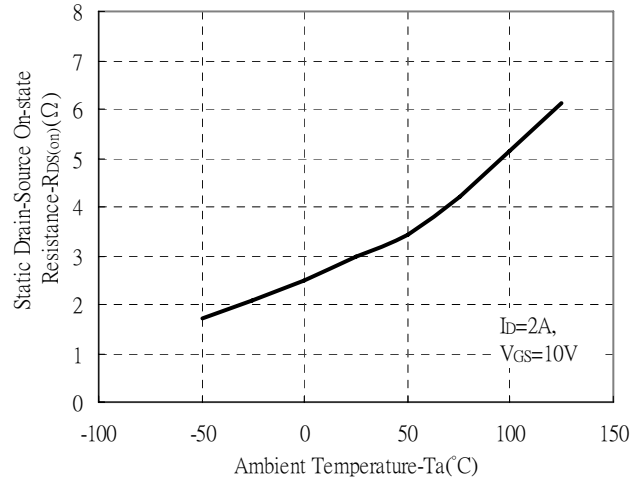


Typical Characteristics

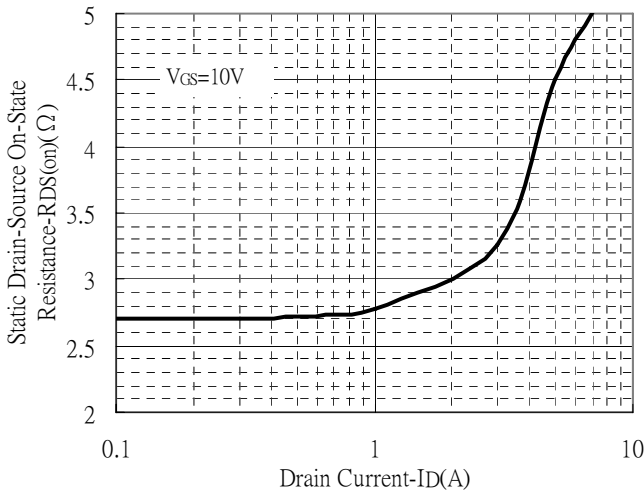
Typical Output Characteristics



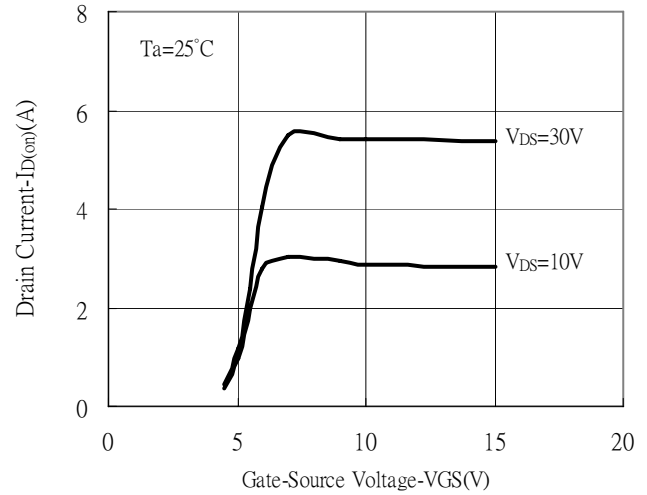
Static Drain-Source On-resistance vs Ambient Temperature



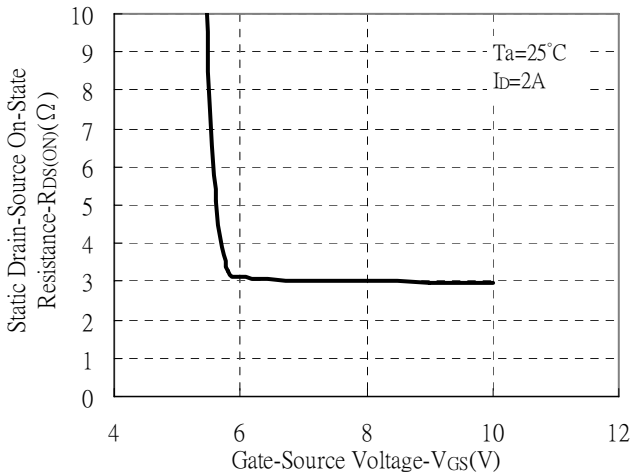
Static Drain-Source On-State resistance vs Drain Current



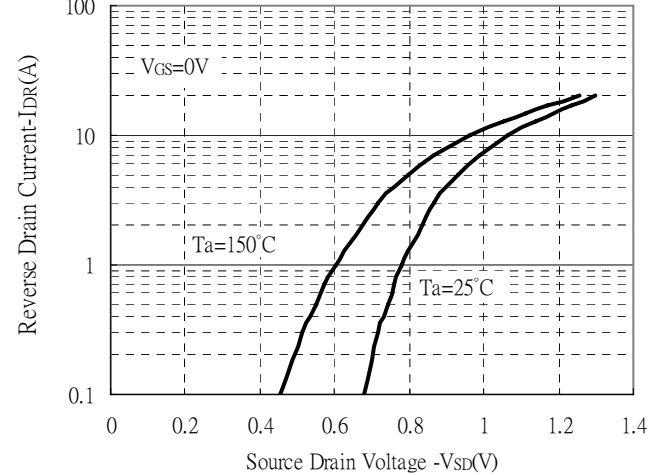
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



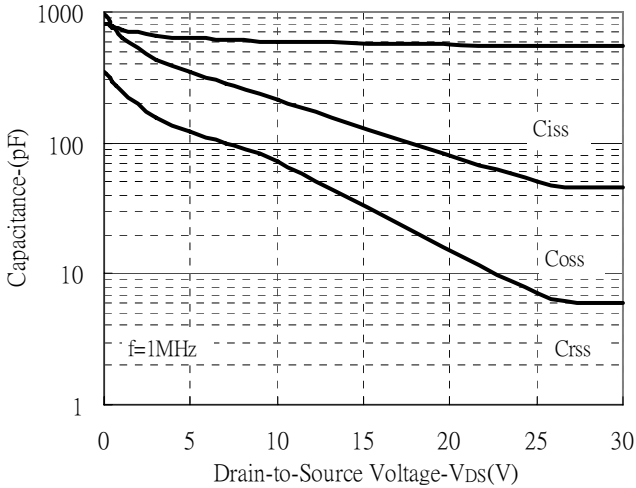
Body Diode Forward Voltage Variation vs Source Current and Temperature



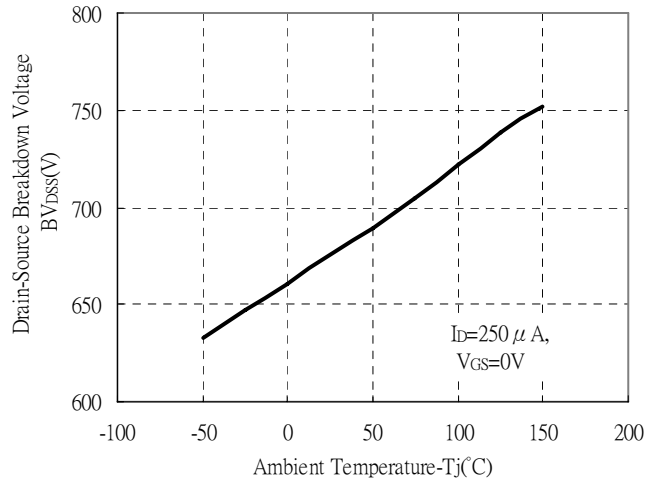


Typical Characteristics(Cont.)

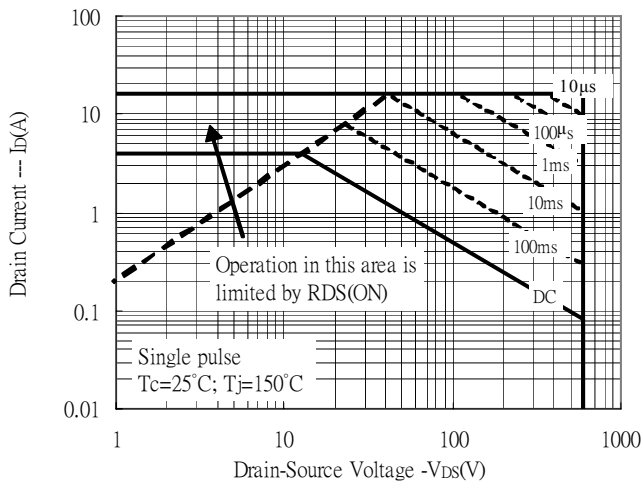
Capacitance vs Reverse Voltage



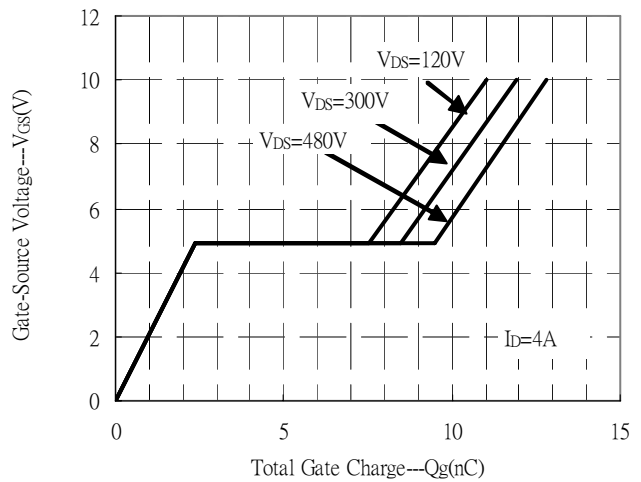
Brekdown Voltage vs Ambient Temperature



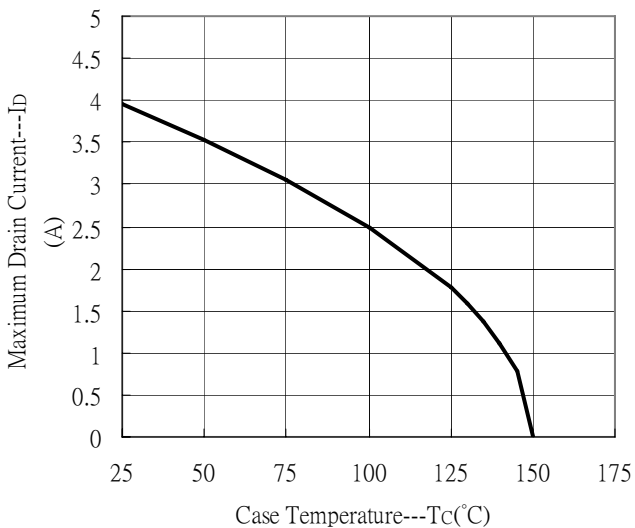
Maximum Safe Operating Area



Gate Charge Characteristics



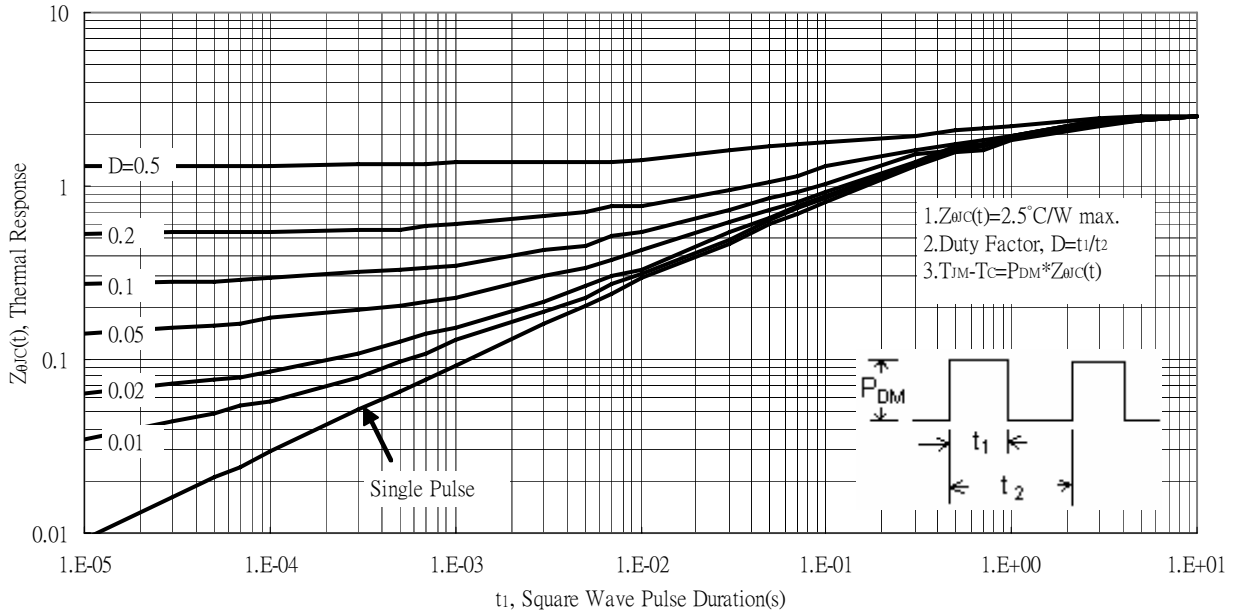
Maximum Drain Current vs Case Temperature





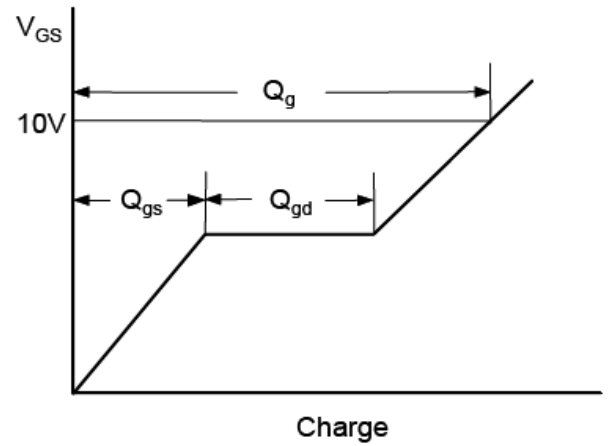
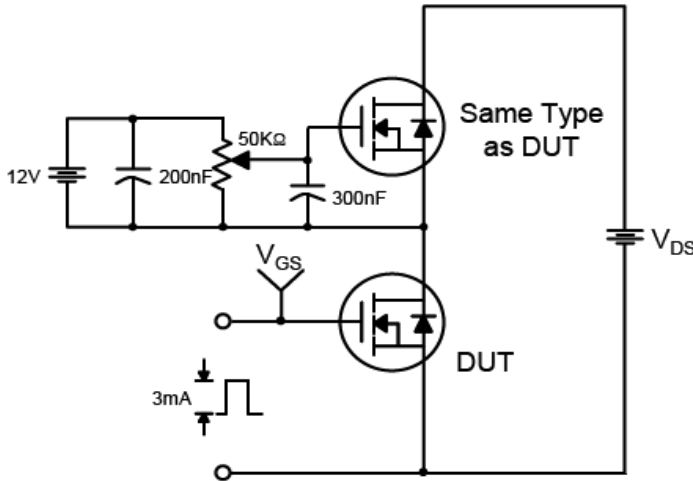
Typical Characteristics(Cont.)

Transient Thermal Response Curves

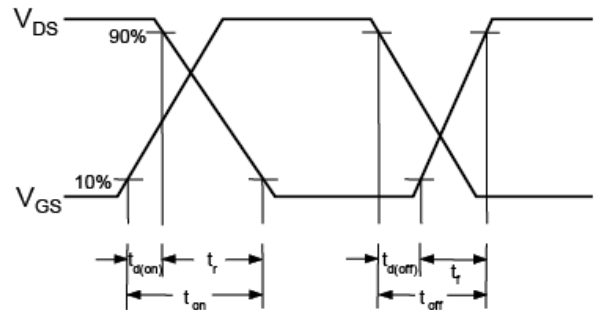
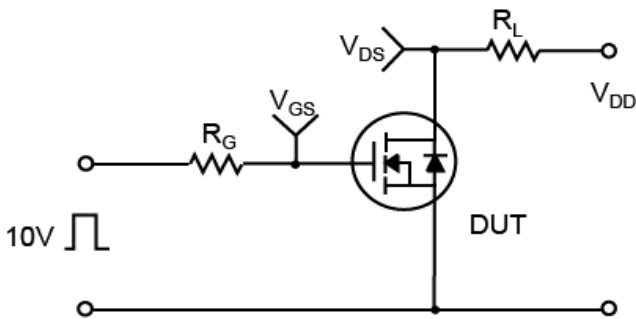


Test Circuits and Waveforms

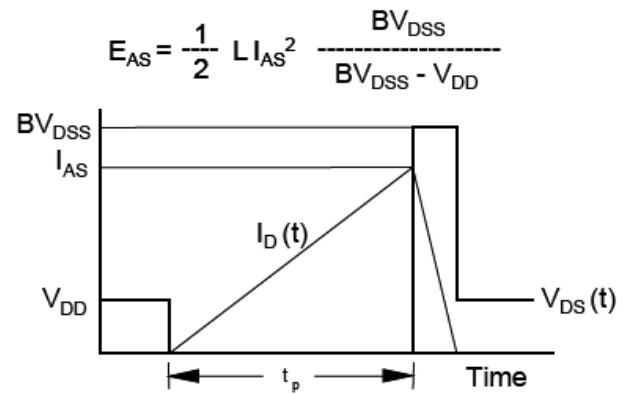
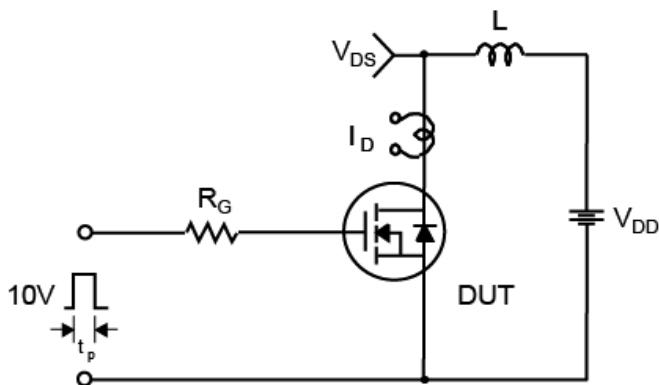
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

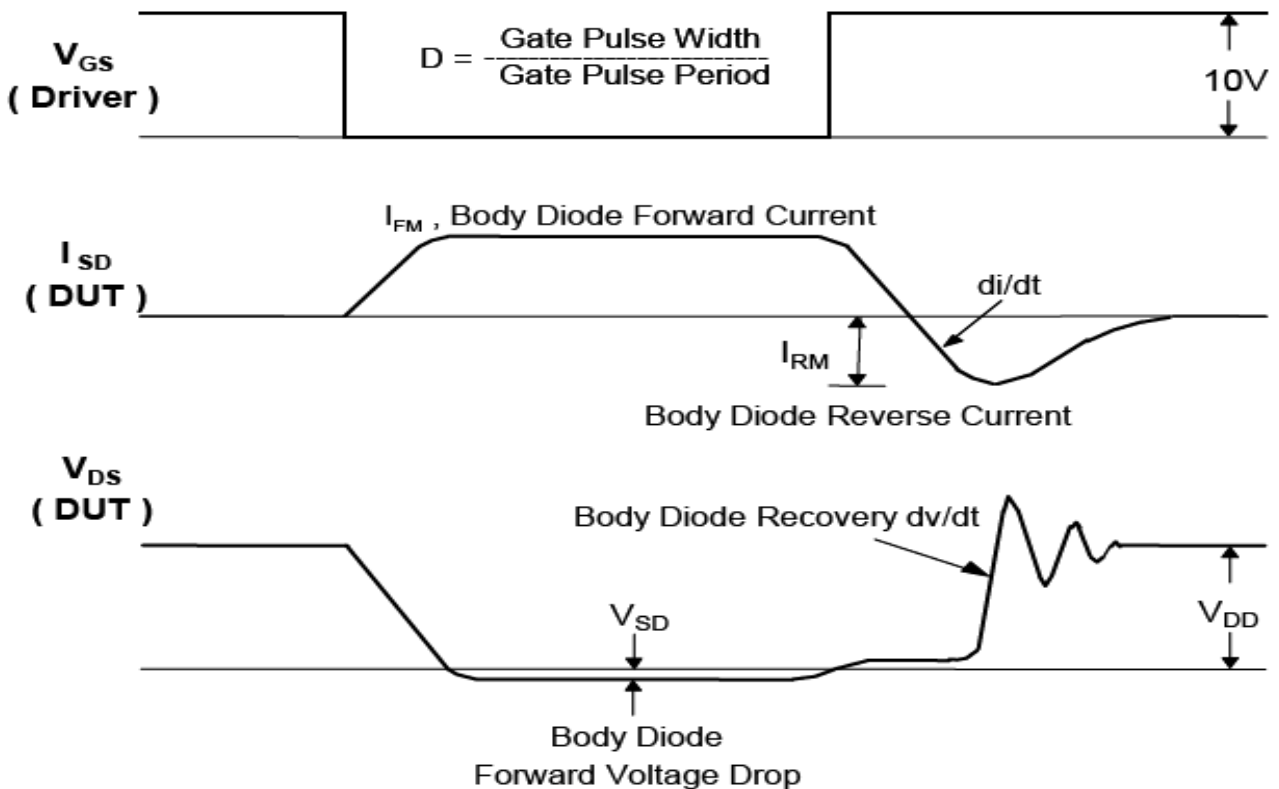
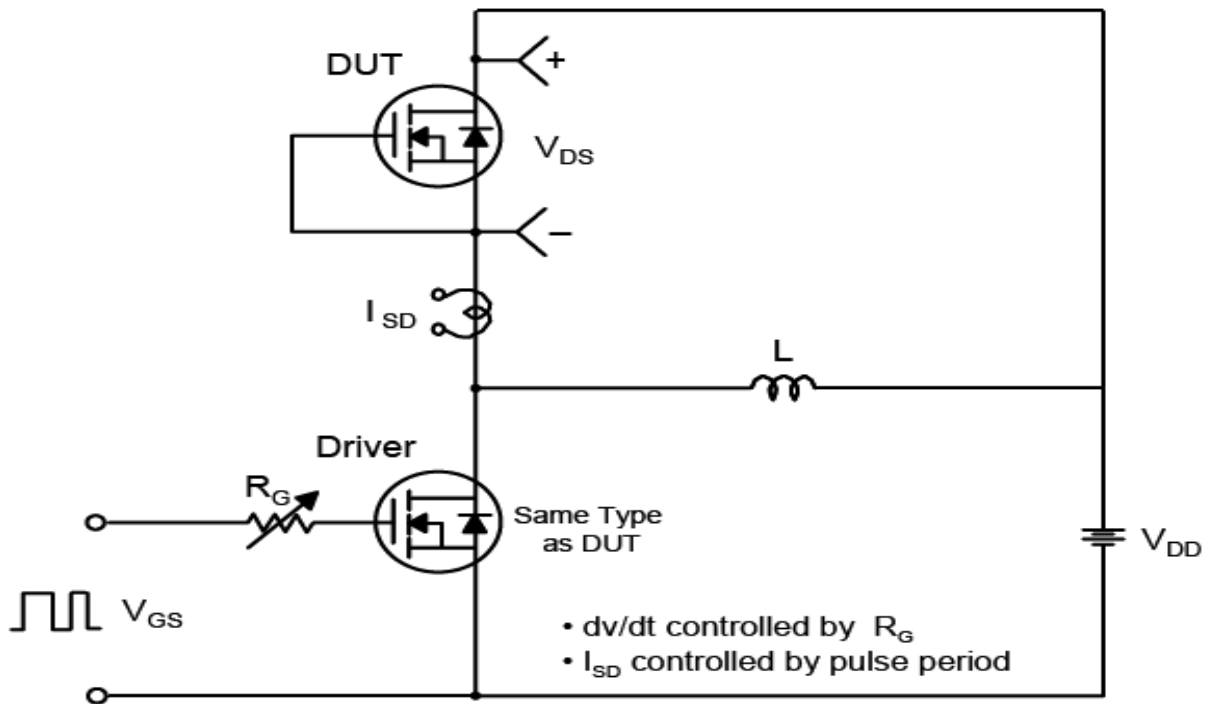


Unclamped Inductive Switching Test Circuit & Waveforms



Test Circuits and Waveforms(Cont.)

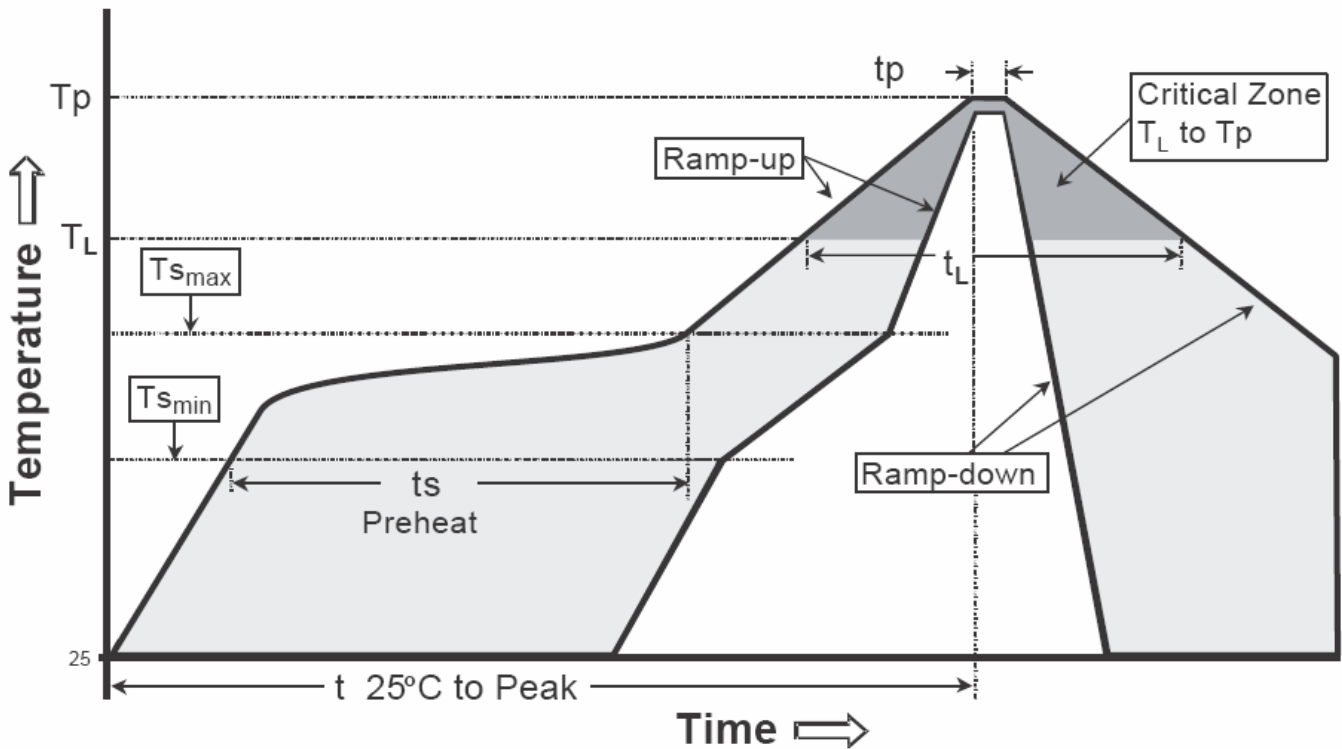
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

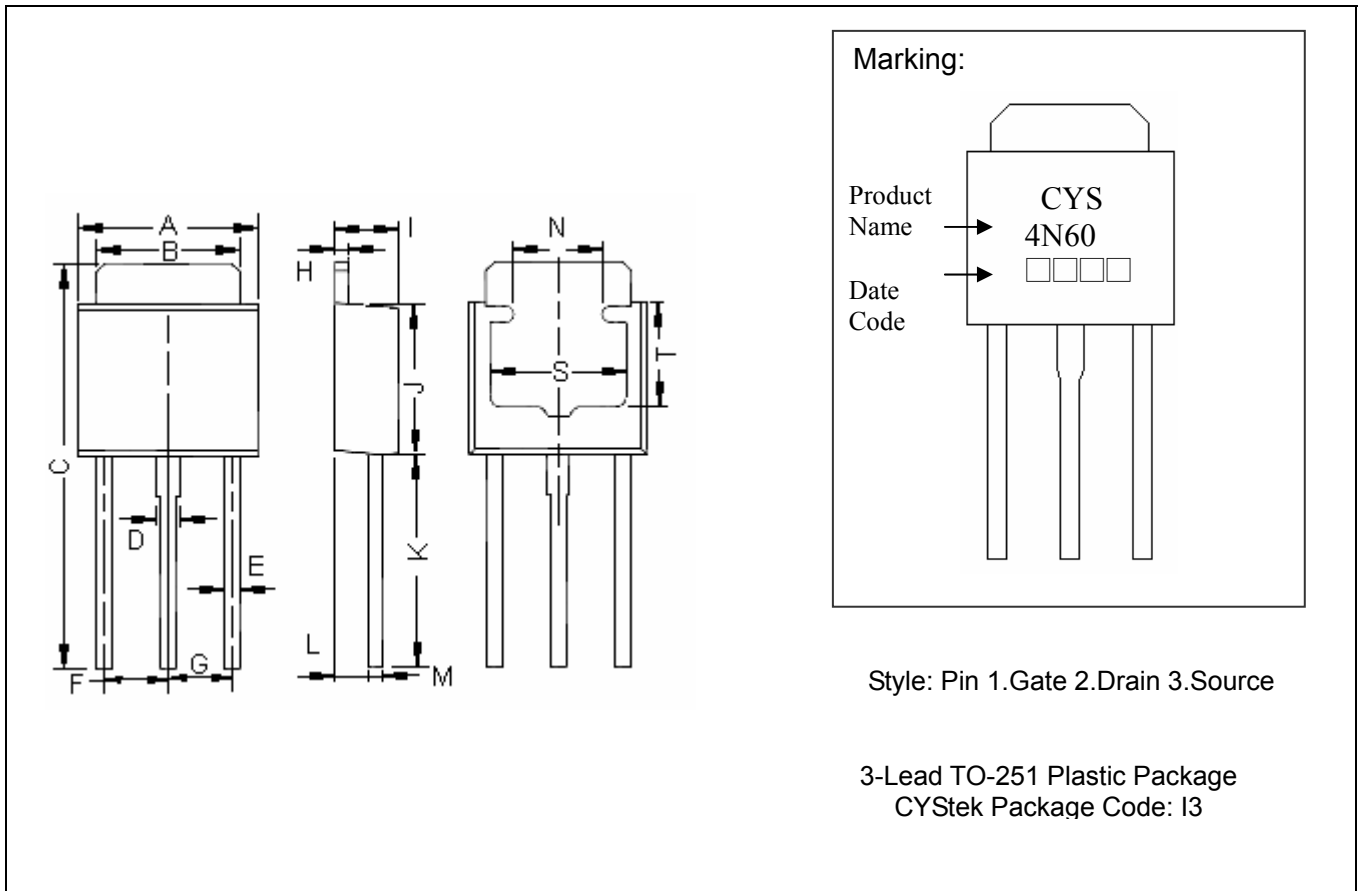
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-251 Dimension



Marking:

Product Name → **CYS 4N60**

Date Code → □ □ □ □

Style: Pin 1.Gate 2.Drain 3.Source

3-Lead TO-251 Plastic Package
 CYStek Package Code: I3

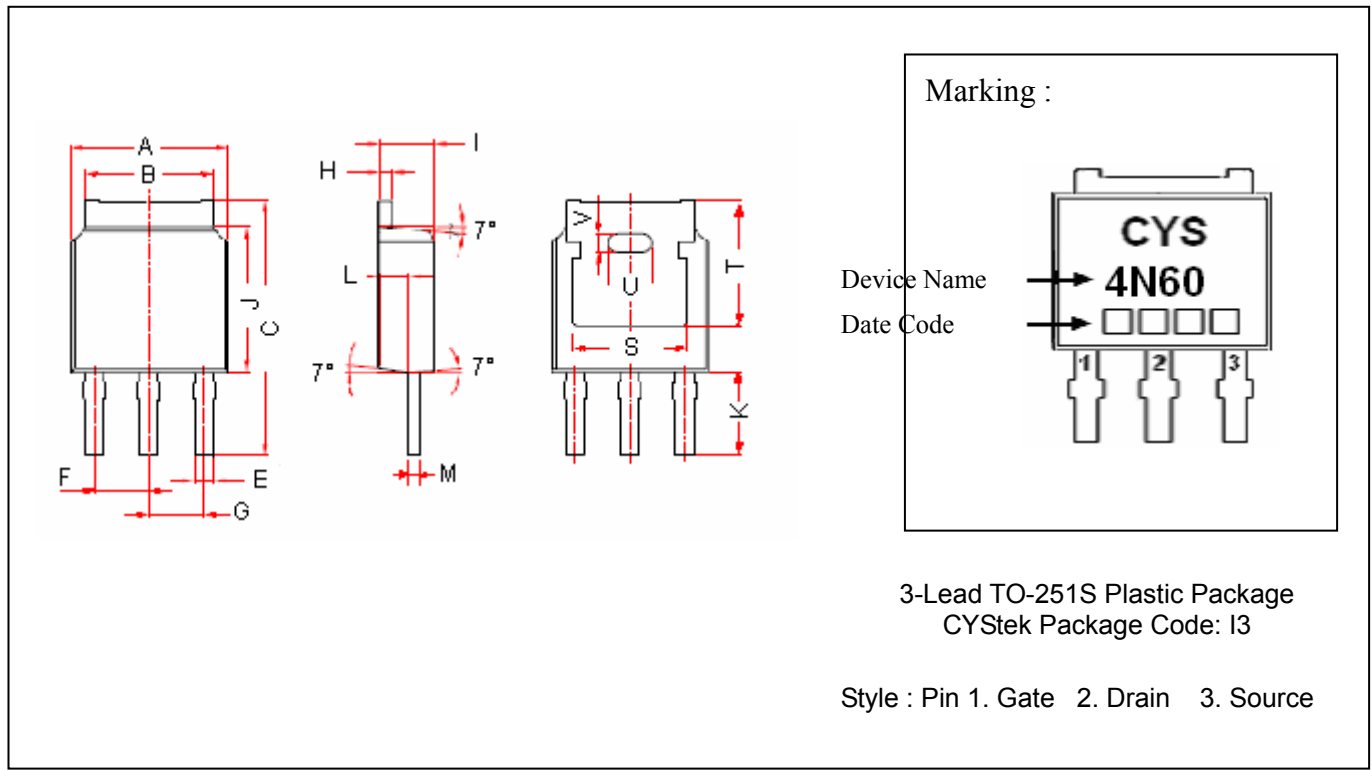
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.2500	0.2618	6.35	6.65	I	0.0866	0.0945	2.20	2.40
B	0.2047	0.2126	5.20	5.40	J	0.2126	0.2244	5.40	5.70
C	0.5709	0.5866	14.50	14.90	K	0.2992	0.3071	7.60	7.80
D	0.0276	0.0354	0.70	0.90	L	0.0453	0.0492	1.15	1.25
E	0.0199	0.0276	0.50	0.70	M	0.0169	0.0228	0.43	0.58
F	0.0886	0.0925	2.25	2.35	N	0.1181	REF	3.00	REF
G	0.0886	0.0925	2.25	2.35	S	0.1969	REF	5.00	REF
H	0.0169	0.0228	0.43	0.58	T	0.1496	REF	3.80	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

TO-251S Dimension



Marking :

Device Name → **CYS 4N60**
 Date Code → □□□□

3-Lead TO-251S Plastic Package
 CYStek Package Code: I3

Style : Pin 1. Gate 2. Drain 3. Source

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.2559	0.2638	6.50	6.70	J	0.2362	0.2441	6.00	6.20
B	0.2020	0.2126	5.13	5.46	K	0.1299	0.1457	3.30	3.70
C	0.4094	0.4331	10.40	11.00	L	0.0358	0.0437	0.91	1.11
E	0.0280	0.0319	0.71	0.81	M	0.0181	0.0220	0.46	0.56
F	0.0858	0.0941	2.18	2.39	S	0.1902	REF	4.83	REF
G	0.0858	0.0941	2.18	2.39	T	0.2106	REF	5.35	REF
H	0.0181	0.0220	0.46	0.56	U	0.0701	REF	1.78	REF
I	0.0902	0.0937	2.29	2.38	V	0.0299	REF	0.76	REF

Notes: 1.Controlling dimension: inch.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.