P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE†
-350V	75Ω	-200mA	VP0535N2	VP0535N3	VP0535ND
-400V	75Ω	-200mA	VP0540N2	VP0540N3	VP0540ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- *Free from secondary breakdown*
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

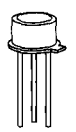
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-39

TO-92

Note: See package outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-39	-0.2A	-0.5A	3.5W	35	125	-0.2A	-0.5A
TO-92	-0.1A	-0.5A	1.0W	125	170	-0.1A	-0.5A

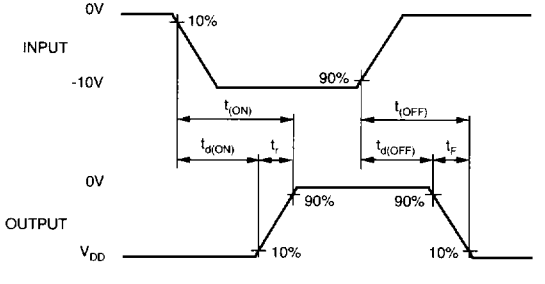
* I_D (continuous) is limited by max rated T_j.

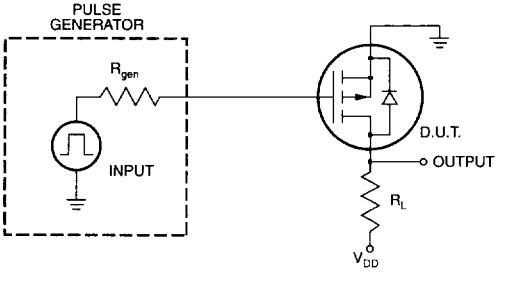
Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0540	-400			V	V_{GS}= 0V, I_D =-1mA
		VP0535	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-2.5		-4.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			3.5	6.0	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				-10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					-500		V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			-80		mA	V_{GS} = -5V, V_{DS} = -25V
			-200	-350			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			60		Ω	V_{GS} = -5V, I_D = -10mA
				45	75		V_{GS} = -10V, I_D = -50mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8	1.5	%/°C	V_{GS} = -10V, I_D = -50mA
G_{FS}	Forward Transconductance		50	70		m℧	V_{DS} = -25V, I_D = -50mA
C_{ISS}	Input Capacitance			40	60	pF	V_{GS} = 0V, V_{DS} = -25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			11	20		
C_{RSS}	Reverse Transfer Capacitance			3	5		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V I_D = -200mA R_{GEN} = 25Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop			-0.8	-1.5	V	V_{GS} = 0V, I_{SD} = -0.1A
t_{rr}	Reverse Recovery Time			200		ns	V_{GS} = 0V, I_{SD} = -0.1A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

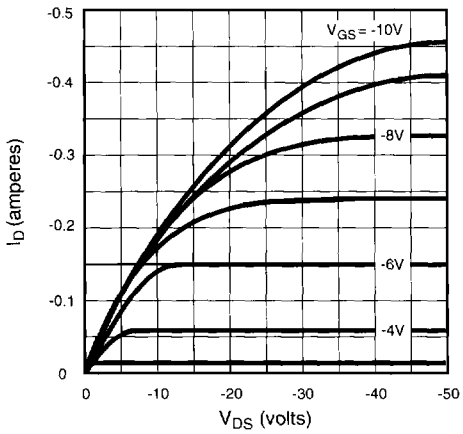
Switching Waveforms and Test Circuit



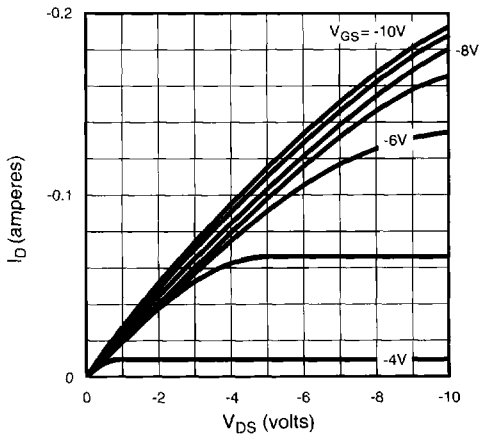


Typical Performance Curves

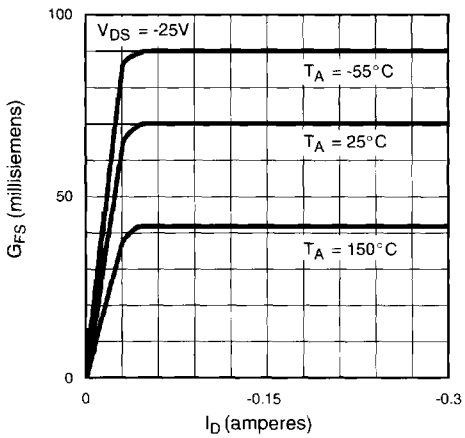
Output Characteristics



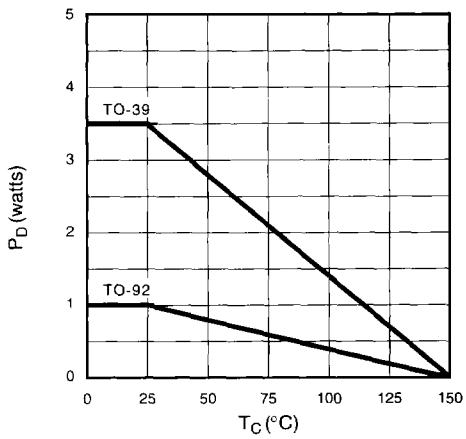
Saturation Characteristics



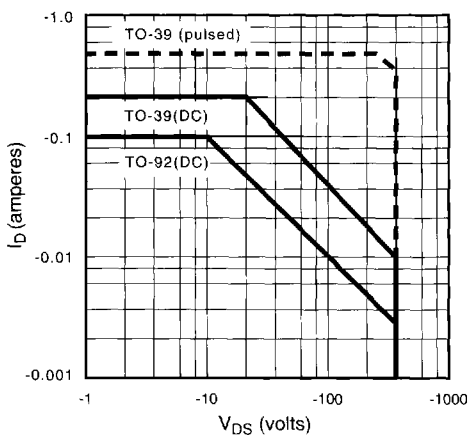
Transconductance vs. Drain Current



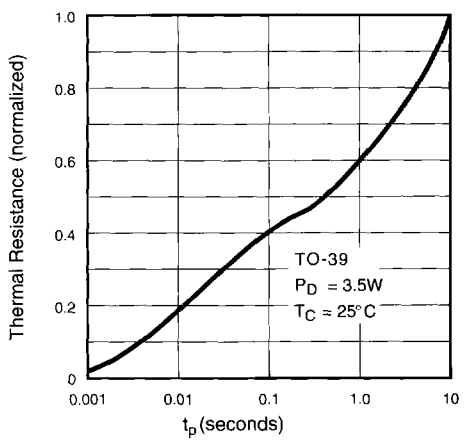
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



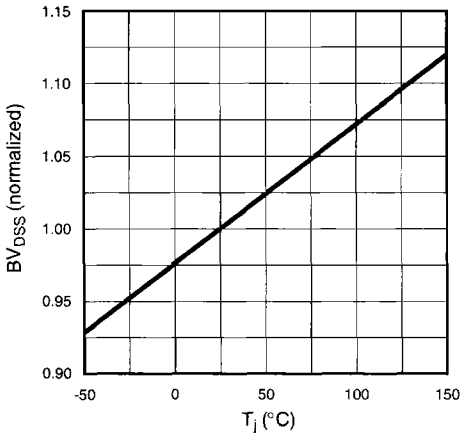
Thermal Response Characteristics



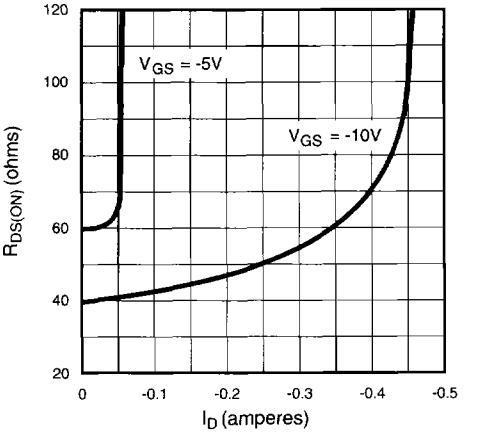
9

Typical Performance Curves

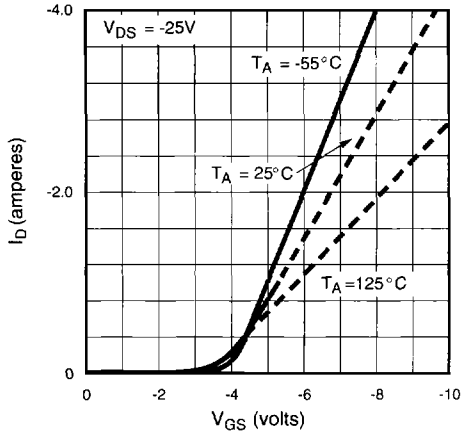
BV_{DSS} Variation with Temperature



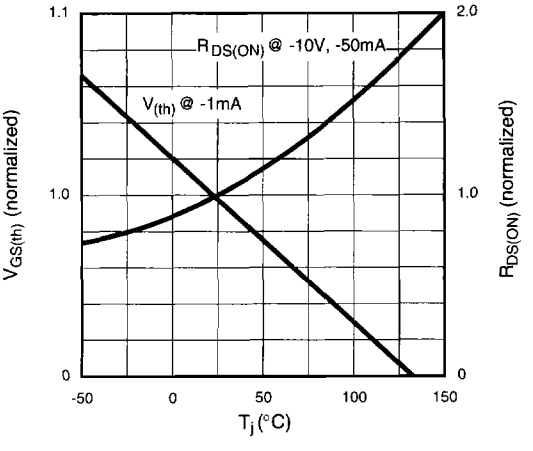
On-Resistance vs. Drain Current



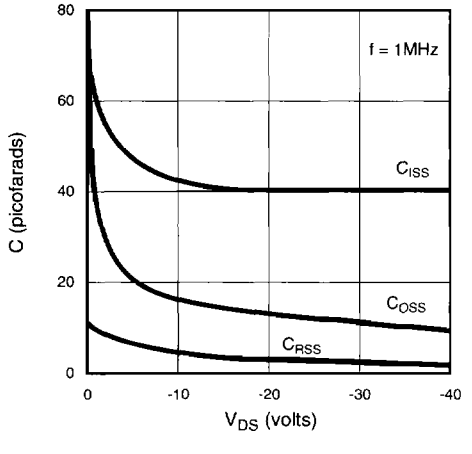
Transfer Characteristics



$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics