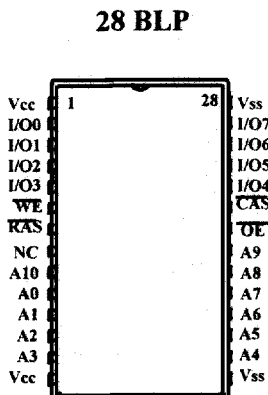




Description

The GM71V(S)17803CI/CLI is the new generation dynamic RAM organized 2,097,152 x 8 bit. GM71V(S)17803CI/CLI has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)17803CI/CLI offers Extended Data out(EDO) Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)17803CI/CLI to be packaged in 28pin BLP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 3.3V±0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Pin Configuration



Features

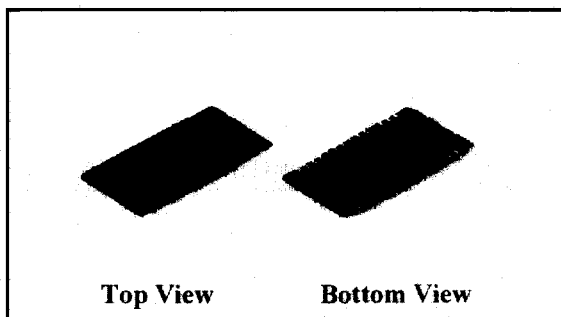
- 2,097,152 Words x 8 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (3.3V±0.3V)
- Fast Access Time & Cycle Time

(Unit: ns)

	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
GM71V(S)17803CI/CLI-5	50	13	84	20
GM71V(S)17803CI/CLI-6	60	15	104	25
GM71V(S)17803CI/CLI-7	70	18	124	30

- Low Power
Active : 396/360/324mW (MAX)
Standby : 7.2mW (CMOS level : MAX)
0.36mW (L-version : MAX)
- RAS Only Refresh, $\overline{\text{CAS}}$ before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 2048 Refresh Cycles/32ms
- 2048 Refresh Cycles/128ms (L-version)
- Self Refresh Operation (L-version)
- Battery Back Up Operation (L-version)

28 pin BLP



Pin Description

Pin	Function	Pin	Function
A0-A10	Address Inputs	\overline{WE}	Read/Write Enable
A0-A10	Refresh Address Inputs	\overline{OE}	Output Enable
I/O0-I/O7	Data Input/ Data Output	V _{cc}	Power (+3.3V)
\overline{RAS}	Row Address Strobe	V _{ss}	Ground
\overline{CAS}	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)17803CI/CLI-5	50ns	28 Pin BLP
GM71V(S)17803CI/CLI-6	60ns	28 Pin BLP
GM71V(S)17803CI/CLI-7	70ns	28 Pin BLP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature	-55 ~ 125	°C
V _{IN/OUT}	Voltage on any Pin Relative to V _{ss}	-0.5 ~ V _{cc} +0.5 (≤ 4.6V(MAX))	V
V _{cc}	Supply Voltage Relative to V _{ss}	-0.5 ~ 4.6	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{cc}	Supply Voltage	3.0	3.3	3.6	V
V _{IH}	Input High Voltage	2.0	-	V _{cc} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltage referred to V_{ss}.

DC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $V_{SS} = 0V$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note	
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -2mA$)	2.0	V_{CC}	V		
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 2mA$)	0	0.4	V		
I_{CC1}	Operating Current Average Power Supply Operating Current (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = t_{RC\ min}$)	50ns	-	110	mA	1, 2
		60ns	-	100		
		70ns	-	90		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (\overline{RAS} , $\overline{CAS} = V_{IH}$, $D_{OUT} = High-Z$)	-	2	mA		
I_{CC3}	RAS Only Refresh Current Average Power Supply Current RAS Only Refresh Mode ($t_{RC} = t_{RC\ min}$)	50ns	-	110	mA	2
		60ns	-	100		
		70ns	-	90		
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode ($t_{HPC} = t_{HPC\ min}$)	50ns	-	100	mA	1, 3
		60ns	-	90		
		70ns	-	85		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (\overline{RAS} , $\overline{CAS} > V_{CC} - 0.2V$, $D_{OUT} = High-Z$)	-	1	mA		
		-	150	μA	5	
I_{CC6}	\overline{CAS} -before- \overline{RAS} Refresh Current ($t_{RC} = t_{RC\ min}$)	50ns	-	110	mA	
		60ns	-	100		
		70ns	-	90		
I_{CC7}	Battery Back Up Operating Current(Standby with CBR Ref.) (CBR refresh, $t_{RC} = 62.5\mu s$, $t_{RAS} \leq 0.3\mu s$, $D_{OUT} = High-Z$, CMOS Interface)	-	400	μA	4, 5	
I_{CC8}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = Enable$	-	5	mA	1	
I_{CC9}	Self-Refresh Mode Current (\overline{RAS} , $\overline{CAS} \leq 0.2V$, $D_{OUT} = High-Z$, CMOS interface)	-	250	μA	5	
I_{LO}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 4.6V$)	-10	10	μA		
I_{LO}	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 4.6V$)	-10	10	μA		

Note: 1. I_{CC} depends on output load condition when the device is selected.

$I_{CC(max)}$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

4. $\overline{CAS} = L (\leq 0.2V)$ while $\overline{RAS} = L (\leq 0.2V)$.

5. L -version.

Capacitance ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
C _{I1}	Input Capacitance (Address)	-	5	pF	1
C _{I2}	Input Capacitance (Clocks)	-	7	pF	1
C _O	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable DOUT.

AC Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim +70^\circ C$, Note 1, 2, 18)

Test Conditions

Input rise and fall times : 2 ns

Input levels : V_{IL} = 0V, V_{IH} = 3V

Input timing reference levels : 0.8V, 2.0V

Output timing reference levels : 0.8V, 2.0V

Output load : 1TTL gate + C_L (100 pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
t _{RP}	\overline{RAS} Precharge Time	30	-	40	-	50	-	ns	
t _{CP}	\overline{CAS} Precharge Time	8	-	10	-	13	-	ns	
t _{RAS}	\overline{RAS} Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t _{CAS}	\overline{CAS} Pulse Width	8	10,000	10	10,000	13	10,000	ns	
t _{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t _{RAH}	Row Address Hold Time	8	-	10	-	10	-	ns	
t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t _{CAH}	Column Address Hold Time	8	-	10	-	13	-	ns	
t _{RCD}	\overline{RAS} to \overline{CAS} Delay Time	12	37	14	45	14	52	ns	3
t _{RAD}	\overline{RAS} to Column Address Delay Time	10	25	12	30	12	35	ns	4
t _{RSH}	\overline{RAS} Hold Time	10	-	13	-	13	-	ns	
t _{CSH}	\overline{CAS} Hold Time	35	-	40	-	45	-	ns	
t _{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	5	-	5	-	5	-	ns	
t _{ODD}	\overline{OE} to D _{IN} Delay Time	13	-	15	-	18	-	ns	5
t _{DZO}	\overline{OE} Delay Time from D _{IN}	0	-	0	-	0	-	ns	6
t _{DZC}	\overline{CAS} Delay Time from D _{IN}	0	-	0	-	0	-	ns	6
t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from \overline{RAS}	-	50	-	60	-	70	ns	8,9
t _{CAC}	Access Time from \overline{CAS}	-	13	-	15	-	18	ns	9,10,17
t _{AA}	Access Time from Address	-	25	-	30	-	35	ns	9,11,17
t _{OAC}	Access Time from \overline{OE}	-	13	-	15	-	18	ns	9
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time to \overline{CAS}	0	-	0	-	0	-	ns	12
t _{RRH}	Read Command Hold Time to \overline{RAS}	5	-	5	-	5	-	ns	12
t _{RAL}	Column Address to \overline{RAS} Lead Time	25	-	30	-	35	-	ns	
t _{CAL}	Column Address to \overline{CAS} Lead Time	15	-	18	-	23	-	ns	
t _{CLZ}	\overline{CAS} to Output in Low-Z	0	-	0	-	0	-	ns	
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t _{OHO}	Output Data Hold Time from \overline{OE}	3	-	3	-	3	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	13
t _{OEZ}	Output Buffer Turn-off Time to \overline{OE}	-	13	-	15	-	15	ns	13
t _{CDD}	\overline{CAS} to D _{IN} Delay Time	13	-	15	-	18	-	ns	5
t _{RCHR}	Read Command Hold Time from \overline{RAS}	50	-	60	-	70	-	ns	
t _{OHR}	Output Data hold Time from \overline{RAS}	3	-	3	-	3	-	ns	
t _{OFR}	Output Buffer turn off to \overline{RAS}	-	13	-	15	-	15	ns	
t _{WEZ}	Output Buffer turn off to \overline{WE}	-	13	-	15	-	15	ns	
t _{WDD}	\overline{WE} to D _{IN} Delay Time	13	-	15	-	18	-	ns	
t _{RDD}	\overline{RAS} to D _{IN} Delay Time	13	-	15	-	18	-	ns	

Write Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
twcs	Write Command Setup Time	0	-	0	-	0	-	ns	14
twch	Write Command Hold Time	8	-	10	-	13	-	ns	
twp	Write Command Pulse Width	8	-	10	-	10	-	ns	
trwl	Write Command to $\overline{\text{RAS}}$ Lead Time	8	-	10	-	13	-	ns	
tcwl	Write Command to $\overline{\text{CAS}}$ Lead Time	8	-	10	-	13	-	ns	
tds	Data-in Setup Time	0	-	0	-	0	-	ns	15
tdh	Data-in Hold Time	8	-	10	-	13	-	ns	15

Read- Modify-Write Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
trwc	Read-Modify-Write Cycle Time	111	-	136	-	161	-	ns	
trwd	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	67	-	79	-	92	-	ns	14
tcwd	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	34	-	40	-	ns	14
tawd	Column Address to $\overline{\text{WE}}$ Delay Time	42	-	49	-	57	-	ns	14
toeh	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
tcsr	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	ns	
tchr	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	8	-	10	-	10	-	ns	
twrp	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	0	-	0	-	0	-	ns	
twrh	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
trpc	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	ns	

EDO Page Mode Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{HPC}	EDO Page Mode Cycle Time	20	-	25	-	30	-	ns	19
t _{RASP}	EDO Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	ns	9,17
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40	-	ns	
t _{DOH}	Output data Hold Time from $\overline{\text{CAS}}$ low	3	-	3	-	3		ns	9,17
t _{COL}	$\overline{\text{CAS}}$ Hold Time referred $\overline{\text{OE}}$	8	-	10	-	13		ns	
t _{COP}	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ Setup Time	5	-	5	-	5		ns	
t _{RCHP}	Read command Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40		ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	79	-	ns	
t _{CPW}	$\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge	45	-	54	-	62	-	ns	14

Refresh

Symbol	Parameter	GM71V(S)17803 CI/CLI-5		GM71V(S)17803 CI/CLI-6		GM71V(S)17803 CI/CLI-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{REF}	Refresh period	-	32	-	32	-	32	ms	2048 cycles
t _{REF}	Refresh period (L-version)	-	128	-	128	-	128	ms	2048 cycles

Self Refresh Mode (L-version)

Symbol	Parameter	GM71VS17400 CL-5		GM71VS17400 CL-6		GM71VS17400 CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RASS}	$\overline{\text{RAS}}$ Pulse Width(Self-Refresh)	100	-	100	-	100	-	us	
t _{RPS}	$\overline{\text{RAS}}$ Precharge Time(Self-Refresh)	90	-	110	-	130	-	ns	
t _{CHS}	$\overline{\text{CAS}}$ Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	ns	

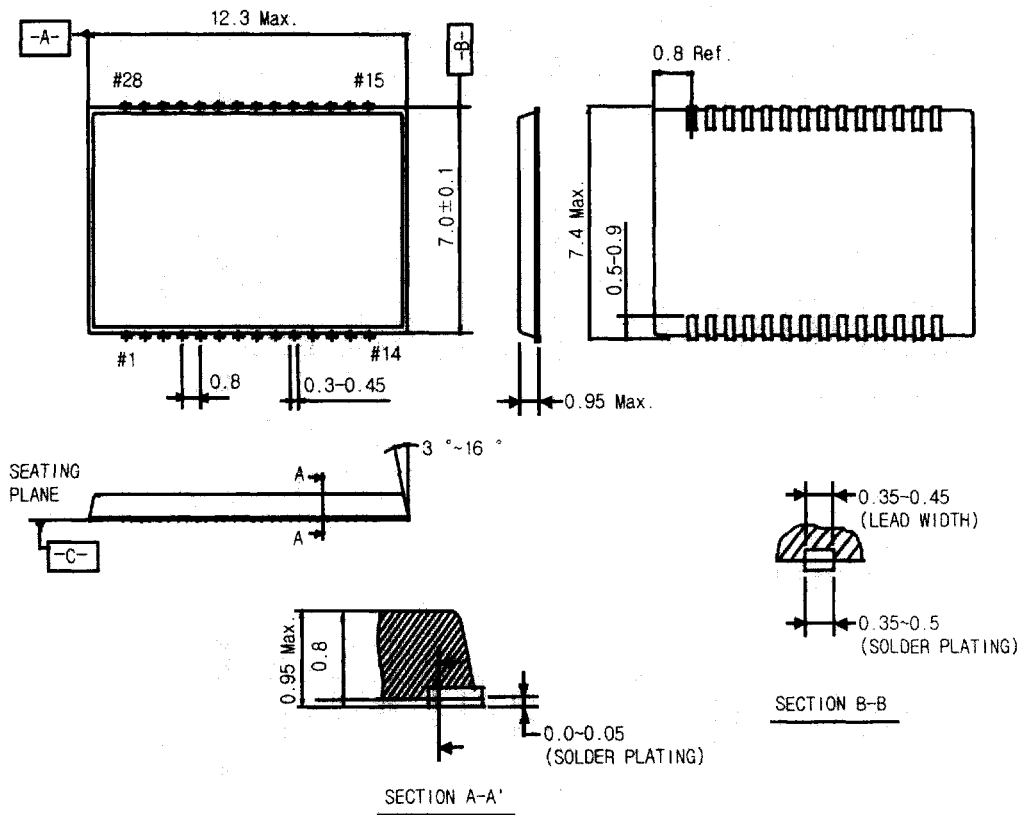
Notes:

1. AC Measurements assume $t_r = 2\text{ns}$.
2. An initial pause of $200\mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
4. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100pF.
10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
11. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, or $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read modify write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read modify write cycle.
16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the I/O pin will remain open circuit (high impedance); if $t_{\text{OEH}} \leq t_{\text{CWL}}$, invalid data will be out at each I/O.
19. EDO Hi-Z control by $\overline{\text{OE}}$ or $\overline{\text{WE}}$. $\overline{\text{OE}}$ rising edge disables data outputs. When $\overline{\text{OE}}$ goes high during $\overline{\text{CAS}}$ high, the data will not come out until next $\overline{\text{CAS}}$ access. When $\overline{\text{WE}}$ goes low during $\overline{\text{CAS}}$ high, the data will not come out until next $\overline{\text{CAS}}$ access.
20. $t_{\text{HPC}}(\text{min})$ can be achieved during a series of EDO mode write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode $\overline{\text{RAS}}$ cycle (EDO mode mix cycle (1),(2)) minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_r$) becomes greater than the specified $t_{\text{HPC}}(\text{min})$ value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).

Package Dimensions

Unit: Inches (mm)

28 BLP



PKG STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD METEIRAL	42 ALLOY
PKG WEIGHT	0.17 gr

