



UTT50P04

Preliminary

Power MOSFET

**-40V, -60A P-CHANNEL
POWER MOSFET**

■ DESCRIPTION

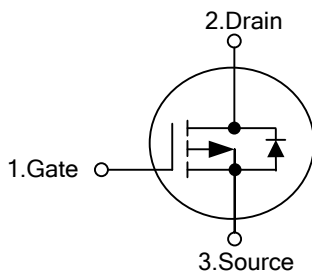
The UTC **UTT50P04** is a P-channel power MOSFET using UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance, and it can also withstand high energy in the avalanche.

This UTC **UTT50P04** is suitable for motor drivers, high-side switch and 12V board net, etc.

■ FEATURES

- * $V_{DS} = -40V$,
- * $I_D = -60A$
- * $R_{DS(ON)} = 0.0105\Omega @ V_{GS} = -10V, I_D = -30A$
- * High Switching Speed

■ SYMBOL

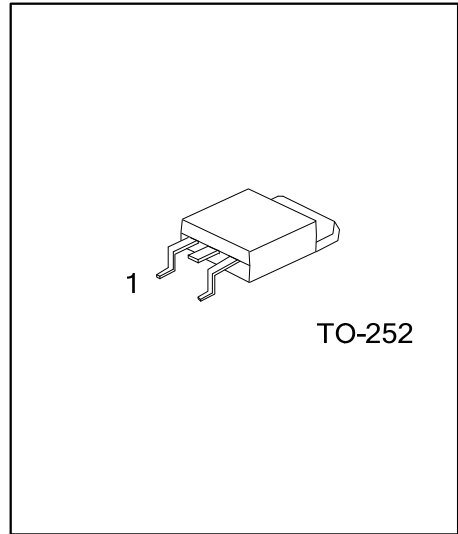


■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT50P04L-TN3-R	UTT50P04G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UTT50P04L-TN3-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Lead Free 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	-40	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous (Note 2)	I_D	$T_C=25^\circ\text{C}$	-60 (Note 3)	A
			$T_C=100^\circ\text{C}$	-43	A
	Pulsed	I_{DM}	-100	A	
Continuous Source Current (Diode Conduction)		I_S	-60 (Note 3)	A	
Avalanche Current		I_{AR}	-40	A	
Avalanche Energy		E_{AS}	80	mJ	
Power Dissipation (Note 2)	$T_C=25^\circ\text{C}$	P_D	93.7 (Note 2)	W	
	$T_A=25^\circ\text{C}$		3 (Note 1)	W	
Junction Temperature		T_J	-55~175	$^\circ\text{C}$	
Storage Temperature		T_{STG}	-55~175	$^\circ\text{C}$	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	$t \leq 10 \text{ sec.}$	θ_{JA}	18	$^\circ\text{C/W}$
	Steady State		50	
Junction to Case		θ_{JC}	1.6	

- Notes:
1. Surface Mounted on 1"x1" FR4 Board.
 2. See SOA curve for voltage derating.
 3. Calculated based on maximum allowable Junction Temperature. Package limitation current is 50A.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-40			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V			-1	μA
		V _{DS} =-40V, V _{GS} =0V, T _J =125°C			-50	
Gate- Source Leakage Current	Forward	I _{GSS}				nA
	Reverse					
		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 1)	R _{DS(ON)}	V _{GS} =-10V, I _D =-30A		0.0105	0.013	Ω
		V _{GS} =-10V, I _D =-30A, T _J =125°C			0.020	
		V _{GS} =-4.5V, I _D =-20A		0.017	0.022	
Forward Transconductance (Note 1)	g _{FS}	V _{DS} =-15V, I _D =-30A	15			S
On State Drain Current (Note 1)	I _{D(ON)}	V _{GS} =-10V, V _{DS} =-5V	-50			A
DYNAMIC PARAMETERS (Note 2)						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1MHz		3120		pF
Output Capacitance	C _{OSS}			440		pF
Reverse Transfer Capacitance	C _{RSS}			320		pF
Gate Resistance	R _G	f=1.0MHz		4.3		Ω
SWITCHING PARAMETERS (Note 2)						
Total Gate Charge (Note 3)	Q _G	V _{GS} =-10V, V _{DS} =-20V, I _D =-50A		63	95	nC
Gate to Source Charge (Note 3)	Q _{GS}			13		nC
Gate to Drain Charge (Note 3)	Q _{GD}			16		nC
Turn-ON Delay Time (Note 3)	t _{D(ON)}	V _{DD} =-20V, V _{GEN} =-10V, I _D ≈-50A, R _L =0.4 Ω, R _g =2.5Ω		15	25	ns
Rise Time (Note 3)	t _R			18	30	ns
Turn-OFF Delay Time (Note 3)	t _{D(OFF)}			60	90	ns
Fall-Time (Note 3)	t _F			47	70	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C=25°C)						
Maximum Body-Diode Pulsed Current	I _{SM}				-100	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _F =-50A, V _{GS} =0V		-1.0	-1.5	V
Body Diode Reverse Recovery Time	t _{RR}	I _F =-50A, di/dt=100A/μs		36	55	ns

- Notes: 1. Pulse test; pulse width≤300μs, duty cycles≤2%.
 2. Guaranteed by design, not subject to production testing.
 3. Independent of operating temperature.

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