S1D16700

Rev.1.1

CONTENTS

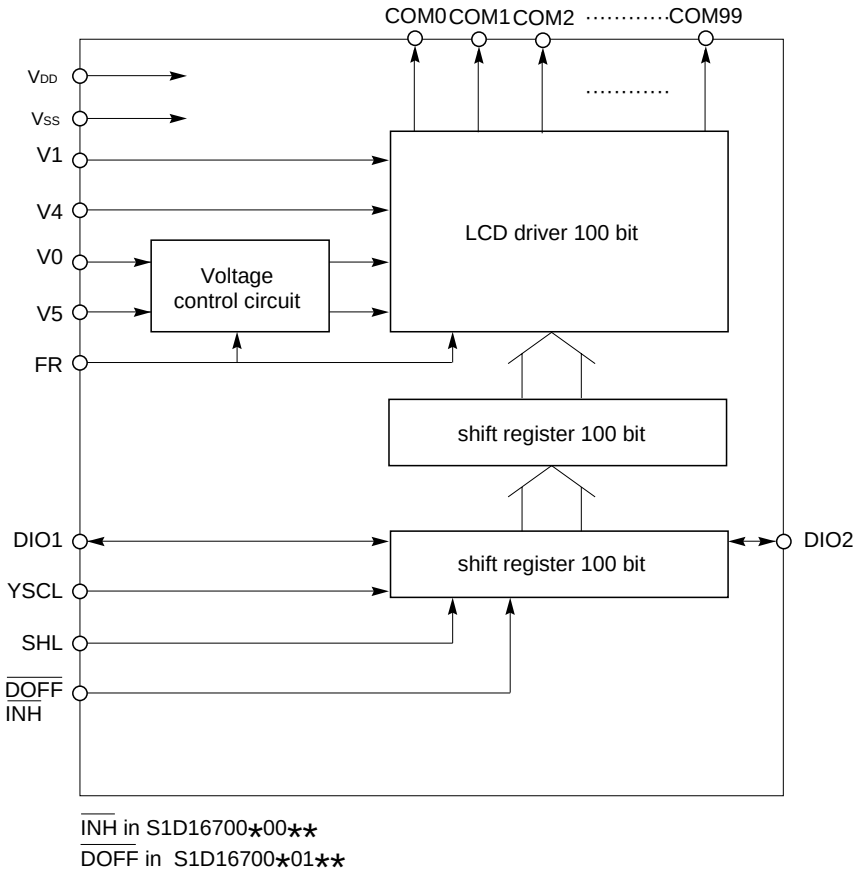
1. DESCRIPTION

The S1D16700 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels upto a duty ratio of 1/300. It is intended to be used in conjunction with the S1D16400 or S1D16006 as a pair.
Since the S1D16700 is so designed to drive LCDs over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.
And the S1D16700∗01∗∗ can display 65 x 132 panel when used as a common driver of RAM buit-in driver, S1D15301.

2. FEATURES

- Number of LCD drive output segments: 100
- Common output ON resistance: 700 Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 × 480 dots when used in combination with S1D 16400D or S1D16006D.
- Selectable pin output shift direction
- No-bias display OFF function (S1D16700∗01∗∗)
- Instantaneous display blanking enabled by inhibit function (S1D16700∗00∗∗)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Shipping pattern
  S1D16700D00A∗ (Al pad chip)
  S1D16700D01A∗ (Al pad chip)
  S1D16700D00B∗ (Au bump chip)
  S1D16700D01B∗ (Au bump chip)
  S1D16700T00A∗ (TCP)
  S1D16700T01A∗ (TCP)
- No radial rays countermeasure taken in designing

3. BLOCK DIAGRAM



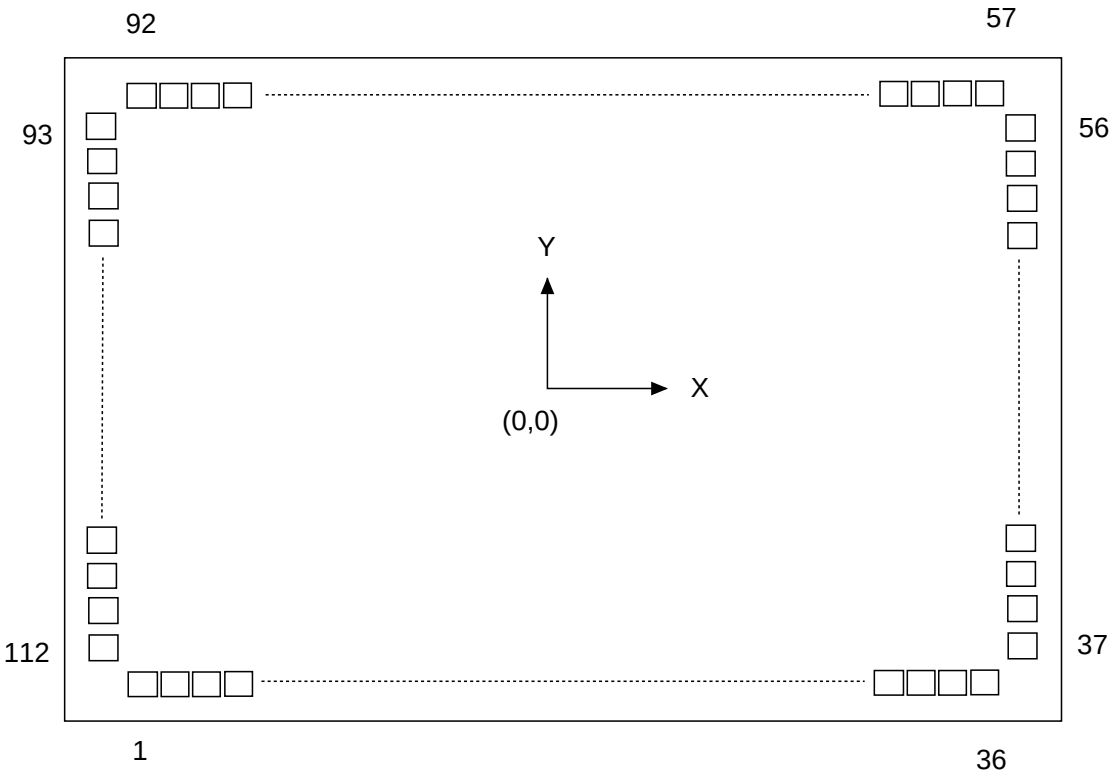
4. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>COM0 to COM099</td><td>O</td><td>LCD drive common (row) output
The output changes at the YS CL falling edge.</td><td>100</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>100-bit shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>COM output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>LOW</td><td>0 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>HIGH</td><td>99 → 0</td><td>Ourput</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LCD display blanking control input
When LOW is input, the content of shift register is cleared and all common outputs become the V_0 level instantaneously (S1D16700D01B*).</td><td>1</td></tr>
<tr><td>($\overline{INH}$)</td><td>I</td><td>LCD drive display blanking control input
When LOW is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously.
Common output = V_4 (when FR = LOW)
Common output = V_1 (when FR = HIGH) (S1D16700D00B*)</td><td>(1)</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –5.0 V</td><td>2</td></tr>
<tr><td>V0, V1, V4, V5</td><td>Power supply</td><td>LCD drive power supply V_5: –7 V to –28 V
$V_{DD} \geq V_0 \geq V_1 > V_4 \geq V_5$</td><td>4</td></tr>
</table>

$\overline{INH}$ for S1D16700*00** Total: 112
$\overline{DOFF}$ for S1D16700*01**

5. PAD

• Pad layout



Chip size ..... 5.49mm × 3.03mm
Chip thickness ..... 525μm (Au-bump die from)
400μm (Al-Pad die from)

1) Au bump specification reference values

Bump specific : High Quarity Au bump
Bump size : 90μm × 90μm
Bump height : 17μm ~ 28μm

2) AL Pad specification reference values

Pad Opening : 100μm × 100μm

● Pad center coordinates

PAD		Actual dimensions	
NO.	NAME	X	Y
1	COM5	-2187	-1357
2	6	-2058	
3	7	-1929	
4	8	-1799	
5	9	-1670	
6	10	-1541	
7	11	-1412	
8	12	-1283	
9	13	-1153	
10	14	-1024	
11	15	-895	
12	16	-766	
13	17	-637	
14	18	-507	
15	19	-378	
16	20	-249	
17	21	-120	
18	22	10	
19	23	139	
20	24	268	
21	25	397	
22	26	526	
23	27	656	
24	28	785	
25	29	914	
26	30	1043	
27	31	1172	
28	32	1302	
29	33	1431	
30	34	1560	
31	35	1689	
32	36	1818	
33	37	1948	
34	38	2077	
35	39	2206	
36	40	2335	-1357
37	41	2584	-1231
38	42	2584	-1094
39	43	2584	-969
40	44	2584	-840

PAD		Actual dimensions	
NO.	NAME	X	Y
41	COM45	2584	-711
42	46		-581
43	47		-452
44	48		-323
45	49		-194
46	50		-65
47	51		65
48	52		194
49	53		323
50	54		452
51	55		581
52	56		711
53	57		840
54	58		969
55	59		1098
56	60	2584	1231
57	61	2298	1357
58	62	2168	
59	63	2039	
60	64	1910	
61	65	1781	
62	66	1652	
63	67	1522	
64	68	1393	
65	69	1264	
66	70	1135	
67	71	1006	
68	72	876	
69	73	747	
70	74	618	
71	75	489	
72	76	360	
73	77	230	
74	78	101	
75	79	-28	
76	80	-157	
77	81	-286	
78	82	-416	
79	83	-545	
80	84	-674	1357

PAD		Actual dimensions	
NO.	NAME	X	Y
81	COM85	-803	1357
82	86	-932	
83	87	-1062	
84	88	-1191	
85	89	-1320	
89	90	-1449	
87	91	-1578	
88	92	-1708	
89	93	-1837	
90	94	-1966	
91	95	-2095	
92	96	-2224	1357
93	97	-2473	1334
94	98		1201
95	99		1071
96	DIO2		941
97	$\overline{\text{DOFF}}$		715
(97)	($\overline{\text{INH}}$)		
98	FR		585
99	YSCL		455
100	SHL		325
101	V_{DD}		185
102	V_{SS}		46
103	V0		-112
104	V1		-252
105	V4		-391
106	V5		-531
107	DIO1		-671
108	COM0		-810
109	1		-941
110	2		-1071
111	3		-1201
112	4	-2473	-1334

PAD No. 97: $\overline{\text{INH}}$ for S1D16700★00★★
$\overline{\text{DOFF}}$ for S1D16700★01★★

6. FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver circuit

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal DOFF, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

(S1D16700★01★★)

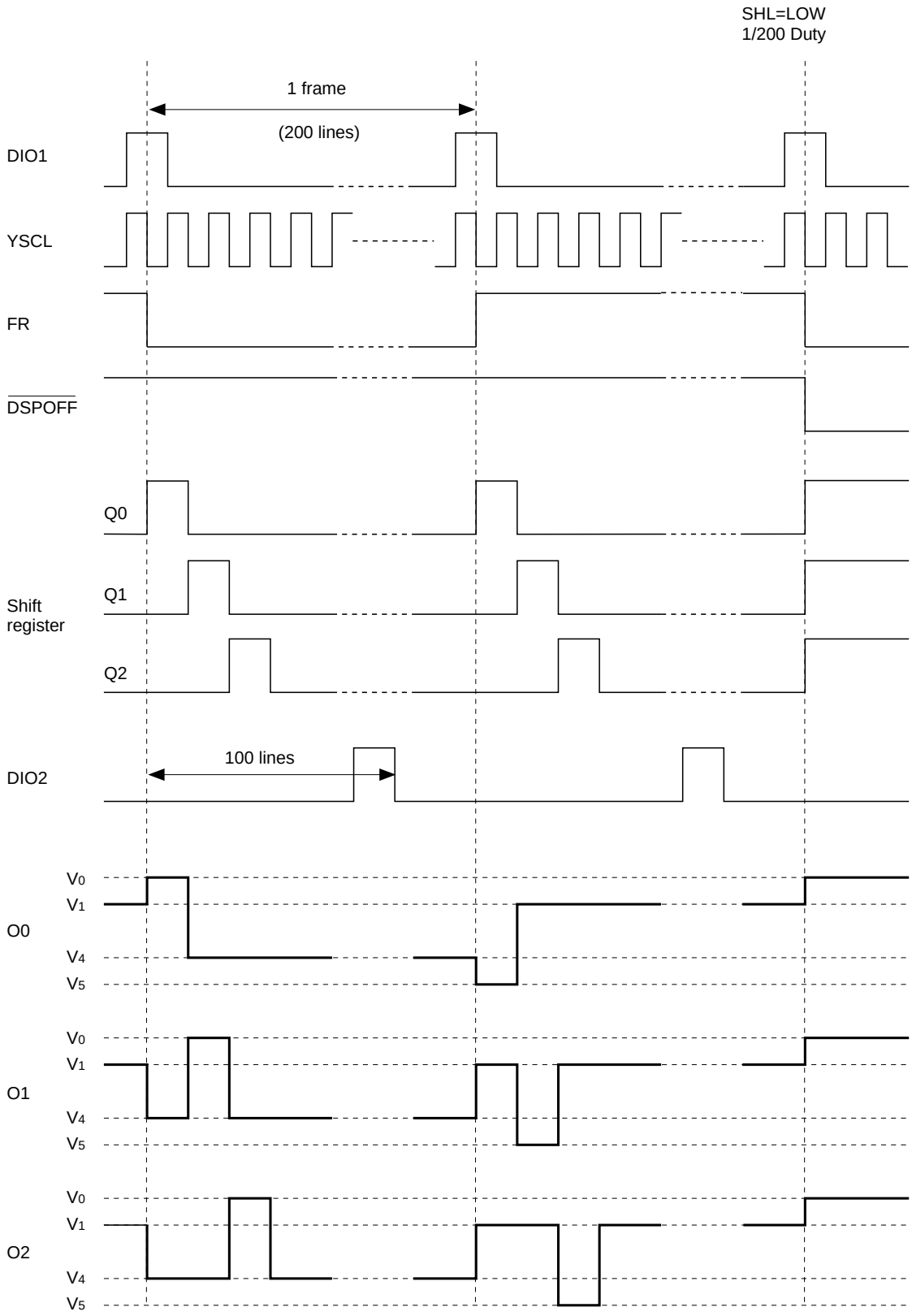
$\overline{DOFF}$	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V_5	(Select level)
		LOW	V_0	
	LOW	HIGH	V_1	(Non-select level)
		LOW	V_4	
LOW	Fixed to LOW	–	V_0	–

The relationship among the display blanking signal INH, contents of the shift register, AC converted signal FR and COM output voltage is as shown in the table below:

(S1D16700★00★★)

INH	Contents of shift register	FR	COM output voltage	
HIGH	HIGH	HIGH	V_5	(Select level)
		LOW	V_0	
	LOW	HIGH	V_1	(Non-select level)
		LOW	V_4	
LOW	Fixed to LOW	HIGH	V_1	(Non-select level)
		LOW	V_4	

7. TIMING CHART (S1D16700D01B∗)



The V1 or V4 non-select level is output corresponding to the FR in S1D16700D00B∗ or $\overline{INH}$=LOW, respectively.

8. ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg	–65 to +150	°C

Notes:
1. The voltage of V_0, V_1 and V_4 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

9. ELECTRICAL CHARACTERISTICS

DC characteristics

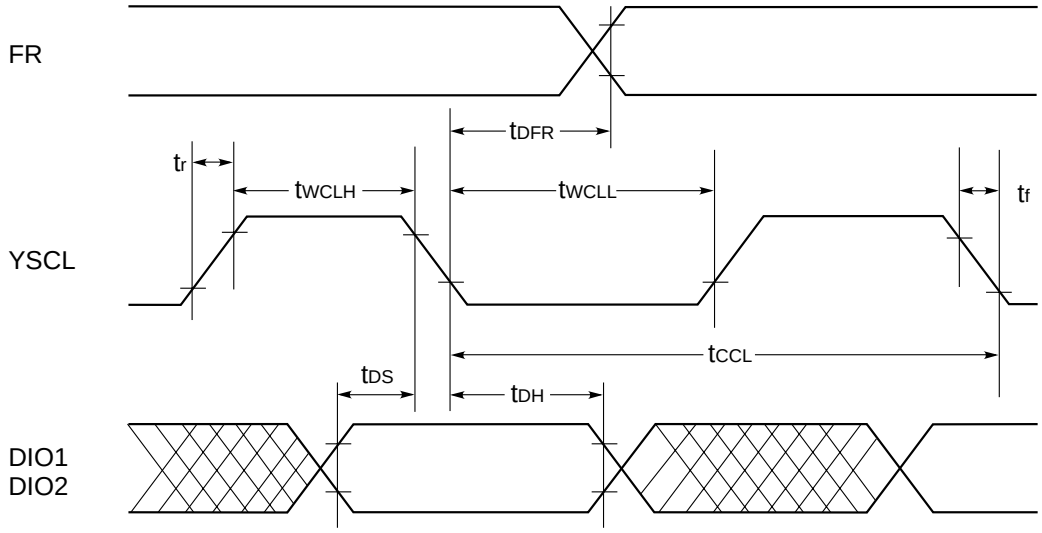
Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10%, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
HIGH input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2, YSCL, SHL, FR
LOW input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	
HIGH input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{DOFF}$, $\overline{INH}$
LOW input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
HIGH output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
LOW output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–7.0 to –28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON =0.5V, V_5= –20.0V, When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	kΩ	COM0~COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, V_{IH}=VDD, V_{IL}=V_{SS}, f_{YSCL}=12KHz, Frame frequency=60Hz Input data; “H” at no load every 1/200 duty	–	7	15	µA	V_{SS}
		Other conditions are the same as V_{SS} = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0, V,=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of I_{SS1}.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

AC Characteristics

Input timing characteristics

$V_{IH}=0.2 \times V_{SS}$
$V_{IL}=0.8 \times V_{SS}$



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

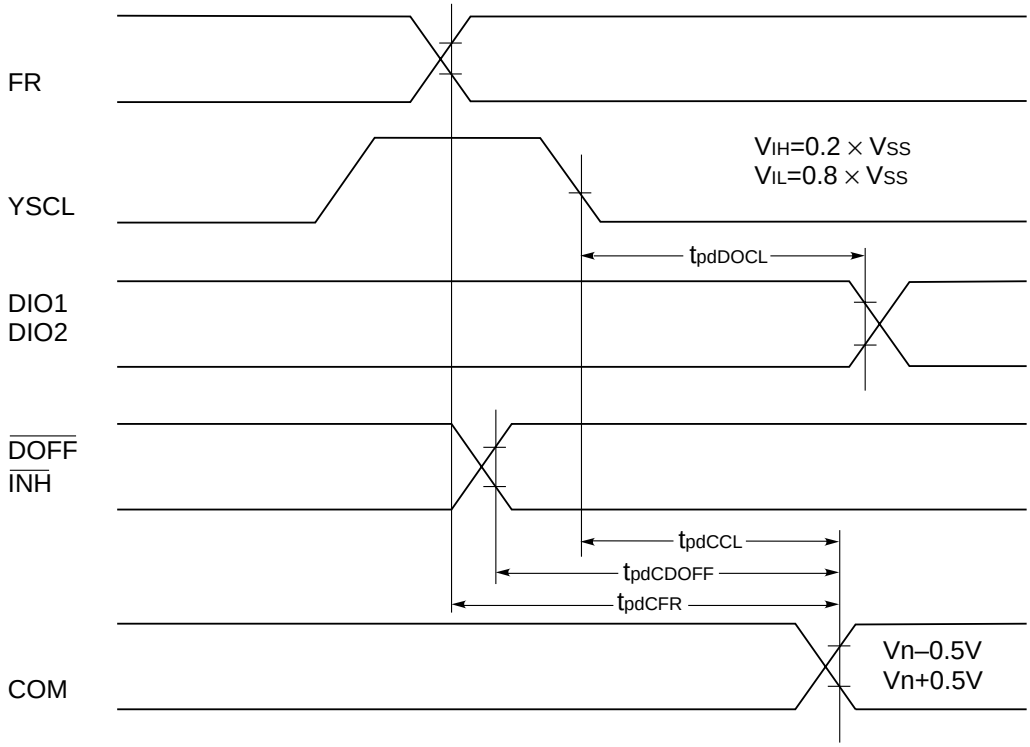
Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL HIGH pulsewidth	t_{WCLH}	–	70	–	ns
YSCL LOW pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL HIGH pulsewidth	t_{WCLH}	–	160	–	ns
YSCL LOW pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

The standard applicable to t_{CCL}, t_{WCLH}, t_{WCLL} and t_{DS} when V_{SS} = –2.4 V shall be 1.3 times of that applies when V_{SS} = –2.7V to –4.5V.

Output timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	CL=15pF	30	300	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V CL=100pF	–	3.0	µs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}		–	3.0	µs

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	CL=15pF	60	600	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V CL=100pF	–	3.0	µs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}		–	3.0	µs

The standard applicable at V_{SS} = –2.4V shall be the same as that employed when V_{SS} = –2.7V to –4.5V.

10. LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example. On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.
Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level V0 for LCD driving has been isolated from the V_{DD} pin.
When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.
When no operational amplifier is used, connect V_0 and V_{DD} pins.

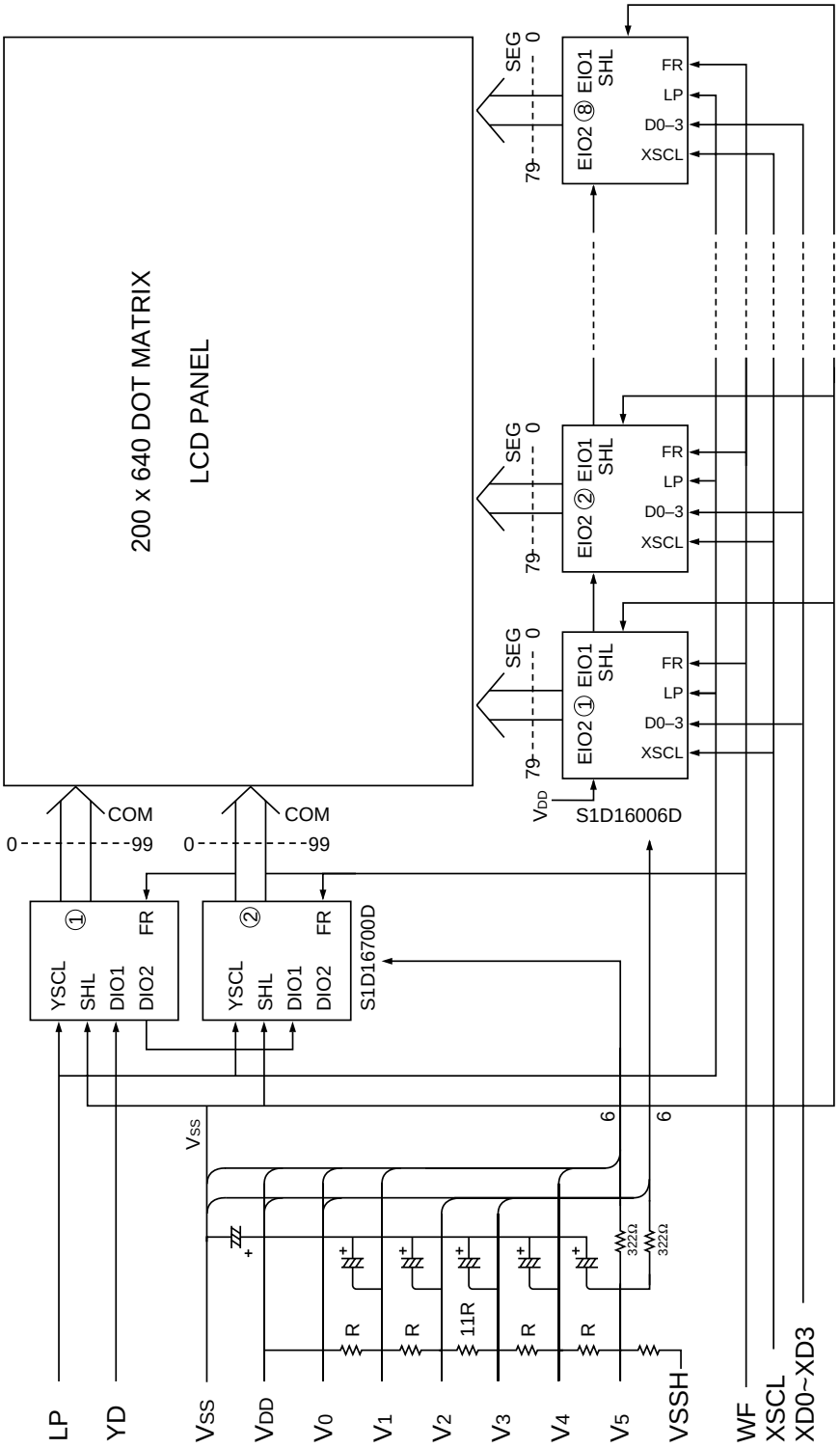
Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

11. CONNECT EXAMPLE



Note *1 It must be provided as the protective resister against overcurrent. Also, the bypass capacitor (0.01 μF) for noise suppression must be provided near to VSS and V5 terminals on each LSI.