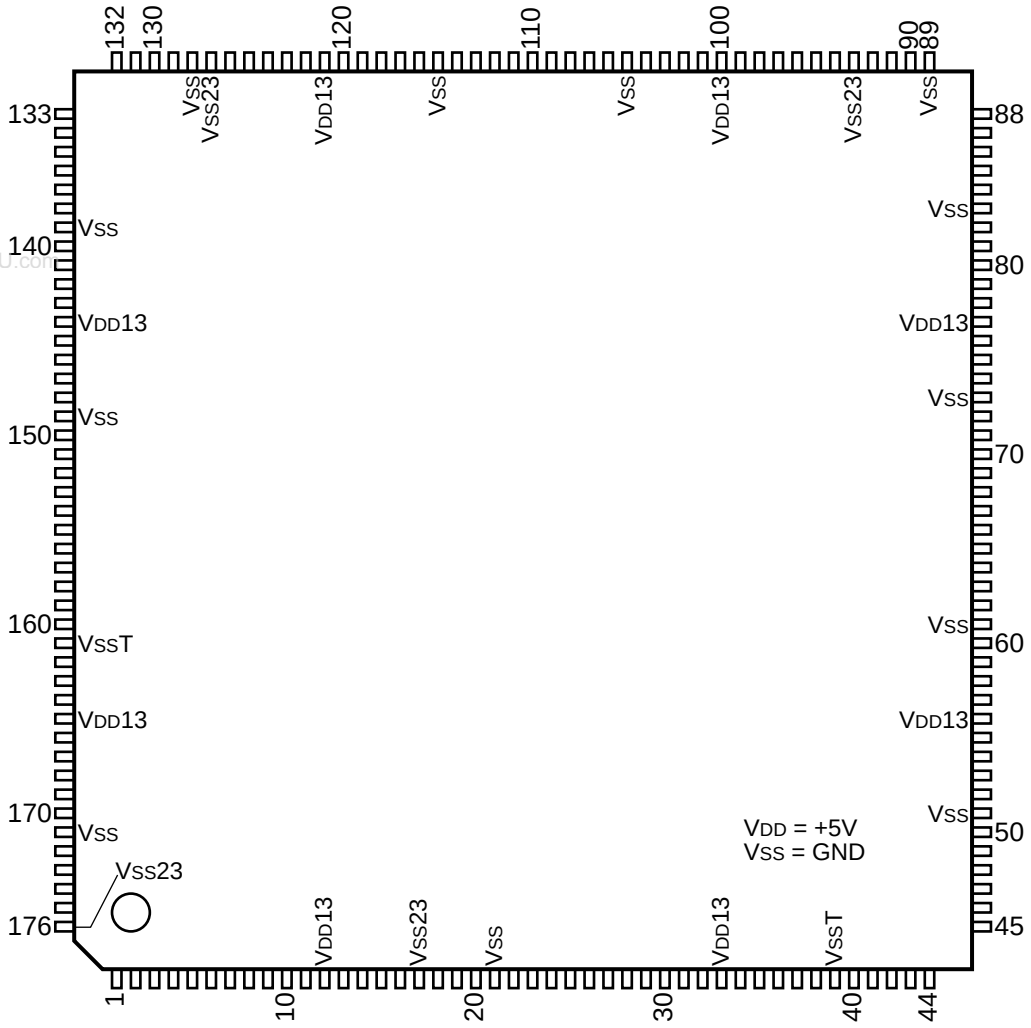
* * * * *

C-MOS RLL 1-7 DECODER (GATE ARRAY)

–TOP VIEW–



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	A17I	45	O	PIPLSO NO	89	—	VSS	133	O	RDAT0 1TO
2	I	A3I	46	O	TEPLSO TO	90	I	RDAT 1NI	134	O	RDAT1 1TO
3	I	A2I	47	O	PIPLSO TO	91	I	RCLK 1NI	135	O	MSEL0 1TO
4	I	A1I	48	O	DSND0O	92	I	SMARK 1NI	136	O	MSEL1 1TO
5	I	CS1I	49	O	DSND1O	93	—	VSS23	137	O	BSH 1TO
6	I	CS2I	50	O	DSND2O	94	I	SEN 1I	138	O	PSH 1TO
7	I	CS3I	51	—	VSS	95	I	REFN CKI	139	—	VSS
8	I	CS5I	52	O	DSND3O	96	O	RDAT0 1NO	140	O	RSH 1TO
9	I	CS6I	53	O	DSND4O	97	O	RDAT1 1NO	141	O	EQS 1TO
10	I	DPWAITI	54	O	DSND5O	98	O	MSEL0 1NO	142	O	DBIAS 1TO
11	I	RDI	55	O	DSND6O	99	O	MSEL1 1NO	143	O	DPEAK 1TO
12	—	VDD13	56	—	VDD13	100	—	VDD13	144	—	VDD13
13	I	WRLI	57	O	DSND7O	101	O	BSH 1NO	145	O	SM 1TO
14	I	WRHI	58	O	DSND8O	102	O	PSH 1NO	146	O	REN 1TO
15	I	RESETI	59	O	DSND9O	103	O	RSH 1NO	147	O	WST 1TO
16	I	MONISELI	60	O	DSND10O	104	O	EQS 1NO	148	O	CRCERR TO
17	—	VSS23	61	—	VSS	105	—	VSS	149	—	VSS
18	I	CRC FORMI	62	O	DSND11O	106	O	DBIAS 1NO	150	O	DCLK 1TO
19	I	AMPATTI	63	O	DSND12O	107	O	DPEAK 1NO	151	I	TESTI
20	I	SM SELI	64	O	DSND13O	108	O	SM 1NO	152	I	TEST2I
21	—	VSS	65	O	DSND14O	109	O	REN 1NO	153	I/O	D0IO
22	O	RAMCSO	66	O	DSND15O	110	O	WST 1NO	154	I/O	D1IO
23	O	PIOCSO	67	I	DST RDI	111	O	CRCERR NO	155	I/O	D2IO
24	O	DSPNCSO	68	I	DST CSI	112	O	DCLK 1NO	156	I/O	D3IO
25	O	DSPTCSO	69	O	TRVDIRTO	113	O	CRCDATAMO	157	I/O	D4IO
26	O	PIO2CSO	70	O	DSTD0O	114	O	SYNDETMO	158	I/O	D5IO
27	O	DAWRO	71	O	DSTD1O	115	—	VSS	159	I/O	D6IO
28	O	WAITO	72	O	DSTD2O	116	O	RSDETMO	160	I/O	D7IO
29	O	CS2SP1O	73	—	VSS	117	O	QADRDATMO	161	—	VSST
30	O	CS2SP2O	74	O	DSTD3O	118	O	AMDETMO	162	I/O	D8IO
31	I	TRT UNLOCKI	75	O	DSTD4O	119	O	SEC ENDMO	163	I/O	D9IO
32	I	TRN UNLOCKI	76	O	DSTD5O	120	O	SYRS DETMO	164	I/O	D10IO
33	—	VDD13	77	—	VDD13	121	—	VDD13	165	—	VDD13
34	I	TCNT TI	78	O	DSTD6O	122	O	REENMO	166	I/O	D11IO
35	I	TCNT NI	79	O	DSTD7O	123	O	SMCCLRMO	167	I/O	D12IO
36	I	PUP TI	80	O	DSTD8O	124	O	AMWINMO	168	I/O	D13IO
37	I	PUP NI	81	O	DSTD9O	125	O	SYNWINMO	169	I/O	D14IO
38	I	HOLDI TI	82	O	DSTD10O	126	O	DAREAMO	170	I/O	D15IO
39	—	VSST	83	—	VSS	127	—	VSS23	171	—	VSS
40	I	HOLDI NI	84	O	DSTD11O	128	—	VSS	172	I	CLK20MW
41	I	DSN RDI	85	O	DSTD12O	129	I	REFT CKI	173	I	CLK20M
42	I	DSN CSI	86	O	DSTD13O	130	I	RDAT 1TI	174	I	A19I
43	O	TRVDIRNO	87	O	DSTD14O	131	I	RCLK 1TI	175	I	A18I
44	O	TEPLSO NO	88	O	DSTD15O	132	I	SMARK 1TI	176	—	VSS23

VDD = +5V VSS = GND

INPUT

A1I~3I	; ADDRESS BUS
A17I~9I	; ADDRESS BUS
AMPATTI	; ADDRESS MARK PATTERN CONTROL
CLK20MI	; 20 MHz CLOCK
CLK20MWI	; WINDOW PULSE GENERATOR MASTER CLOCK
CRC FORMI	; CRCC PATTERN DETECT CONTROL FOR TRACK AND SECTOR
CS1I~6I	; CHIP SELECT
DPWAITI	; CHIP SELECT WAIT
DSN CSI, DSN RDI, DST CSI, DST RDI	; TRAVERSE COUNTER READ CONTROL FROM DSP
HOLDI NI, HOLDI TI	; TRAVERSE COUNTER HOLD MODE
MONISELI	; MONITOR OUTPUT SIGNAL SELECT
PUP NI, PUP TI, TCNT NI, TCNT TI	; CLOCK PULSE INPUT FOR TRAVERSE COUNTER
RCLK 1NI, RCLK 1TI	; CLOCK SYNCHRONIZED TO RDAT (TTL INPUT)
RDAT 1NI, RDAT 1TI	; DISK DATA PLAYBACK (TTL INPUT) FROM RF
RDI	; DATA BUS READ
REFN CKI, REFT CKI	; REFERENSE CLOCK (SAME FREQUENCY AS RCLK)
RESETI	; SYSTEM RESET
SEN 1I	; DATA READ ENABLE
SM SELI	; WINDOW PULSE DECODE SELECT
SMARK 1NI, SMARK 1TI	; SECTOR MARK DETECT
TEST	; TEST PIN
TRN UNLOCKI, TRT UNLOCKI	; TRACKING ERROR ACKNOWLEDGE
WRHI, WRLI	; DATA BUS WRITE

OUTPUT

AMDETO	; ADDRESS MARK DETECT RESULT
AMWINMO	; ADDRESS MARK DETECT WINDOW
BSH INO, BSH 1TO	; BIAS LOOP SAMPLE HOLD
CRCDATAMO	; CRCC DETECT RESULT
CRCERR NO, CRCERR TO	; CRCC ERROR SIGNAL
CS2SP1O, CS2SP2O, DSPNCSO, DSPTCSO, PI0CSO, PI02CSO, RAMCSO	; CHIP SELECT
D0IO~D15IO	; DATA BUS
DAREAMO	; VALID DATA AREA
DAWRO, WAITO	; WAIT CONTROL
DBIAS 1NO, DBIAS ITO	; BIAS LOOP TEST ENABLE
DCLK 1NO, DCLK 1TO	; CLOCK SHNCHRONIZED TO RDAT0 AND RDAT1
DPEAK 1NO, DPEAK 1TO	; PEAK LOOP TEST ENABEL
DSND0O~DSND15O, DSTDO~DSTD15O	; DATA BUS
EQS 1NO, EQS 1TO	; EQ START SIGNAL
MSEL0 1NO, MSEL0 1TO, MSEL1 1NO, MSEL1 1TO	; RF MODE SELECT
PIPLSO NO, PIPLS0 TO, TEPLSO NO, TEPLS0 TO	; CLOCK PULSE FOR TRAVERSE COUNTER
PSH 1NO, PSH 1TO	; PEAK LOOP SAMPLE HOLD
QADRDATMO	; RDAT LATCH BY RCLK
RDAT0 1NO, RDAT0 ITO, RDAT1 1NO, RDAT1 1TO	; NRZI AND RLL CONVERT
REENMO	; SECTOR READ ENABLE
REN 1NO, REN 1TO	; DATA READ ENABLE
RSDETMO	; RESYNC DETECT RESULT
RSH 1NO, RSH 1TO	; READ SAMPLE HOLD
SEC ENDMO	; SECTOR END DETECT RESULT
SM 1NO, SM 1TO	; SECTOR MARK REGENERATE
SMCCLRMO	; CLEAR SIGNAL BY SECTOR MARK
SYNDETMO	; SYNC DETECT RESULT
SYRS DETMO	; SYNC AND RESYNC OR BETWEEN DETECT AND AUTO CORRECT
SYNWINMO	; SYNC DETECT WINDOW
TRVDIRNO,TRVDIRTO	; TRAVERSE COUNTER COUNT DIRECTION
WST 1NO, WST 1TO	; WRITE START