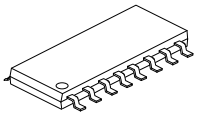
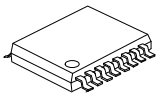
U74HC165

CMOS IC

8-BIT PARALLEL-LOAD SHIFT REGISTER



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74HC165** is an 8-bit parallel-load shift register that, when clocked, shifts the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A-H) inputs that are enabled by a low level at shift/load (SH/ $\overline{LD}$) input. The U74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

■ FEATURES

* Complementary Outputs
* Direct Overriding Load (Data) Inputs
* Gated Clock Inputs
* Parallel-to-Serial Data Conversion

■ ORDERING INFORMATION

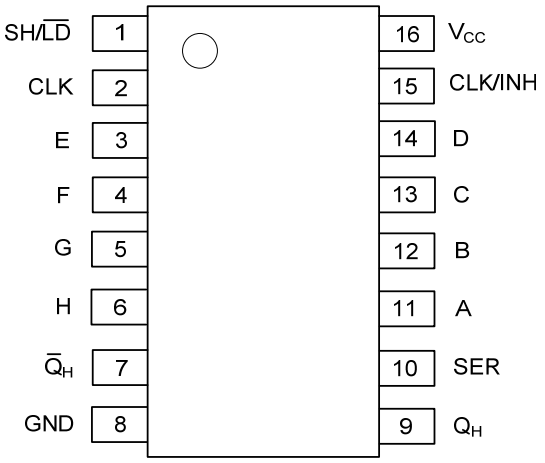
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC165L-S16-T	U74HC165G-S16-T	SOP-16	Tube
U74HC165L-S16-R	U74HC165G-S16-R	SOP-16	Tape Reel
U74HC165L-P16-T	U74HC165G-P16-T	TSSOP-16	Tube
U74HC165L-P16-R	U74HC165G-P16-R	TSSOP-16	Tape Reel

U74HC165L-S16-T

(1) Packing Type
(2) Package Type
(3) Lead Free

(1) T: Tube, R: Tape Reel
(2) S16: SOP-16, P16: TSSOP-16
(3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION

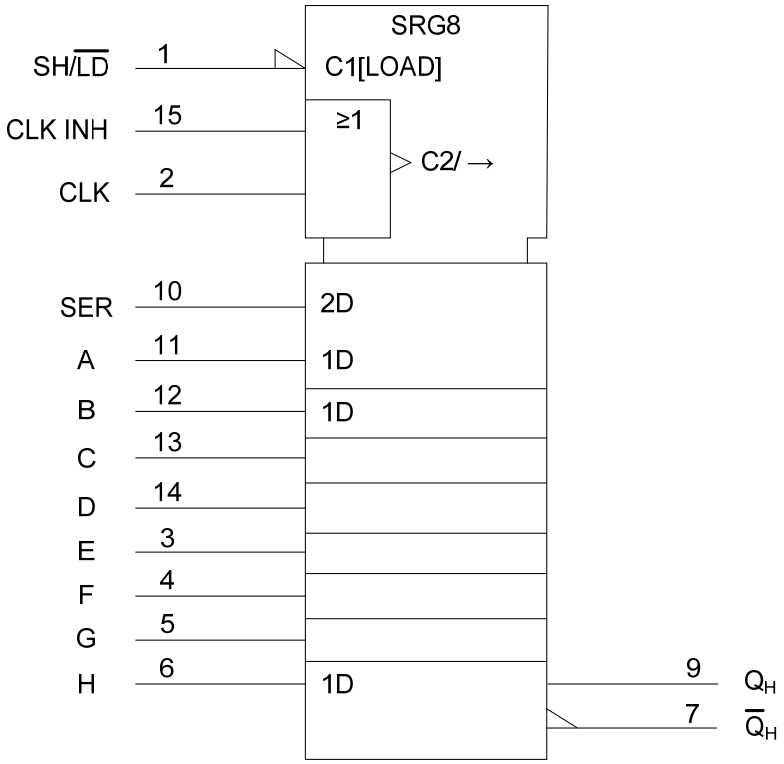


■ FUNCTION TABLE

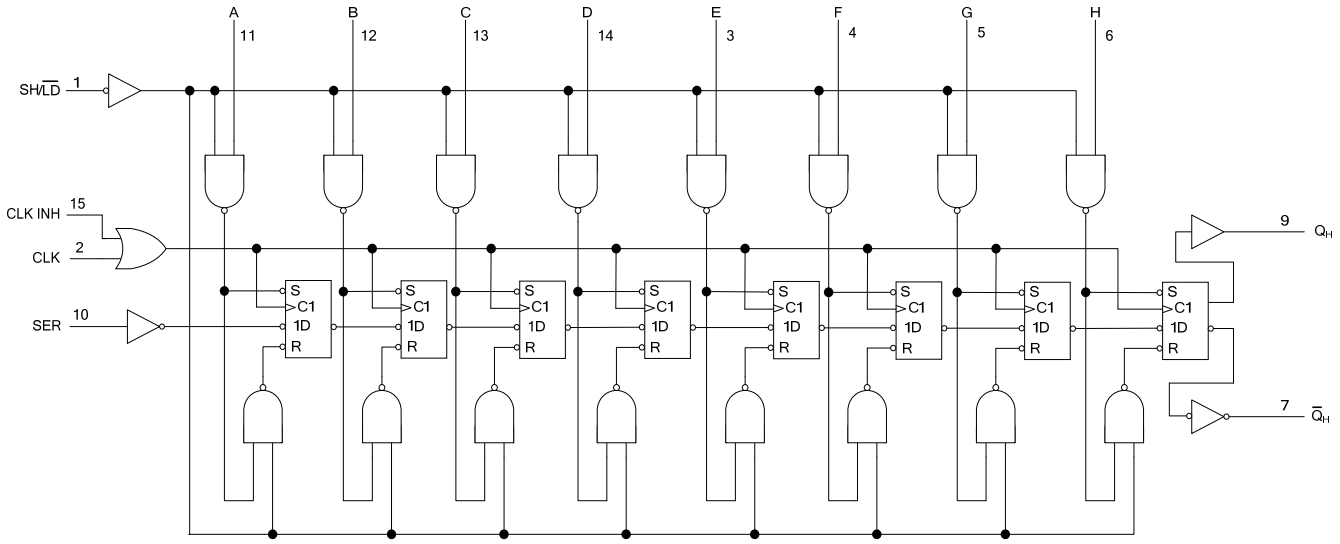
INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift↑
H	↑	L	Shift↑

↑ Shift=content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

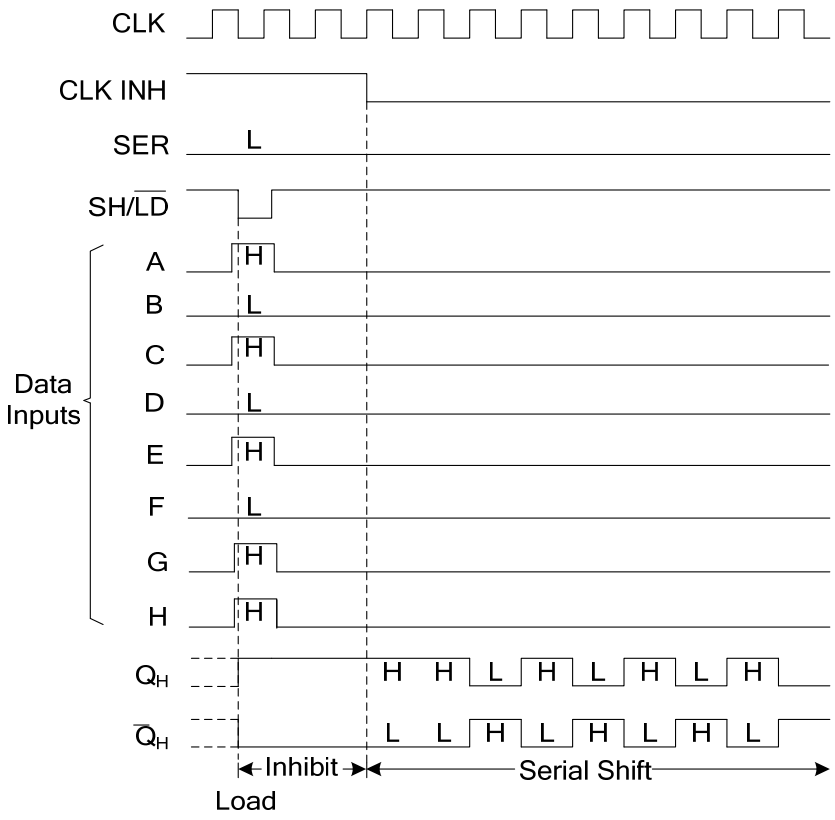
■ LOGIC SYMBOL



■ LOGIC DIAGRAM (positive logic)



■ TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCE



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}	±50	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL RESISTANCES

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	TSSOP-16		110	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			
		V_{CC}=6V	4.2			
Low-level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	
		V_{CC}=6V			1.8	
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition (Rise and Fall) Time	t_t	V_{CC}=2V			1000	ns
		V_{CC}=4.5V			500	
		V_{CC}=6V			400	
Operating Free-air Temperature	T_A		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		
		V_{CC}=6V, I_{OH}=-5.2mA	5.48	5.8		
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1	
		V_{CC}=4.5V, I_{OL}=4mA		0.17	0.26	
		V_{CC}=6V, I_{OL}=5.2mA		0.15	0.26	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND		±0.1	±100	nA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Input Capacitance	C_I	V_{CC}=2V to 6V		3	10	pF

■ TIMING REQUIREMENTS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency	f_{clock}	V_{CC}=2V	0		6	MHz
		V_{CC}=4.5V	0		31	
		V_{CC}=6V	0		36	

■ TIMING REQUIREMENTS(Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration	SH/$\overline{LD}$ low	t_w	V_{CC}=2V	80			ns
			V_{CC}=4.5V	16			
			V_{CC}=6V	14			
	CLK high or low		V_{CC}=2V	80			
			V_{CC}=4.5V	16			
			V_{CC}=6V	14			
Setup time	SH/$\overline{LD}$ high before CLK↑	t_{SU}	V_{CC}=2V	80			ns
			V_{CC}=4.5V	16			
			V_{CC}=6V	14			
	SER before CLK↑		V_{CC}=2V	40			
			V_{CC}=4.5V	8			
			V_{CC}=6V	7			
	CLK INH low before CLK↑		V_{CC}=2V	100			
			V_{CC}=4.5V	20			
			V_{CC}=6V	17			
	CLK INH high before CLK↑		V_{CC}=2V	40			
			V_{CC}=4.5V	8			
			V_{CC}=6V	7			
	Data before SH/$\overline{LD}$ ↓		V_{CC}=2V	100			
			V_{CC}=4.5V	20			
			V_{CC}=6V	17			
Hold time	SER data after CLK↑	t_h	V_{CC}=2V	5			ns
			V_{CC}=4.5V	5			
			V_{CC}=6V	5			
	PAR data after SH/$\overline{LD}$ ↓		V_{CC}=2V	5			
			V_{CC}=4.5V	5			
			V_{CC}=6V	5			

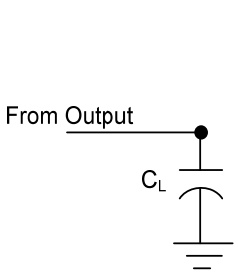
■ SWITCHING CHARACTERISTICS ($t_r = t_f$ = 6ns, C_L=50pF, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	V_{CC}	MIN	TYP	MAX	UNIT
Minimum Frequency Response	f_{max}	V_{CC}=2V	6	13		ns
		V_{CC}=4.5V	31	50		
		V_{CC}=6V	36	62		
Propagation delay from input (SH/$\overline{LD}$) to output(QH or $\overline{Q}_H$)	t_{PD}	V_{CC}=2V		80	150	ns
		V_{CC}=4.5V		20	30	
		V_{CC}=6V		16	26	
Propagation delay from input (CLK) to output(QH or $\overline{Q}_H$)		V_{CC}=2V		75	150	
		V_{CC}=4.5V		15	30	
		V_{CC}=6V		13	26	
Propagation delay from input (H) to output(QH or $\overline{Q}_H$)		V_{CC}=2V		75	150	
		V_{CC}=4.5V		15	30	
		V_{CC}=6V		13	26	
To Output(Any)	t_t	V_{CC}=2V		38	75	ns
		V_{CC}=4.5V		8	15	
		V_{CC}=6V		6	13	

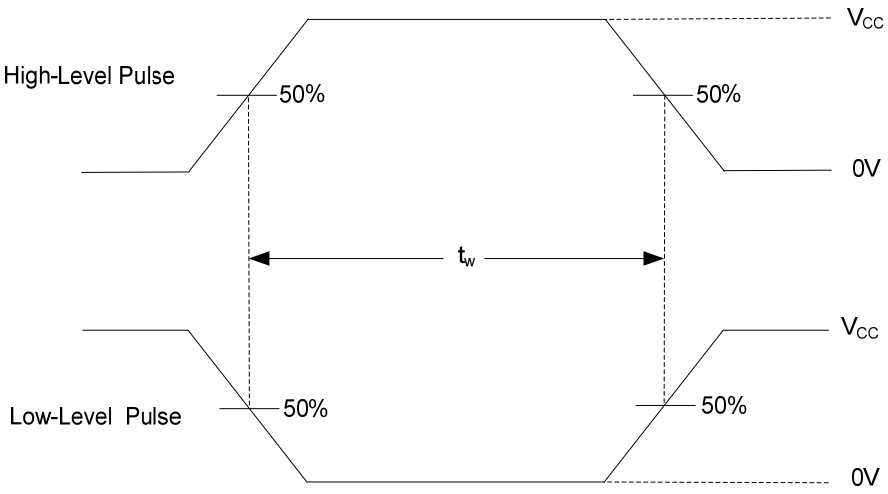
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		75		pF

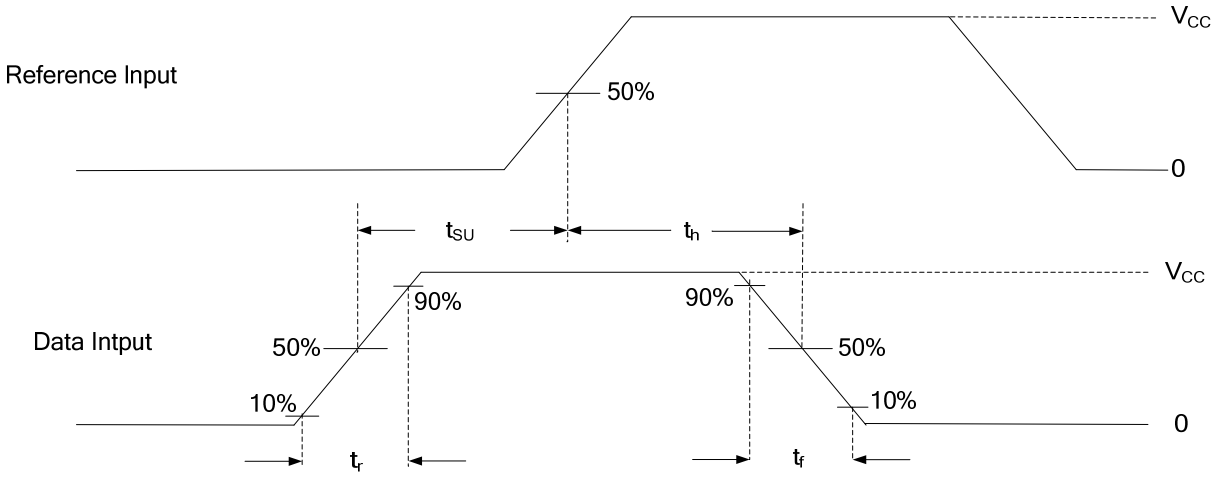
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

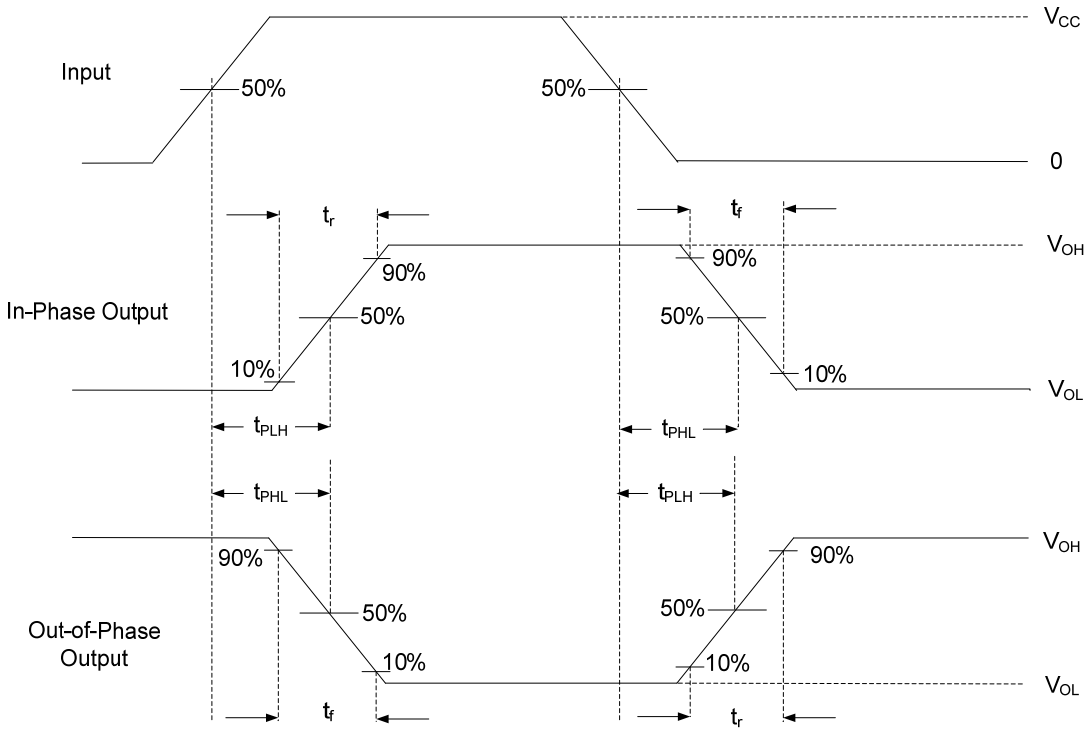


PULSE DURATIONS



SETUP AND HOLD AND INPUT RISE AND FALL TIMES

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES