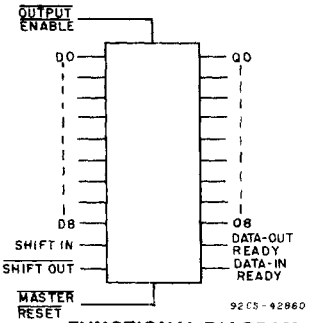
File Number **2122**

CD54/74HC7030
CD54/74HCT7030



FUNCTIONAL DIAGRAM

64-Word x 9-Bit FIFO Register; 3-State

Type Features:

- *Synchronous or asynchronous operation*
- *3-state outputs (standard)*
- *Master-reset inputs to clear data and control functions*
- *25-MHz (typ.) shift-in, shift-out rates with flags*
- *40-MHz (typ.) burst-in, burst-out rates without flags*
- *Cascadable to 25 MHz (typ.)*
- *Readily expandable in word and bit dimensions*
- *Pinning arranged for easy board layout: input pins directly opposite output pins*
- *I_{CC} category: LSI*
- *Functionally equivalent and pin capatible with the TRW to TDC1030*

The RCA-CD54HC/HCT7030 and CD74HC/HCT7030 are high-speed expandable silicon-gate CMOS first-in first-out (FIFO) memories organized as 64-word by 9-bit registers. A 25-MHz data-rates makes them ideal for high-speed applications. Burst data-rates of 40 MHz can be obtained in applications where the status flags are not used.

With separate controls for Shift-In (SI) and Shift-Out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a Master-Reset input ($\overline{MR}$) and and Output Enable Input ($\overline{OE}$). Flags for Data-In-Ready (DIR) and Data-Out-Ready (DOR) indicate the status of the device.

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

INPUTS AND OUTPUTS

Data Inputs (D_0 to D_8)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration, i.e. 8 x 64, 7 x 64, down to 1 x 64, by tying unused data input pins to V_{CC} or GND.

Data Outputs (Q_0 to Q_8)

As there is no weighting of the outputs any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open.

Master-Reset ($\overline{MR}$)

When $\overline{MR}$ is LOW, the control functions within the FIFO are cleared and data content is declared invalid; the Data-In-Ready (DIR) flag is set HIGH and the Data-Out-Ready flag (DOR) is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Applications:

- *Bit-rate smoothing*
- *CPU/terminal buffering*
- *Data communications*
- *Peripheral buffering*
- *Line printer input buffers*
- *Auto-dialers*
- *CRT buffer memories*
- *Radar data acquisition*
- *High-speed disc or tape controller*
- *Video synthesis*
- *I/O formatter for digital filters and FFTs*

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +125° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

CD54/74HC7030
CD54/74HCT7030

Status Flag Outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, Data-In-Ready (DIR) and Data-Out-Ready (DOR):

DIR = HIGH indicates the input stage is empty and ready to accept valid data;

DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete;

DOR = HIGH assures valid data is present at the outputs Q_0 to Q_8 (does not indicate that new data is awaiting transfer into the output stage);

DOR = LOW indicates the output stage is busy or there is no valid data.

Shift-In Control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process (ripple-through).

Shift-Out Control ($\overline{SO}$)

A LOW-to-HIGH transition of $\overline{SO}$ causes the DOR flag to go LOW. A HIGH-to-LOW transition of $\overline{SO}$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

Output Enable ($\overline{OE}$)

The outputs Q_0 to Q_8 are enabled when $\overline{OE}$ = LOW. When $\overline{OE}$ = HIGH the outputs are in the high impedance OFF-State.

These types are supplied in 28-lead dual-in-line plastic package E suffix. These types are also available in pellet (die) form H suffix.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltage referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC} +0.5$ V):
STANDARD OUTPUT ..... ±25 mA
BUS DRIVER OUTPUT ..... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):
STANDARD OUTPUT ..... ±50 mA
BUS DRIVER OUTPUT ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE H) ..... Derate Linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	
Operating Temperature, T_A:			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

* Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC7030
CD54/74HCT7030

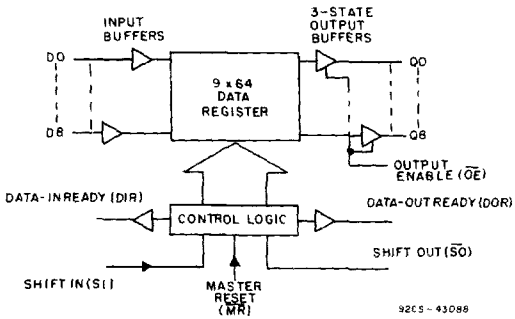


Fig. 1 - Functional block diagram.

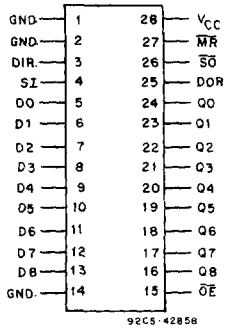


Fig. 2 - Terminal connections.

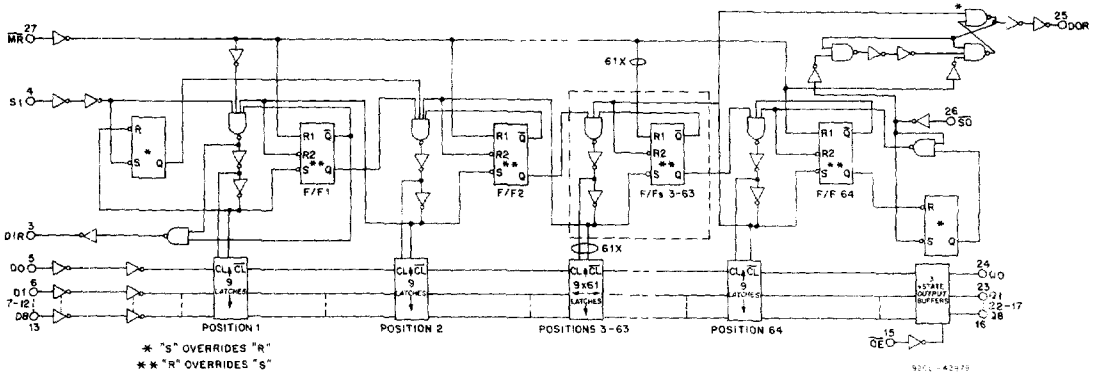


Fig. 3 - Logic diagram.

CD54/74HC7030
CD54/74HCT7030

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC7030/CD54HC7030										CD74HCT7030/CD54HCT7030										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current (LSI) I_{CC}	V_{CC} or Gnd	0	6	—	—	50	—	500	—	1000	V_{CC} or Gnd	5.5	—	—	50	—	500	—	1000		
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O=V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10		

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
$\overline{OE}$	1
SI, $\overline{SO}$, $\overline{MR}$	1.5
D_n	0.75

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC7030
CD54/74HCT7030

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay	t_{PLH} t_{PHL}				
$\overline{MR}$ to DIR, DOR		15	21	26	ns
$\overline{SO}$ to Q_n			36	40	
SI to DIR	t_{PHL}		20	21	
$\overline{SO}$ to DOR			25	26	
Maximum SI, $\overline{SO}$ Frequency		15	33	29	MHz
Power Dissipation Capacitance *	C_{PD}	—	660	660	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS +25° C HC MIN.	HC MAX.	HCT MIN.	HCT MAX.	-40° C to +85° C 74HC MIN.	74HC MAX.	74HCT MIN.	74HCT MAX.	-55° C to +125° C 54HC MIN.	54HC MAX.	54HCT MIN.	54HCT MAX.	UNITS
SI Pulse Width	t_w	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
HIGH or LOW		4.5	10	—	12	—	13	—	15	—	15	—	18	—	
Fig. 4		6	9	—	—	—	11	—	—	—	13	—	—	—	
$\overline{SO}$ Pulse Width	t_w	2	100	—	—	—	125	—	—	—	150	—	—	—	
HIGH or LOW		4.5	20	—	15	—	25	—	19	—	30	—	22	—	
Fig. 7		6	17	—	—	—	21	—	—	—	26	—	—	—	
DIR Pulse Width	t_w	2	50	145	—	—	—	180	—	—	—	220	—	—	
HIGH		4.5	10	29	13	37	—	36	—	46	—	44	—	56	
Fig. 5		6	9	25	—	—	—	31	—	—	—	38	—	—	
DOR Pulse Width	t_w	2	50	145	—	—	—	180	—	—	—	220	—	—	
HIGH		4.5	10	29	12	35	—	36	—	44	—	44	—	53	
Fig. 8		6	9	29	—	—	—	31	—	—	—	38	—	—	
$\overline{MR}$ Pulse Width	t_w	2	70	—	—	—	90	—	—	—	105	—	—	—	
LOW		4.5	14	—	18	—	18	—	23	—	21	—	27	—	
Fig. 6		6	12	—	—	—	15	—	—	—	18	—	—	—	
Removal Time	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{MR}$ to SI		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
Fig. 13		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time	t_{su}	2	-35	—	—	—	-45	—	—	—	-55	—	—	—	
D_n to SI		4.5	-7	—	-8	—	-9	—	-10	—	-11	—	-12	—	
Fig. 11		6	-6	—	—	—	-8	—	—	—	-9	—	—	—	
Hold Time		2	110	—	—	—	140	—	—	—	165	—	—	—	
D_n to SI		4.5	22	—	22	—	28	—	28	—	33	—	33	—	
Fig. 11		6	19	—	—	—	24	—	—	—	28	—	—	—	
Maximum Clock Pulse Frequency SI, $\overline{SO}$ (Burst Mode or Using Flags) Figs. 4, 7, 9 and 10	f_{MAX}	2	3.6	—	—	—	2.8	—	—	—	2.4	—	—	—	MHz
		4.5	18	—	15	—	14	—	12	—	12	—	10	—	
		6	21	—	—	—	16	—	—	—	14	—	—	—	
Maximum Clock Pulse Frequency SI, $\overline{SO}$ (Cascaded) Figs. 4 and 7	f_{MAX}	2	2.8	—	—	—	2.2	—	—	—	1.8	—	—	—	
		4.5	14	—	13	—	11	—	10	—	9.2	—	7.8	—	
		6	17	—	—	—	13	—	—	—	11	—	—	—	

CD54/74HC7030
CD54/74HCT7030

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
		+25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Propagation Delay t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	ns
$\overline{MR}$ to DIR, DOR t_{PLH}	4.5	—	42	—	51	—	53	—	53	—	63	—	63	
Fig. 6	6	—	36	—	—	—	45	—	—	—	54	—	—	
Propagation Delay t_{PLH}	2	—	235	—	—	—	295	—	—	—	355	—	—	
SI to DIR	4.5	—	47	—	49	—	59	—	61	—	71	—	74	
Fig. 4	6	—	40	—	—	—	50	—	—	—	60	—	—	
Propagation Delay t_{PHL}	2	—	315	—	—	—	395	—	—	—	475	—	—	
$\overline{SO}$ to DOR	4.5	—	63	—	67	—	79	—	84	—	95	—	101	
Fig. 7	6	—	50	—	—	—	63	—	—	—	76	—	—	
Propagation Delay t_{PHL}	2	—	35	—	—	—	45	—	—	—	55	—	—	
DOR to Q_n t_{PLH}	4.5	—	7	—	22	—	9	—	28	—	11	—	33	
Fig. 8	6	—	6	—	—	—	8	—	—	—	9	—	—	
Propagation Delay t_{PHL}	2	—	345	—	—	—	430	—	—	—	520	—	—	
$\overline{SO}$ to Q_n t_{PLH}	4.5	—	69	—	78	—	86	—	98	—	104	—	117	
Fig. 12	6	—	55	—	—	—	69	—	—	—	83	—	—	
Propagation Delay t_{PLH}	2	—	8	—	—	—	10	—	—	—	12	—	—	μs
Ripple through Delay	4.5	—	1.6	—	1.6	—	2	—	2	—	2.4	—	2.4	
SI to DOR Fig. 8	6	—	1.3	—	—	—	1.6	—	—	—	1.9	—	—	
Propagation Delay t_{PLH}	2	—	10	—	—	—	12.5	—	—	—	15	—	—	
Ripple through Delay	4.5	—	2	—	2	—	2.5	—	2.5	—	3	—	3	
$\overline{SO}$ to DIR Fig. 5	6	—	1.6	—	—	—	2	—	—	—	2.4	—	—	
3-State Output Enable t_{PZH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
$\overline{OE}$ to Q_n t_{PZL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
Fig. 14	6	—	30	—	—	—	37	—	—	—	45	—	—	
3-State Output Disable t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{OE}$ to Q_n t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
Fig. 14	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Standard Outputs t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
Fig. 12	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance C_O	—	—	15	—	15	—	15	—	15	—	15	—	15	

FUNCTIONAL DESCRIPTION

Data Input

Following power-up, the Master-Reset ($\overline{MR}$) input is pulsed LOW to clear the FIFO memory. The Data-In-Ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D_0 to D_8 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until SI is set to LOW. With SI = LOW the data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig. 6).

With the FIFO full, SI can be held LOW until a Shift-Out ($\overline{SO}$) pulse occurs. Then, following a Shift-Out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be Shifted-In (this data remains at the first FIFO location until SI again goes LOW) (see Fig. 5).

Data Transfer

After data has been transferred from the input stage to the FIFO following SI = LOW, the data moves through the FIFO asynchronous and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as the data moves through the device.

Data Output

The Data-Out Ready flag (DOR = HIGH) indicates that there is valid data the output (Q_0 to Q_8). The initial Master-Reset at power on ($\overline{MR}$ = LOW) sets DOR to LOW (see Fig. 6).

After $\overline{MR}$ = HIGH, data shifted onto the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the $\overline{SO}$ control input. With $\overline{SO}$ = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When $\overline{SO}$ is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW (see Fig. 11). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_8.

With the FIFO empty, the $\overline{SO}$ input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a Shift-Out of data occuring. The $\overline{SO}$ control must be made LOW before additional data can be shifted out (see Fig. 8).

High-Speed Burst Mode

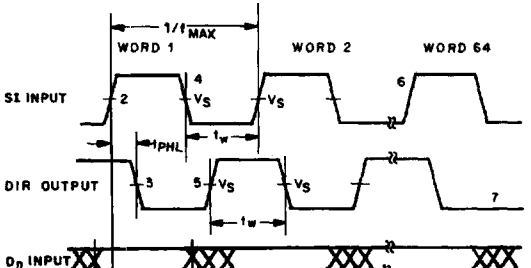
If it is assumed that the Shift-In/Shift-Out pulses are not applied until the respective status flags are valid, it follows that the Shift-In/Shift-Out rates are determined by the status flags. However, without the status flags a high-speed burst-mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse-widths of the Shift-In/Shift-Out inputs and burst rates of 40 MHz can be obtained. Shift pulses can be applied without regard to the status flags but Shift-In pulses that would overflow the storage capacity of the FIFO are not allowed (see Fig. 9 and 10).

Expanded Format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig. 19). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. Word length can be expanded beyond the 18-bits x 64 words configuration shown in Fig. 15.

The "7030" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs themselves. The inter-communications speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words x 9-bits (see Fig. 16).

AC WAVEFORMS



The above waveforms show the SI input to DIR output propagation delay times; the SI, DIR pulse widths; and the SI maximum pulse-frequency.

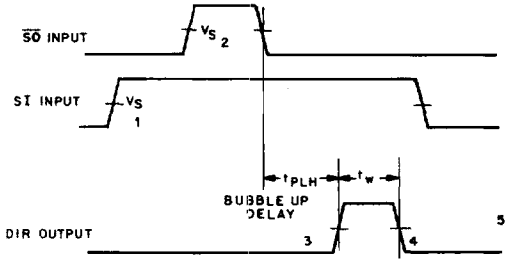
Fig. 4 - Shift-In sequence timing waveforms (FIFO empty to FIFO full).

TEST VOLTAGES FOR FIGS. 4 TO 14.

TEST VOLTAGE	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

NOTES:
1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage busy.
4. SI set LOW; data from first location "ripple through".
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd word through to 64th word into FIFO.
7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

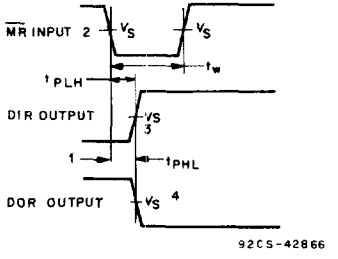
CD54/74HC7030
CD54/74HCT7030



The above waveforms show bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse-width.

Fig. 5 - Bubble-up delay timing waveforms.

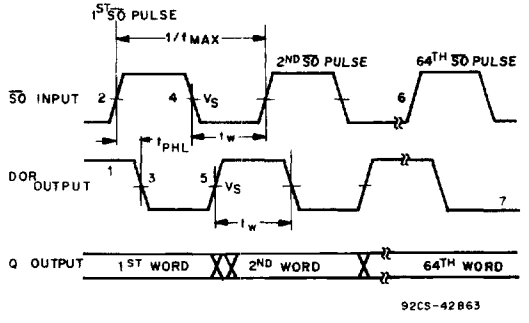
NOTES:
1. FIFO is initially full, shift-in is held HIGH.
2. $\overline{SO}$ pulse; data in the output stage is unloaded, bubble-up process of empty location begins.
3. DIR HIGH; when empty location reaches input stage, flag indicates FIFO is prepared for data input.
4. DIR goes LOW; data shift-in to empty location is complete, FIFO is full again.
5. SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.



The above waveforms show $\overline{MR}$ input to DIR, DOR output propagation delay times and the $\overline{MR}$ pulse-width.

Fig. 6 - $\overline{MR}$ input timing waveforms.

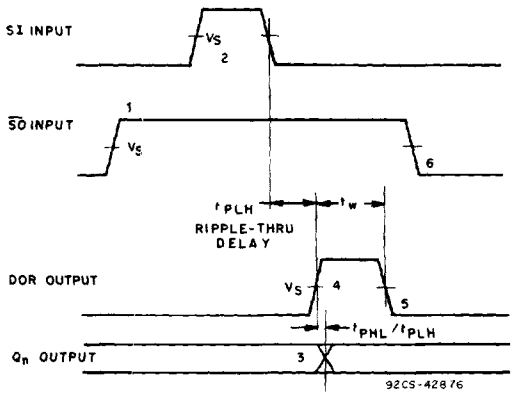
NOTES:
1. DIR LOW, output ready HIGH; assume FIFO is full.
2. $\overline{MR}$ pulse LOW; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.



The above waveforms show the $\overline{SO}$ input to DOR output propagation delay times, the $\overline{SO}$, DOR pulse-widths, and $\overline{SO}$ maximum pulse frequency.

Fig. 7 - $\overline{SO}$ input timing waveforms. (FIFO full to FIFO empty)

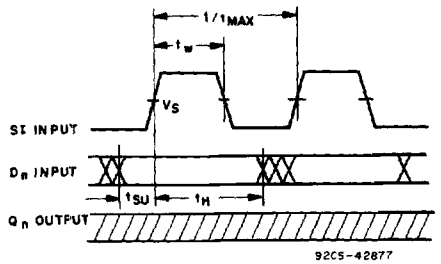
NOTES:
1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2. $\overline{SO}$ set HIGH; results in DOR going LOW.
3. DOR drops LOW; output stage busy.
4. $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location bubbles-up to input stage.
5. DOR goes HIGH; transfer process completed, valid data present at output.
6. Repeat process to unload the 3rd through to the 64th word from FIFO after the specified propagation delay times.
7. DOR remains LOW; FIFO is empty.



The above waveforms show ripple-through delay times, SI input to DOR output, DOR output pulse-width, and propagation delay times from the DOR pulse-width to the Q_n output.

Fig. 8 - Ripple-through delay timing waveforms.

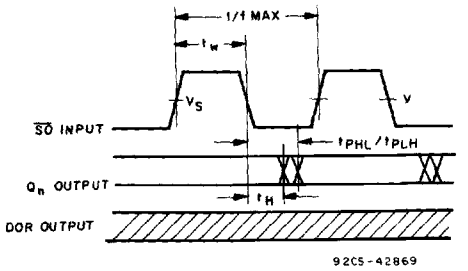
NOTES:
1. FIFO is initially empty, $\overline{SO}$ is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. Output transition; data arrrives at output stage (after specified propagation delay times between rising edge of the DOR pulse to Q_n output).
4. DOR HIGH; DOR flag signals the arrival of valid data at the output stage.
5. DOR goes LOW; data shift-out is complete, FIFO is empty again.
6. $\overline{SO}$ set LOW, necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.



The above waveforms show SI minimum pulse-width and SI maximum pulse frequency, in high-speed Shift-In burst mode.

Fig. 9 - SI pulse-width timing waveforms.

NOTE:
In the high-speed mode, the burst-in rate is determined by the minimum Shift-In HIGH and Shift-In LOW specifications. The DIR status flag is a don't care condition, and a Shift-In pulse can be applied regardless of the flag. An SI pulse which would overflow the storage capacity of the FIFO is not permitted.

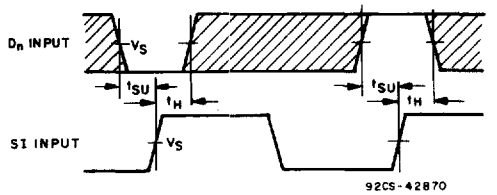


The above waveforms show $\overline{SO}$ minimum pulse-width and maximum pulse frequency, in high-speed, Shift-Out burst mode.

Fig. 10 - $\overline{SO}$ pulse-width timing waveforms.

NOTE:
In the high-speed mode, the burst-out rate is determined by the minimum Shift-Out HIGH and Shift-Out LOW specifications. The DOR flag is a don't care condition and an $\overline{SO}$ pulse can be applied regardless of the flag.

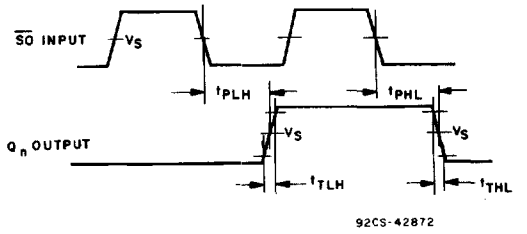
CD54/74HC7030
CD54/74HCT7030



NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

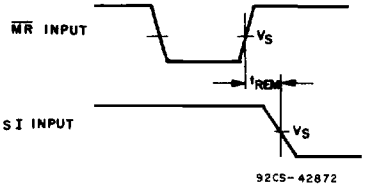
The above waveforms show hold and set-up times for D_n and SI input.

Fig. 11 - Hold and set-up timing waveforms.



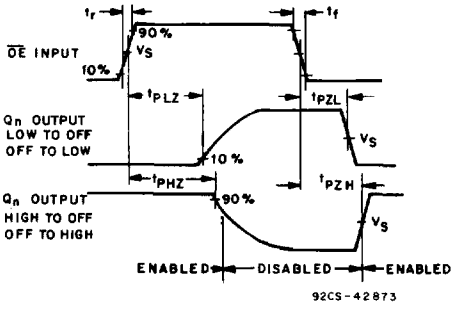
The above waveforms show $\overline{SO}$ input to Q_n output, propagation delay times, and output transistion times.

Fig. 12 - Propagation delay and transition timing waveforms.



The above waveforms show $\overline{MR}$ output and SI input removal time.

Fig. 13 - Removal timing waveforms.



The above waveforms show the 3-state enable and disable times for input $\overline{OE}$.

Fig. 14 - 3-state enable and disable timing waveforms.

CD54/74HC7030
CD54/74HCT7030

Application Information on Expanded Format

Fig. 16 shows two FIFOs connected in cascade. The obtained capacity is 128 words of 9 bits.

Fig. 17 shows the signals on the nodes of both FIFOs at the application of one Shift-In pulse when the FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFO A. As $\overline{SO}$(A) is HIGH at this time instant a DOR(A) pulse is generated. The width of this DOR(A) pulse and the timing between the rising edge of this pulse and the signal change of Q_n(A) meets the requirement of SI(B) and D_n(B) of FIFO B. After a second ripple through delay data arrives at the output of FIFO B (Q_n(B)).

Fig. 18 shows the signals on these nodes after the application of an $\overline{SO}$(B) pulse when both FIFOs are initially full. After a bubble-up delay a DIR(B) pulse is generated that serves as a $\overline{SO}$(A) pulse for FIFO A. One word is transferred from the output of FIFO A to the input of FIFO B. The width of DIR(B) meets the requirements of the $\overline{SO}$(A) pulse of FIFO A. After a second bubble-up delay an empty space arrives at D_n(A) at which time instant DIR(A) goes HIGH.

Fig. 19 shows the waveforms at all external nodes of these two registers during a complete Shift-In and Shift-Out sequence.

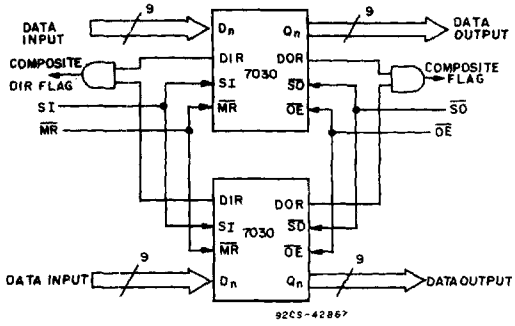


Fig. 15 - Functional diagram of expanded FIFO for increased word length - 64-words x 18-bits.

NOTE:
The 7030 is easily expanded to increase word length. Composite DIR and DOR flags are forced with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay for the flags.

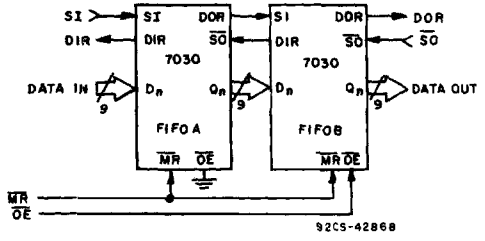


Fig. 16 - Functional diagram of cascaded FIFOs for increased word capacity - 128-words x 9-bits.

NOTE:
The 7030 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Fig. 19 demonstrates the intercommunication timing between FIFO A and FIFO B. Figs. 17 and 18 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

CD54/74HC7030
CD54/74HCT7030

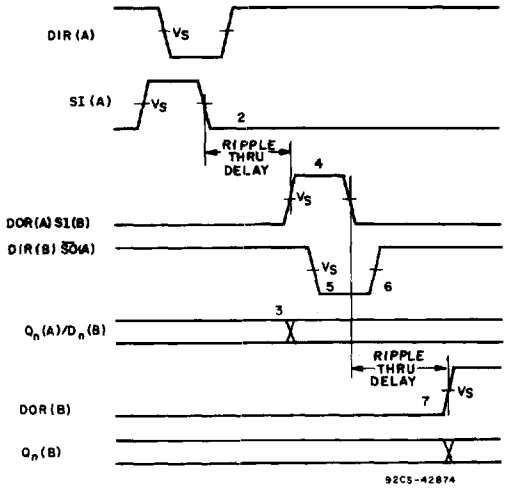


Fig. 17 - FIFO to FIFO communications timing waveforms, input timing under empty condition.

NOTES:
1. FIFO(A) and (B) initially empty, $\overline{SO}$(A) held HIGH in anticipation of data.
2. Load one word into FIFO(A) SI pulse applied, results in DIR pulse.
3. DOR(A) and SI(B) pulse HIGH; (ripple through delay after SI(A) LOW) data is unloaded from FIFO(A) as a result of the data output ready pulse, data is shifted into FIFO(B).
4. Data-out(A)/data-in(B) transition; valid data arrives at FIFO(A) output stage simultaneously with DOR flag, meeting data input set-up requirements of FIFO(B).
5. DIR(B) and $\overline{SO}$(A) go LOW; flag indicates input stage of FIFO(B) is busy, shift-out of FIFO(A) is complete.
6. DIR(B) and $\overline{SO}$(B) go HIGH: automatically, input stage of FIFO(B) is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data.
7. DOR(B) goes HIGH; (ripple through delay after SI(B) LOW) valid data is present one propagation delay-time later at the FIFO(B) output stage.

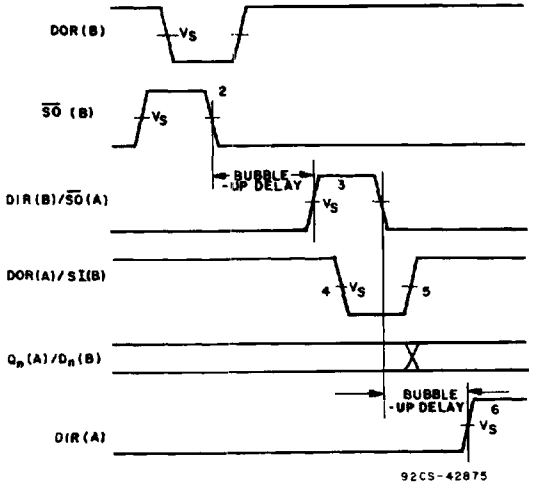


Fig. 18 - FIFO to FIFO communications timing waveforms, output timing under full condition.

NOTES:
1. FIFO(A) and (B) initially full, SI(B) held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word from FIFO(B); $\overline{SO}$ pulse applied, results in DOR pulse.
3. DIR B and $\overline{SO}$(A) pulse HIGH; (bubble-up delay after $\overline{SO}$(B) LOW) data is loaded into FIFO(B) as a result of the DIR pulse, data is shifted out of FIFO(A).
4. DOR(A) and SI(B) go LOW; flag indicates the output stage of FIFO A is busy, shift-in to FIFO(B) is complete.
5. DOR(A) and SI(B) go HIGH; flag indicates valid data is again available at FIFO(A) output stage, SI(B) is held HIGH, awaiting bubble-up of empty location.
6. DIR(A) goes HIGH; (bubble-up delay after $\overline{SO}$(A) LOW) an empty location is present at input stage of FIFO(A).

CD54/74HC7030
CD54/74HCT7030

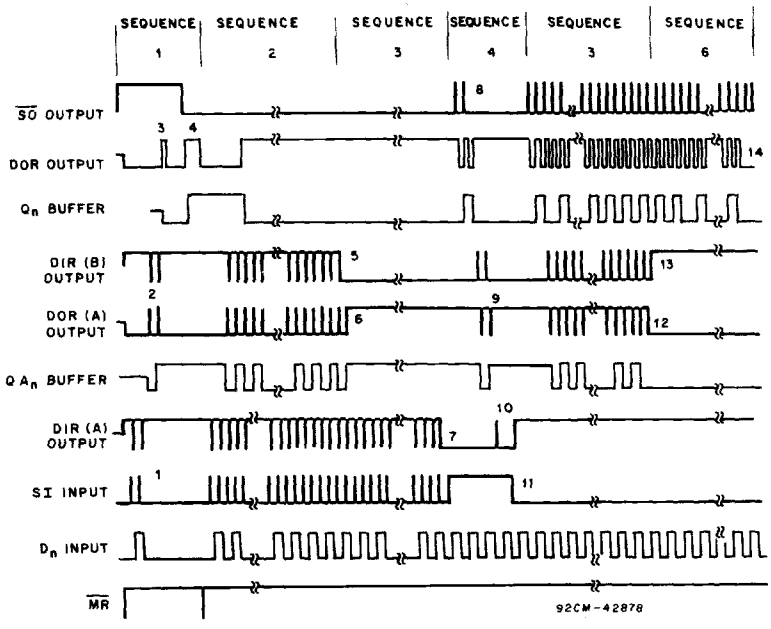


Fig. 19 - Function and intercommunication timing waveforms between two cascaded FIFOs (see Fig. 16 for corresponding pin description).

NOTES:

Sequence 1:

Both FIFOs are empty shift-in process starts.

After a $\overline{MR}$ pulse has been applied FIFO A and FIFO B are both empty. The DOR flag of both FIFOs become LOW because no valid data is present at the outputs. The DIR flags are set HIGH because the FIFOs are ready to accept data. $\overline{SO}$; (B) is held HIGH and two SI(A) pulses are applied (see instant 1). These pulses allow two data words to ripple through to the output stage of FIFO A, and they are loaded into FIFO B (see instant 2). When data arrives at the output of FIFO B, a DOR(B) pulse is generated (see instant 3). When at instant 4, $\overline{SO}$ (B) is turned LOW the first bit is shifted out and the second bit ripples to the output after which DOR(B) becomes HIGH.

Sequence 2:

FIFO B runs full.

After a $\overline{MR}$ pulse, a series of 64 SI pulses are applied by which 64 words are shifted in. Finally DIR(B) remains LOW because FIFO B is full (see instant 5). DOR(A) ends up LOW because FIFO A is again empty.

Sequence 3:

FIFO A runs full.

When 65 words are shifted in, DOR(A) remains HIGH because valid data remains at the output stage of FIFO A. After this Q_n(A) remains HIGH being the polarity of the applied 65th data word (see instant 6). After the 128th SI pulse DIR(A) remains LOW because both FIFOs are full (see instant 7). At additional SI pulses no data transfer occurs.

Sequence 4:

Both FIFOs are full shift out process starts.

SI(A) held HIGH and two $\overline{SO}$ (B) pulses are applied (see instant 8). These pulses shift out two words and thus allow two empty locations to bubble up to the input stage of FIFO B, and then proceeding their way to FIFO A (see instant 9). When the first empty location arrives at the input of FIFO A a new word is shifted in immediately during which a DIR(A) pulse is generated (see instant 10). When at instant 11, SI is turned down the second empty location reaches the input after which DIR(A) remains HIGH.

Sequence 5:

FIFO A runs empty.

FIFO A contains 63 valid words now, because in sequence 4 two words were shifted out and one was shifted in again. An additional series of $\overline{SO}$, (B) pulses is applied. After 63 $\overline{SO}$, (B) pulses all words from FIFO A are shifted into FIFO B, DOR(A) remains LOW (see instant 12).

Sequence 6:

FIFO B runs empty.

After the next $\overline{SO}$ (B) pulse, DIR(B) remains HIGH, because the input stage of FIFO B is empty now (see instant 13). After another 63 $\overline{SO}$ (B) pulses, DOR(B) remains LOW, because both FIFOs are empty again (see instant 14). Additional $\overline{SO}$ (B) pulses don't result in a transfer of information, but the last word remains available at the output Q_n.